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SINGLE-ELECTRON TRANSISTORS FOR FUTURE APPLICATIONS*

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Single electron transistors with wire channels are fabricated by a nanoelectrode-pair technique. Their characteristics strongly depend on the channel widths and the voltages on the in-plane gates. A few dips in the Coulomb blockade oscillations were observed at the less positive gate voltages for a device with a 70nm-wide wire due to Coulomb blockade between the coupled dots. By applying negative voltages to the in-plane gates, the oscillations became periodic, which indicated the formation of a single dot in the conducting channel. These gates facilitate fabricating single-electron transistors with single dot structures, which have potential applications on its integration.

Keywords: single-electron tunneling, Coulomb blockade, quantum dots
PACC: 7280E, 7335C, 7340G

With the recent rapid progress of fabrication techniques for nanostructures, many types of single-electron transistors (SET) have been fabricated. From the engineering viewpoint, single-electron transistors with wire channels[1−7] have a larger chance to be used to construct next-generation electronics with new system architectures. These transistors are not only suitable for their integration but also have potential applications in investigating quantum effects. Efforts have been paid to raise their working temperatures. The operation at room temperature for such kinds of devices has also been reported.[2] However, some of these devices have shown complicated behaviors because of the formation of multiple-dots in the wire channels. The realization of the high-temperature operation for these devices is mainly dependent on the channel width. As the channel width is decreased, the fluctuation of the geometric width becomes more serious. This leads to the formation of multiple-dots. Therefore, it is very important to develop techniques which can be used to realize one single dot in the narrow channels. We have combined the in-plane gate technique and the split-gate technique and developed them into a nanoelectrode-pair technique. By using this technique, we fabricated Si single-electron transistors with in-plane point contact metal (IPPCM) gates by using a self-aligned process. Point contacts were formed by etching a constriction with a designed length of 100nm and a width of 70nm. The effective width of the conducting area can be modified by biasing the IPPCM gates. The pattern was defined by photolithography and mesa-etching.

Figure 1 shows the schematic view of the single-electron transistors with IPPCM gates. A (001) oriented, p-type silicon-on-insulator (SOI) substrate prepared by the separation by implanted oxygen (SIMOX) technique was employed. The silicon single crystal layer was thinned by repeated thermal oxidation and HF etching of the oxide to 70nm. A point contact channel was formed in the Si layer between source and drain electrodes by photolithography and electron-cyclotron-resonance (ECR) plasma etching. Then the wafer was subjected to thermal oxidation in dry oxygen ambient. By using a self-aligned process, IPPCM gates were deposited. This was realized by rotating the wafer to expose both sides of the channel during evaporation. A layer of silicon dioxide with the thickness of 80nm was deposited and finally a top metal gate was formed. The oxide layer serves to insulate the IPPCM gates and the top gate. Applying positive voltages to the top gate leads to the formation of two-dimensional electron gases (2DEGs) at the inversion layer and controls the electrostatic potential of the SET island. Here we report on transport beharior of one device with 70nm-wide channel.

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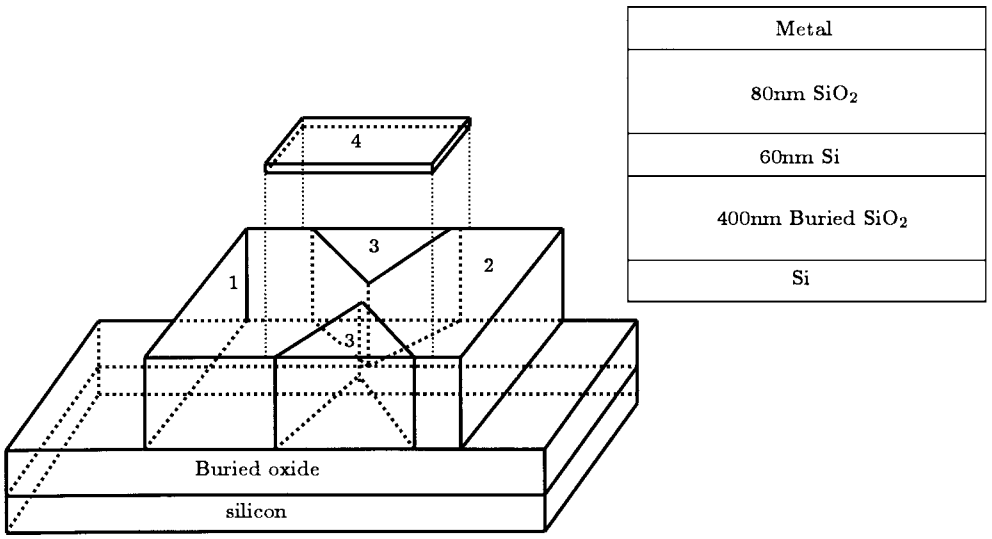


Fig.1. A schematic illustration of the fabricated device. The source and the drain are indicated by 1 and 2, the in-plane gates by 3, and the top gate by 4.

Figure 2 shows the drain current I_2 versus the top gate voltage V_4 characteristic of the device with 70nm-wide channel. The source is grounded. With scanning V_4, I_d oscillates and decreases significantly at V_4 <3.5V. Above V_4=3.5V, both the amplitude of the oscillations and the minimum of the current change a little. In the range of 0.22V< V_4 <3.5V, I_d shows peaks at 2.16, 1.89, 1.36, 1.12, and 0.53V, and also exhibits dips at 2.26, 1.97, 1.41, and 0.90V. The shape of these three peaks is irregular and similar to that of the peaks above 3.5V. The irregular shape is typical characteristic of the Coulomb blockade oscillations (CBOs) through coupled dots.[7−9] Therefore, it can be inferred that a number of dots are formed at the constriction.

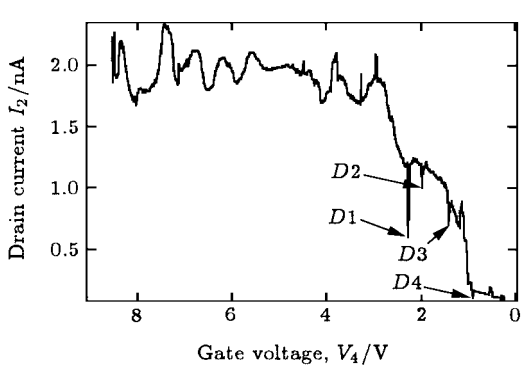


Fig.2. I_2-V_4 characteristic of the device with 70nm-wide channel at V_2=1mV, V_3=0mV, and T=4.2K.

It could be easily understood by simply assuming that five dots be formed, as shown in Fig.3. The dips, which are indicated by $D1$, $D2$, $D3$, and $D4$ in Fig.2 arise from the stochastic Coulomb blockade within the multiple-dot structure.[7−9] Decreasing V_4 reduces the electron density in the inversion layer. Below some critical density, electrons localize in the potential minimum within the channel. So quantum dots are formed at the constriction. We argue that dots are formed even in the range 9V> V_4 >3.5V from the observation of both the irregular shape and their Coulomb staircases.

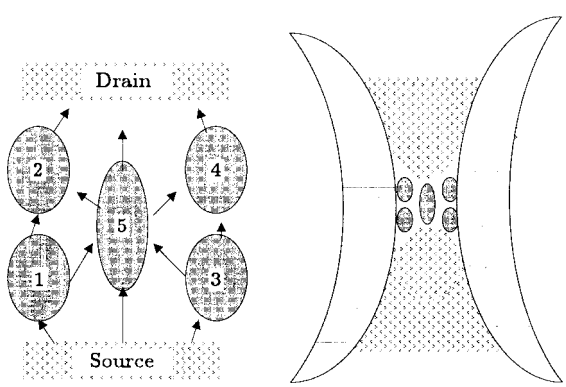


Fig.3. The shape of the channel and formation of the dots. The channel has a length of about 100nm and a width of 70nm.

Considering the shape of the channel, we assume that two dots be formed at each side of the channel and one dot at the center. This is reasonable because the fluctuation of the potential at the edge of the channel is more serious than that at the center of the channel. Transport through the channel is controlled by charging and discharging of all these five dots. For a special arrangement of the charge within the five dots, either Dot-1, Dot-2, and Dot-3 or Dot-5, Dot-2, and Dot-4

are in the Coulomb blockade regime. For such two cases, the channel was blockaded and no electrons can flow through the channel. These gives rise to a sharp drop in the drain current.[6,10,11] The drain current at the four dips in Fig.2 is not zero and this could be partly caused by cotunneling.

Applying negative voltages on the in-plane gates V_3 squeezes the channel and depletes Dot-1, Dot-2, Dot-3, and Dot-4. The electrostatic potential of the four dots is raised so that all the electrons in these four dots are moved out and no other electrons can tunnel into these dots. So the charging and discharging disappear in the four dots. In this case, only Dot-5 controls the current flow through the channel and this leads to the observation of the CBOs with a period of 0.64 V in Fig.4.

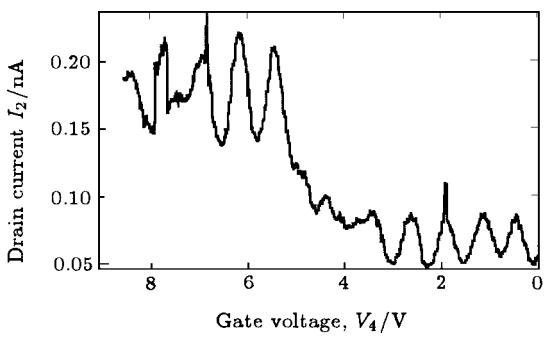


Fig.4. Coulomb blockade oscillations of the devices with 70nm-wide channel at V_2=1mV, V_3=−116mV, and T=4.2K.

Formation of dots could arise from (1) the thickness fluctuations of the SOI layer, (2) the fluctuation of the channel width, (3) pattern dependent oxidation, (4) strain by etching and oxidation, (5) localized states and (6) Si nanoparticles at the interface between the SOI layer and the buried oxide layer. The narrow channel in our case is a point contact wire and the period of the thickness fluctuations should be much larger than its wire length. This rules out the thickness fluctuations for the formation of the dots. Ishikuro *et al.*[2] reported formation of the dots resulting from the fluctuation of the channel width. This contradicts our results on formation of multiple-dots for the devices with wide channels. We also checked the devices without thermal oxidation and found that CBOs could not be observed in these devices. So the considerable band gap shrinkage[12] from the oxidation induced compressive strain probably accounts for the formation of the dots in our devices.

In summary, we investigated a Si single-electron transistor with in-plane point metal gates. The device with 70nm-wide channel exhibited dips in the $I_2 - V_4$ characteristic, which were attributed to stochastic Coulomb blockade within the multiple-dot structure. By applying negative voltages on the in-plane gates, the device showed clear periodic CBOs. These indicate that the in-plane point gates can be used to realize single-electron transistors with single dot structures.

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