Recent Advances in Heteroepitaxial Growth and Non-Epitaxial Integration of Ga_2O_3 on Silicon

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Abstract: Gallium oxide (Ga_2O_3) is an emerging semiconductor with a wide bandgap of 4.8–5.3 eV, featuring ultra-high breakdown electric field strength, great thermal stability, and resistance to extreme environments, making it an ideal choice for deep ultraviolet optoelectronic devices, high-power electronic devices, high-frequency Radio Frequency (RF) devices, etc. However, the difficulty in obtaining large-area, high-quality epitaxial layers, together with the intrinsically low thermal conductivity of Ga_2O_3, limits its applications. To address these issues, silicon (Si), which possesses good thermal conductivity, as well as the mature and cost-effective semiconductor manufacturing lines, is considered for use as the heteroepitaxial substrate, opening a new path for the low-cost industrialization of Ga_2O_3 and laying the foundation for next-generation power electronics and specialized optoelectronic devices. This paper reviews the crystal phase characteristics of Ga_2O_3, focuses on the lattice and thermal mismatch problems encountered in silicon-based epitaxy, discusses oxide layer removal and buffer layer engineering as conventional heteroepitaxial strategies, and further introduces liquid metal printing as a complementary non-epitaxial integration approach. The current research limitations and future development directions are also discussed.

Key words: Si-based Ga_2O_3, native oxide layer removal, buffer layer, liquid metal printing, non-epitaxial integration

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1. Introduction

In recent years, wide-bandgap semiconductors represented by silicon carbide (SiC), gallium nitride (GaN), and gallium oxide (Ga_2O_3) have exhibited broad application prospects in power electronics, optoelectronic devices, and power devices. They have garnered extensive attention from researchers and emerged as hotspots in wide-bandgap semiconductor research.[1, 2] Ga_2O_3 exists in five crystal polymorphs (α, β, γ, δ, ε/κ), and possesses abundant physical and chemical properties.[3-7] Of all crystal polymorphs, the β-phase possesses superior thermodynamic stability and represents the most thoroughly investigated crystalline form. As presented in Table 1, compared with other mainstream semiconductor materials, β-Ga_2O_3 is well-known for featuring a wider bandgap energy (E_g), higher critical breakdown electric field strength (E_{br}) and a superior Baliga figure of merit (BFOM). These outstanding intrinsic properties establish it as a highly promising candidate for next-generation power electronic and optoelectronic systems.[8, 9] Consequently, β-Ga_2O_3 has been widely utilized in the fabrication of various devices, including field-effect transistors,[10, 11] metal-oxide-semiconductor field-effect transistors,[12, 13] photodetectors,[14-16] Schottky barrier diodes,[17, 18] and heterojunction diodes.[19, 20] These devices play crucial roles in defense and aerospace fields such as radar systems, missile detection, and wireless communications.

However, despite the outstanding intrinsic material properties of Ga_2O_3, the large-scale application of its devices remains hindered by several issues associated with homoepitaxial growth. A key advantage of β-Ga_2O_3 is that bulk single crystals can be grown from the melt, enabling the fabrication of native substrates. Nevertheless, commercially available native β-Ga_2O_3 substrates at the current stage still suffer from practical manufacturing challenges, including relatively high production costs, limited available wafer sizes, and non-negligible dislocation density. These issues are all process- and industry-related constraints that can be gradually addressed and optimized

with the development of crystal growth and wafer fabrication technologies. In terms of the material itself, bulk β-Ga_2O_3 exhibits intrinsically low and strongly anisotropic thermal conductivity, with reported room-temperature values ranging from approximately 10.9 to 27.0 $W \cdot m^{-1} \cdot K^{-1}$ along different crystallographic directions.[21, 22] This anisotropic thermal transport originates from the intrinsic phonon properties of the monoclinic crystal and represents a fundamental limitation for thermal management in high-power β-Ga_2O_3 devices. Consequently, severe self-heating may occur during high-power operation, adversely affecting device stability and long-term reliability. To circumvent these challenges, the focus of contemporary research has increasingly shifted toward the heterogeneous integration of Ga_2O_3 on silicon (Si) substrates. Beyond providing high-quality, large-area templates at a fraction of the cost of native substrates, Si possesses a thermal conductivity of approximately 148 $W \cdot m^{-1} \cdot K^{-1}$. This nearly ten-fold increase over bulk Ga_2O_3 establishes an efficient primary heat dissipation path, effectively mitigating the localized heat accumulation that typically plagues power modules. While this thermal advantage is indeed significant, it should not be overestimated without considering the thermal boundary resistance (TBR) that inherently exists at the Ga_2O_3/Si heterointerface. Quantitative modeling reveals a room-temperature interface thermal conductance (ITC) of only 0.47–1.01 $GW \cdot m^{-2} \cdot K^{-1}$, indicating a substantial temperature drop occurs right at the interface rather than within the Si substrate.[23] Moreover, as the thermal conductivity of the heat-spreading substrate increases, the overall thermal bottleneck gradually shifts from the substrate itself to the heterointerface, making the TBR an increasingly dominant factor in high-power operation.[24] The presence of amorphous interfacial layers, which are commonly formed during the initial stage of heteroepitaxy, can further reduce the ~~interface~~ ITC by approximately 24%.[25] Therefore, to fully exploit the thermal benefits of the Si substrate, the TBR must be minimized through careful interface engineering, for instance, by optimizing interfacial smoothness, minimizing amorphous interlayers, or selecting appropriate buffer layers. Furthermore, the mature mechanical properties of silicon facilitate advanced thinning and packaging techniques that are not yet viable for brittle oxide substrates. From a

systems-integration perspective, utilizing a silicon platform enables seamless compatibility with existing high-volume Complementary Metal-Oxide-Semiconductor (CMOS) fabrication lines. This synergy paves the way for the monolithic integration of Ga_2O_3 power devices alongside Si-based logic and driver circuitry, offering a pathway toward highly compact, multifunctional power-system-on-chip (PSoC) architectures.

Despite its compelling advantages, the practical heteroepitaxy of β-Ga_2O_3 on Si substrates remains a formidable challenge, fundamentally constrained by severe material incompatibilities. The lattice mismatch (~22.14%) and the naturally grown SiO_2 layer on silicon substrates can significantly degrade the performance of β-Ga_2O_3 devices.[26] Furthermore, the Coefficient of Thermal Expansion (CTE) mismatch presents a significant bottleneck. At room temperature, the CTE of β-Ga_2O_3 (6.0×10^{-6} K^{-1}[27]) is more than twice that of Si (2.54×10^{-6} K^{-1}[28]). This disparity induces massive tensile stress during the post-growth cooling phase, often exceeding the critical fracture limit and leading to wafer bowing or catastrophic film cracking. Moreover, direct growth of β-Ga_2O_3 on Si at elevated temperatures suffers from several drawbacks. Ga metal will react with Si by meltback etching at high temperatures, which will result in the nonuniform growth of epitaxial film.[29] Beyond lattice mismatch and CTE disparity, various factors collectively limit the heteroepitaxial quality of Ga_2O_3 on Si. Here we focus on two particularly critical ones, namely threading dislocations (TDs) and elemental interdiffusion. The large misfit strain typically generates TD densities in the range of 10^{10}–10^{11} cm^{-2}, which act as carrier scattering centers and non-radiative recombination pathways, severely degrading mobility and increasing leakage current.[30] Concurrently, elevated growth temperatures provoke substantial Ga–Si interdiffusion, introducing deep-level traps and parasitic conductive channels that compromise device reliability. The necessity of suppressing these defects is further evidenced by the effectiveness of diffusion-barrier interlayers, such as titanium nitride (TiN), in blocking mutual diffusion.[31] In response to these multi-faceted issues, current research efforts have converged on several key

mitigation strategies.

To address the issues of oxide layer interference, severe lattice and thermal mismatch, and high epitaxial defect density in Ga_2O_3/Si heterogeneous integration, existing mainstream research encompasses multiple technical routes. As shown in Fig. 1, these strategies can be broadly divided into two categories: conventional heteroepitaxial approaches, including substrate pretreatment and buffer-layer engineering, and emerging non-epitaxial integration approaches represented by liquid metal printing.

Building upon this context, this review aims to provide a comprehensive overview of the current state of the art in the heteroepitaxial growth and non-epitaxial integration of Ga_2O_3 on Si. We systematically examine the growth mechanisms, the evolution of structural defects, and the latest breakthroughs in interfacial engineering. By identifying the remaining gaps between theoretical potential and experimental reality, this paper seeks to provide a strategic roadmap for the development of high-performance, cost-effective Ga_2O_3-on-Si power electronics and optoelectronic systems.

Table 1. Comparison of properties of β-Ga_2O_3 with other semiconductor materials. [32]

Physical properties	Si	4H-SiC	GaN	β-Ga_2O_3
E_g (eV)	1.1	3.3	3.4	4.8
ε	11.8	9.7	9.0	10–12
μ ($cm^2/V \cdot s$)	1400	1000	1200	200
E_{br} (MV/cm)	0.3	2.5	3.3	7–8
BFOM relative to Si	1	340	870	3444
TC ($W \cdot m^{-1} \cdot K^{-1}$)	150	270	210	27

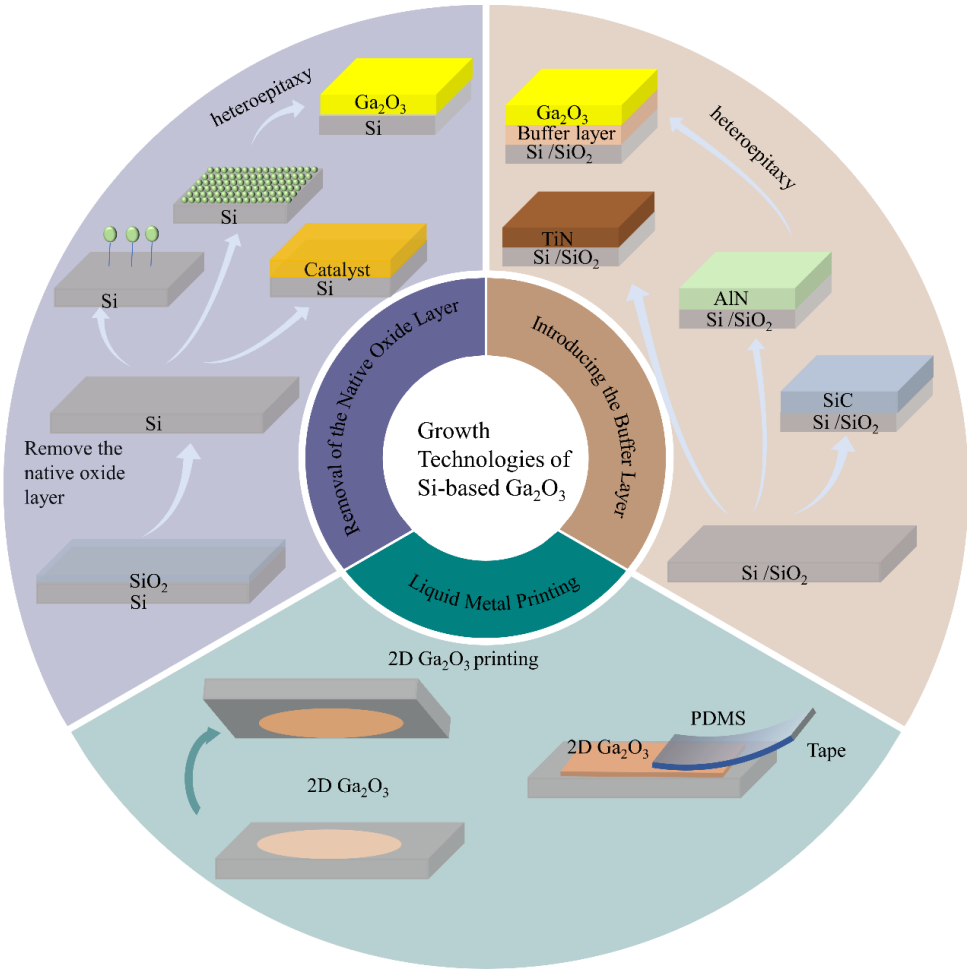


Fig. 1. Strategies for Ga_2O_3/Si heterogeneous integration

2. Material Properties of Gallium Oxide

This section summarizes the crystal structures and key physical properties of Ga_2O_3.

Fig. 2 (a) shows the corundum-type structure of α-Ga_2O_3. Similar to corundum (α-Al_2O_3), α-Ga_2O_3 belongs to the trigonal crystal system with a space group of $R\bar{3}c$. High-quality α-Ga_2O_3 heteroepitaxy can be achieved on sapphire, owing to the structural similarity and relatively small lattice mismatch.[33] The bandgap of α-Ga_2O_3 is between 5.1 eV and 5.3 eV.[34, 35] Its wider bandgap is associated with a high theoretical critical electric field, reported to reach approximately 9.5 MV/cm.[36]

As illustrated in Fig. 2 (b), β-Ga_2O_3 crystallizes in the monoclinic system with space group C2/m. Its unit cell contains both four-coordinated (Ga1) and six-coordinated (Ga2) gallium atoms, as well as three coordinated (O1/O3) and four coordinated (O2) oxygen atoms. β-Ga_2O_3 exhibits the highest thermodynamic stability, crystallizing in

the monoclinic crystal system with a space group of C2/m.[37] The bandgap of β-Ga_2O_3 is measured to be ~ 4.8 eV via the optical transmission method, arising from the electron transition from the top of the valence band to the bottom of the conduction band as described by Fermi's Golden Rule.[38]

The crystal structure of γ-Ga_2O_3 is depicted in Fig. 2 (c). It adopts a cubic defect spinel structure (space group $Fd\bar{3}m$), which modifies the electronic energy states and transition pathways. Its atomic arrangement and chemical bonding features govern the electron distribution within the energy bands, enabling electrons to traverse the bandgap via direct or indirect transitions under varying conditions. In direct transitions, electrons move from the valence band maximum (VBM) to the conduction band minimum (CBM), and this energy corresponds to the direct bandgap. In contrast, indirect transitions require phonon-assisted momentum change. The optical bandgap of γ-Ga_2O_3 was analyzed using Tauc plots. Based on the corresponding direct- and indirect-transition relations, the reported direct and indirect bandgaps are approximately 5.0 and 4.4 eV, respectively.[39]

Fig. 2 (d) presents the δ-Ga_2O_3 structure. Currently, experimental studies of δ-Ga_2O_3 remain limited. Via neutron diffraction experiments, Playford et al. demonstrated that the δ phase is essentially the nanocrystalline form of ε-Ga_2O_3.[5] In 2023, the research team from Kyoto Institute of Technology (Japan) first achieved the epitaxial growth of δ-Ga_2O_3 thin films and made a breakthrough in confirming its semiconductor functionality.[40] In February 2025, the team's latest research on δ-Ga_2O_3 has realized its semiconductor functionalization and successfully extended it to deep-ultraviolet (DUV) detection applications.[41]

As shown in Fig. 2 (e), ε-Ga_2O_3 and κ-Ga_2O_3 are two names for essentially the same material. Similar to hexagonal wurtzite-structured ZnO and GaN, ε-Ga_2O_3 lacks inversion symmetry and exhibits a large spontaneous polarization coefficient (≈0.24 C/m^2).[42-44] Reports indicate that the bandgap of ε-Ga_2O_3 ranges from 4.6 to 5.03 eV,[45, 46] endowing it with a high breakdown voltage and making it well-suited for high-voltage and high-power applications analogous to those of β-Ga_2O_3. κ-Ga_2O_3

crystallizes in an orthorhombic structure with a space group of $Pna2_1$ and a bandgap of approximately 4.9 eV. This polymorph exhibits high spontaneous polarization intensity (≈0.23 C/m^2)[47] as well as distinctive ferroelectric and piezoelectric properties.[48] The nearly identical polarization values of ε/κ-Ga_2O_3 arise because the true microstructure is the orthorhombic κ phase, while the conventionally termed "ε phase" is a macroscopic pseudo-hexagonal assembly formed by 120° in-plane rotations of nanoscale κ-domains.[3, 49] Consequently, ε and κ are essentially two names for the same material: κ represents the actual crystal structure, whereas ε is a historical name based on macroscopic observations. Among these polymorphs, β-Ga_2O_3 exhibits the highest thermodynamic stability and serves as the primary research focus for silicon-based heteroepitaxy.

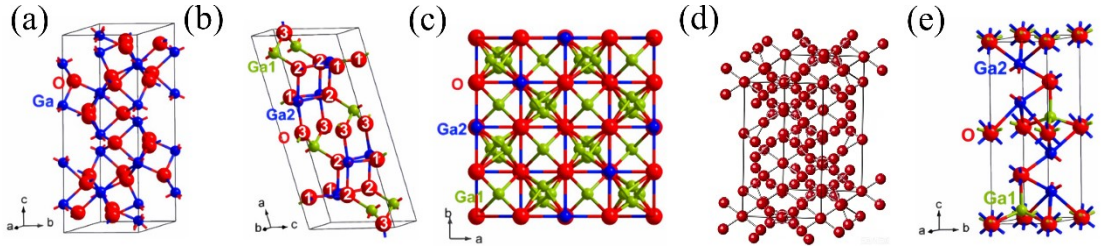


Fig. 2. Crystal structures of five Ga_2O_3 polymorphs: (a) α-Ga_2O_3 (b) β-Ga_2O_3 (c) γ-Ga_2O_3 (d) δ-Ga_2O_3, and (e) ε/κ-Ga_2O_3. Reproduced with permission from Ref. [50]

3. Heteroepitaxial Growth of Ga_2O_3 on Silicon

Si substrates have emerged as a preferred substrate for the heteroepitaxy of Ga_2O_3, owing to their low cost, large-size availability, compatibility with mature semiconductor process flows, and ability to effectively enhance the heat dissipation capability of Ga_2O_3. Various epitaxial techniques, including molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), hydride vapor phase epitaxy (HVPE), and related vapor-phase approaches, have been extensively explored for the growth of Ga_2O_3 thin films and heterostructures.[51, 52] For Si-based heteroepitaxy, however, the native SiO_2 layer together with the substantial lattice and thermal-expansion mismatches introduces additional challenges for nucleation, strain relaxation, and interface quality. These interfacial and structural incompatibilities can lead to degraded crystallinity, high defect densities, and nonideal film morphology.

Early efforts to directly epitaxially grow Ga_2O_3 on Si substrates, as exemplified by the work of D. H. Kim[53] in 2002 and H. W. Kim[54] in 2004, encountered numerous challenges. These included low growth efficiency, poor crystallinity (predominantly amorphous films), high surface roughness, and the presence of unexplained interfacial layers and defects, which are directly attributable to the aforementioned material mismatches and surface issues. Accordingly, this section reviews the major conventional heteroepitaxial strategies, including substrate surface pretreatment (Section 3.1) and buffer-layer engineering (Section 3.2).

3.1 Substrate Surface Pretreatment and Native Oxide Removal

An amorphous native oxide layer inherently exists on Si surfaces. This layer readily introduces interface defects and silicon impurity adsorption, thereby inducing parasitic conductive channels or carrier non-radiative recombination centers[55], which exert a significant impact on the growth of Ga_2O_3 thin films and subsequent device fabrication. After removing this oxide layer, the thickness of the interface transition layer can be reduced to 2–3 nm, leading to a thinner interfacial transition layer and improved interfacial bonding and nucleation conditions. Consequently, the removal of the oxide layer on Si surfaces constitutes a critical prerequisite for growing high-quality Ga_2O_3 thin films. Current mainstream removal methods involve hybrid processes that combine chemical cleaning with other techniques (such as plasma treatment, thermal annealing-induced surface reconstruction, etc.).

Acid solutions, especially Hydrofluoric acid (HF) solution, are typically used to chemically remove the oxide layer on the surface of Si substrate in the semiconductor industry. Due to the strong affinity between fluoride (F) ions and Si atoms, HF (hydrofluoric acid) reacts chemically with SiO_2 to form stable fluorides, such as volatile silicon tetrafluoride (SiF_4) or soluble hexafluorosilicic acid (H_2SiF_6), thereby achieving the dissolution or etching of SiO_2.[56] The conventional steps for removing the oxide layer are as follows: Firstly, the Si substrate is subjected to a standard cleaning, such as ultrasonically cleaned with acetone, isopropanol, and deionized water. Then, its native oxide layer is removed by using diluted HF acid solution (volume ratio

1:100, 1:30, 1:20, etc.), or a sulfuric acid-hydrogen peroxide mixture (SPM) solution with HF solution. After chemical cleaning, Ga_2O_3 can be epitaxially grown on the relatively clean Si surface using methods as shown in Fig. 3, such as plasma pretreatment to introduce hydroxyl active sites, seed layer-induced nucleation growth, and catalyst-modified assisted growth. These strategies aim to compare the effects of different interface engineering approaches on the epitaxial growth behavior of Ga_2O_3.

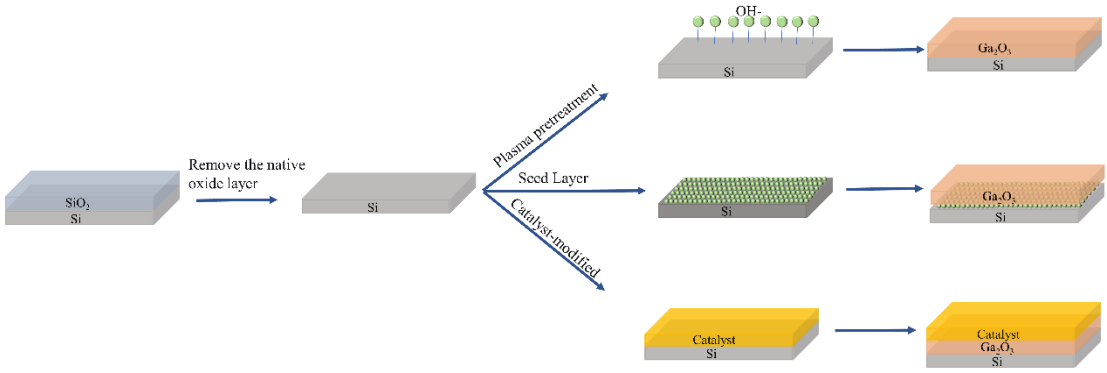


Fig. 3. Comparison of different pretreatment strategies for Ga_2O_3 heteroepitaxy on Si

K. Arora et al.[57] employed a high-temperature Ga_2O_3 seed layer (HSL) to improve the crystallinity and photoresponse of β-Ga_2O_3 thin films grown on Si. The HSL-assisted film exhibited enhanced crystallinity but a higher root-mean-square (RMS) surface roughness (11.55 ± 1.51 nm) than the film grown without HSL (0.31 ± 0.029 nm), which was attributed to the formation of larger crystallites. Under 250 nm illumination at a bias of 5 V, the HSL-assisted photodetector achieved a responsivity of 96.13 A/W and an external quantum efficiency (*EQE*) of 4.768×10^4%. These two values are internally consistent according to the relation between responsivity and *EQE*. The exceptionally high *EQE*, far exceeding 100%, indicates substantial internal photoconductive gain rather than a simple one-photon–one-electron conversion process. The original study attributed this gain to enhanced carrier mobility and shallow trap states at the metal–semiconductor interface, which can trap photogenerated holes, suppress electron–hole recombination, and thereby increase the photocurrent. Under zero-bias operation at 254 nm, the device exhibited rise and decay time constants of 32.2 and 78 ms, respectively. Therefore, the unusually high responsivity and *EQE* should be interpreted together with the applied bias, illumination wavelength,

carrier-trapping dynamics, and response characteristics rather than being treated as directly comparable performance metrics under identical measurement conditions.

Hao et al.[58] innovatively introduced an in-situ NH_3 plasma pretreatment process (13 s plasma exposure + 6 s N_2 purge, 10–70 cycles at room temperature under 2000 W RF power) to optimize the chemically-cleaned Si(100) substrate surface state for the subsequent Ga_2O_3 film growth at 100–400 ℃ (preferentially 250 ℃) via a remote plasma-enhanced atomic layer deposition (RPEALD) technology. NH_3 plasma treatment increased the density of surface hydroxyl (–OH) groups on the Si substrate, raising the film deposition rate from 0.44 Å/cycle to 0.53 Å/cycle while maintaining the film stoichiometric ratio (O/Ga ~ 1.3) and surface morphology; the resulting film on Si exhibits a low surface roughness of 0.117 nm.

R. Saha et al.[59] prepared single-crystalline β-Ga_2O_3 thin films on Si substrates using a catalyst-modified vapor–liquid–solid (VLS) technique. The VLS method is a catalyst-assisted growth approach that dissolves vapor-phase precursors in a liquid metal alloy and precipitates them at the liquid–solid interface to produce high-quality single crystals. The Si substrates were cleaned by a standard procedure and immersed in 1:100 diluted HF solution for 5 min to eliminate native oxide. The VLS growth employed β-Ga_2O_3 powder synthesized via chemical bath deposition (CBD) mixed with graphite powder at a mass ratio of 1:3, carried out at 250 ℃ under argon flow for 3 min. The resulting continuous β-Ga_2O_3 single-crystal film exhibits a thickness of ~ 15 nm, grain size of 20.41 nm, RMS surface roughness of 2.55 nm, optical bandgap of 4.78 eV, refractive index of 1.84, extinction coefficient of 0.10 (at 260 nm), and transmittance of approximately 60%.

The three pretreatment approaches exhibit distinct trade-offs in processing temperature, film quality, deposition efficiency, and device performance. The HSL strategy improves crystallinity and photodetection performance, although the formation of larger crystallites is accompanied by increased surface roughness. [57] The in-situ NH_3 plasma pretreatment activates the Si substrate to generate abundant hydroxyl groups, effectively increasing film deposition rate while maintaining the original film

stoichiometry and ultra-smooth surface morphology. This room-temperature pretreatment avoids thermal damage and enables efficient and high-quality low-temperature film deposition.[58] In contrast, the catalyst-modified VLS growth combined with dilute HF etching pretreatment removes the native oxide layer on the Si substrate to optimize the growth interface, which facilitates the growth of continuous single-crystal β-Ga_2O_3 films with good crystallinity, uniform grain size and stable and reliable optical parameters, exhibiting unique advantages in preparing high-quality single-crystal oxide thin films.[59] Although these pretreatment strategies can improve the initial Si surface and subsequent Ga_2O_3 nucleation, they cannot completely resolve the intrinsic lattice and thermal mismatches between Ga_2O_3 and Si. Therefore, buffer-layer engineering provides an additional strategy for further improving the heteroepitaxial interface.

3.2 Buffer Layer Engineering for Ga_2O_3/Si Heteroepitaxy

Direct growth of Ga_2O_3 following merely the removal of the Si surface oxide layer tends to introduce a high density of defects, such as dislocations and cracks. In contrast, a buffer layer can mitigate the adverse effects of these mismatches through lattice transition and stress relaxation, thereby offering multiple advantages. It not only enhances the crystalline quality and structural integrity of the Ga_2O_3 film,[60] but also maintains compatibility with mature Si-based semiconductor processes, enabling low-cost, large-area fabrication and device integration. Additionally, the buffer layer improves the adhesion between the film and the substrate, leading to enhanced electrical performance and long-term stability of the resulting devices. As shown in Fig. 4, the widely studied buffer layer materials include aluminum nitride (AlN), SiC, TiN, and so on.

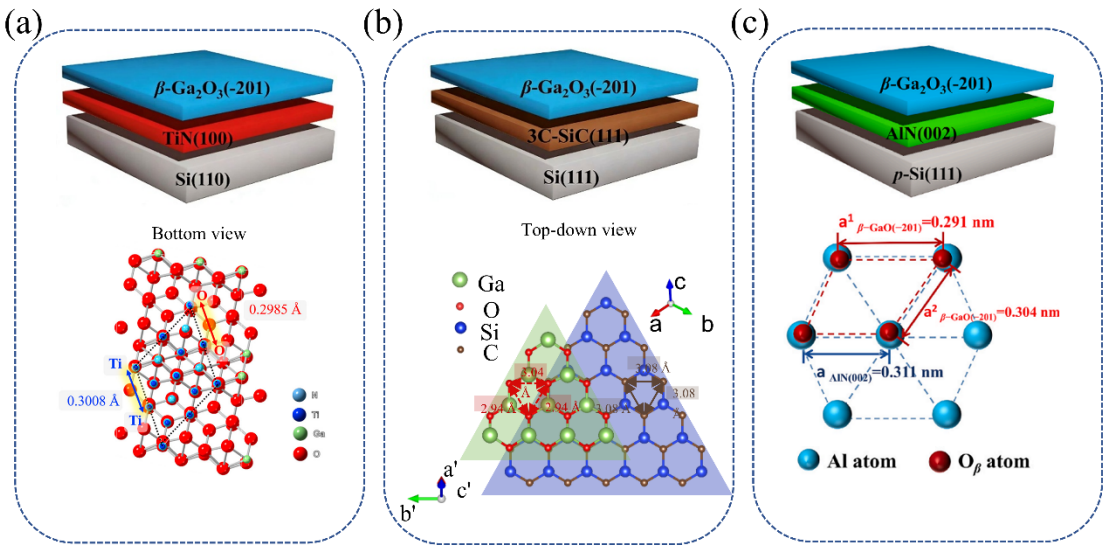


Fig. 4. Schematic of β-Ga_2O_3 thin film heterostructures with (a) TiN, (b) 3C-SiC, and (c) AlN buffer layers on Si substrates. Schematic illustration prepared by the authors based on Ref. [31]

3.2.1 AlN buffer layer

Wang et al.[31] used an AlN buffer layer to mitigate lattice and thermal mismatches between β-Ga_2O_3 and Si, and systematically optimized key growth parameters including growth temperature and oxygen pressure. As shown in Fig. 5, the AlN buffer layer serves two primary roles: on one hand, it drastically reduces the large lattice mismatch (20.8%–25.7%) between β-Ga_2O_3 (-201) and Si (111) to 2.3%–8.3% at the β-Ga_2O_3 (-201)/AlN (002) interface, and achieves the β-Ga_2O_3 (-201)/AlN (002) crystallographic orientation matching, effectively alleviating interfacial strain and disordered atomic arrangements. On the other hand, it inhibits the formation of native SiO_2 layer on Si, reduces interfacial dangling bond density and defect concentrations (e.g., oxygen vacancies, grain boundaries) in the β-Ga_2O_3 film. Consequently, the films obtain a distinct preferred orientation, a low RMS surface roughness of 3.2 nm and high structural quality. The fabricated Metal-semiconductor-metal (MSM) solar-blind UV photodetectors achieve self-powered operation, with a responsivity of 0.0027 A/W at 225 nm (0 V bias) and 0.005 A/W at 225 nm (5 V bias), presenting favorable solar-blind selectivity and stable photoresponse.

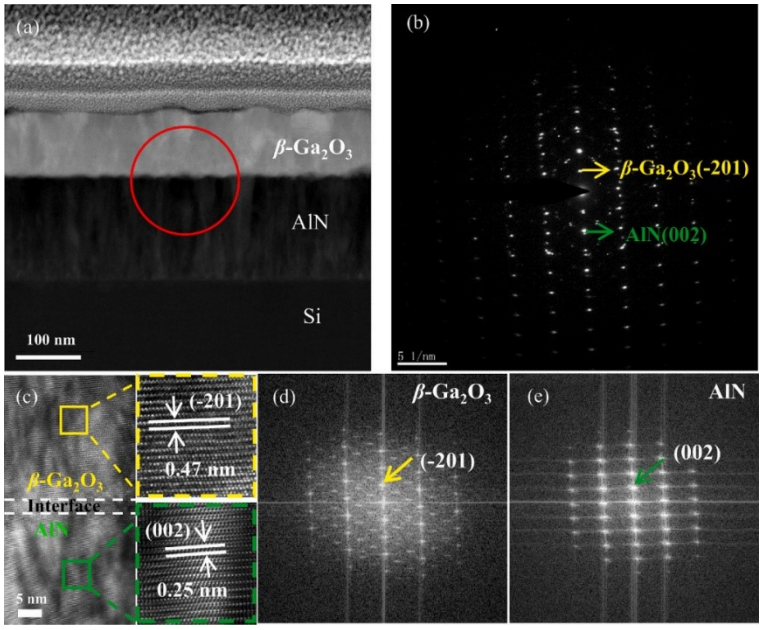


Fig. 5. (a) The Cross-sectional Transmission Electron Microscope (TEM) image of β-Ga_2O_3 film grown at 900 ℃ & 0.02 mbar oxygen pressure. (b) The selected area electron diffraction (SAED) patterns obtained from the region marked by the red circle in (a). (c) Cross-sectional high-resolution TEM (HRTEM) image of the β-Ga_2O_3/AlN interface. (d) Fast Fourier Transformation (FFT) pattern of the β-Ga_2O_3 film. (e) FFT pattern of the AlN buffer layer. Reproduced with permission from Ref. [31]

A. K. Singh et al. [26] deposited β-Ga_2O_3 thin films onto Si (111) substrates via MOCVD by introducing an AlN buffer layer. Material characterizations demonstrated that without the AlN buffer layer, an amorphous SiO_x interlayer was formed at the β-Ga_2O_3/Si interface, accompanied by a polycrystalline β-Ga_2O_3 film with RMS of 3.36 nm. In contrast, the introduction of the AlN buffer layer not only effectively suppressed the formation of an amorphous SiO_x interlayer, but also realized the heteroepitaxial growth of β-Ga_2O_3 (-201) on AlN (002) with a well-defined interface, along with a reduced RMS of 2.17 nm. As a result, the lattice mismatch between β-Ga_2O_3 and Si was significantly reduced from 22.14% to 3.85%, which concurrently enhanced the crystalline quality and lowered the defect density of the β-Ga_2O_3 film. The as-fabricated β-Ga_2O_3/AlN/Si Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) exhibited a breakdown voltage of 178 V, a maximum drain current of 52 mA/mm and an on/off current ratio of ~ 10^8, demonstrating remarkable performance improvement. In addition, Gao et al. [61] systematically studied the epitaxial growth of β-Ga_2O_3 thin films on Si substrates with an AlN buffer layer and fabricated relevant photodetectors.

Comprehensive material characterizations and device performance results verify that the AlN buffer layer is an outstanding candidate buffer scheme.

3.2.2 SiC buffer layer

In 2016, S.A. Kukushkin et al.[62] conducted research on SiC buffer layers: they synthesized a ~ 100 nm-thick 3C-SiC epitaxial buffer layer on Si (111) substrates via the atomic substitution method, followed by growing β-Ga_2O_3 thin films using HVPE. As shown in Fig. 6, the prepared β-Ga_2O_3 thin films (0.5–1.0 μm thick) featured pure β-phase (-201) orientation, and no polycrystalline phases. The SiC buffer layer effectively protected the Si substrate from oxidation and chlorine compound corrosion while realizing orientation control of the thin films. Additionally, the film's dielectric constant varied regularly with photon energy (0.7–6.5 eV), and Raman spectrum characterization revealed that its Raman characteristics were consistent with bulk β-Ga_2O_3, with phonon peaks showing a 1-4 cm^{-1} blue shift.

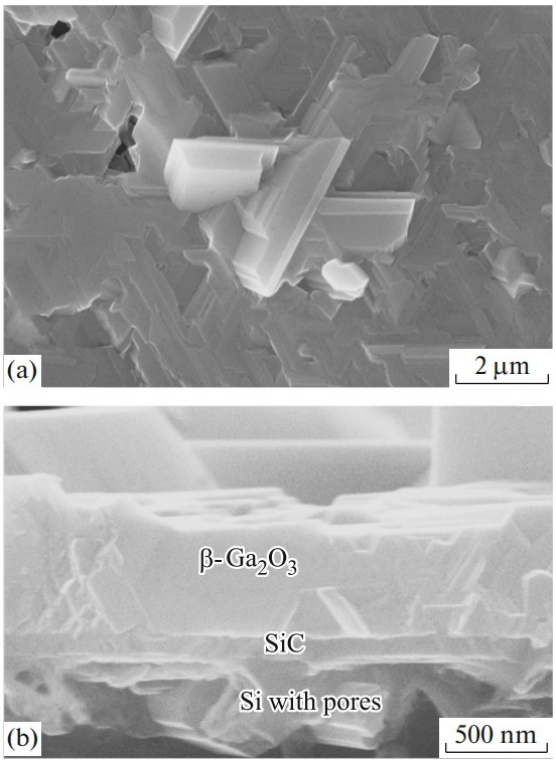


Fig. 6. SEM images: (a) Surface of the sample; (b) Cross-section of the SiC/Si sample and β-Ga_2O_3 layer. Reproduced with permission from Ref. [62]

Furthermore, A. V. Osipov et al.[63] adopted the Modified Coordinated Atomic

Substitution (MCSA) method to synthesize a dislocation-free 3C-SiC buffer layer, which improved the interface quality with the Si substrate and the orientation control of Ga_2O_3 thin films compared to the traditional atomic substitution approach. Notably, this study demonstrated controllable growth of α-, ε-, and β-Ga_2O_3 thin films on 3C-SiC(111)/Si(111) substrates, extending Ga_2O_3/Si heterointegration beyond the β-phase growth predominantly reported in previous studies. The relationships among growth temperature, crystal phase, and film density were further investigated, showing that the metastable α- and ε-phases could transform into the thermodynamically stable β-phase at elevated temperatures. These results provide useful insights into phase control of Ga_2O_3 thin films on Si-based substrates.

3.2.3 TiN buffer layer

C. C. Yen et al.[64] fabricated β-Ga_2O_3/TiN (300 nm)/Si heterostructures via radio-frequency magnetron sputtering. TEM characterization in Fig. 7 revealed that the TiN (111) and β-Ga_2O_3 (-201) interfaces achieved atomic-level flat stacking, with the lattice mismatch between the two layers reduced to 0.76%. This buffer suppressed twin boundaries and stacking faults, improved film crystallinity, and attained a root-mean-square surface roughness of 1.98 nm after 800 °C rapid thermal annealing, while effectively blocking Ga/Si interdiffusion. The optimized lateral Schottky barrier diode exhibited an on-resistance of 3.03×10^4 m$\Omega\cdot$cm^2, a breakdown voltage of 48 V, and a Baliga's figure of merit of 7.60×10^{-2} kW/cm^2, four orders of magnitude higher than that of the TiN-free β-Ga_2O_3/Si diode.

To address the high specific on-resistance in β-Ga_2O_3 integrated with Si (100), M. Mehta et al.[65] introduced a conductive TiN interlayer and devised three process strategies (S1–S3). Fig. 8 revealed that the S3 process (vacuum-based seed layer + forming gas annealing) effectively suppresses Ti–Ga interdiffusion and avoids the formation of a $GaTiO_x$ interfacial barrier, whereas S2 exhibits an intermixing region of approximately 20 nm. The S3 approach ultimately achieved a record-low specific on-resistance of 3.3 m$\Omega\cdot$cm^2, approaching the performance of single-crystal β-Ga_2O_3 devices. The authors further estimated that integration with Si could improve the

effective heat-dissipation capability by approximately 5–10 times, although this estimate did not account for thermal boundary resistance. However, the breakdown voltage remained below 10 V, with leakage current dominated by Poole–Frenkel emission, where electrons are emitted from defect levels located 0.57 eV below the conduction band. High defect density remains a key challenge for further improvement.

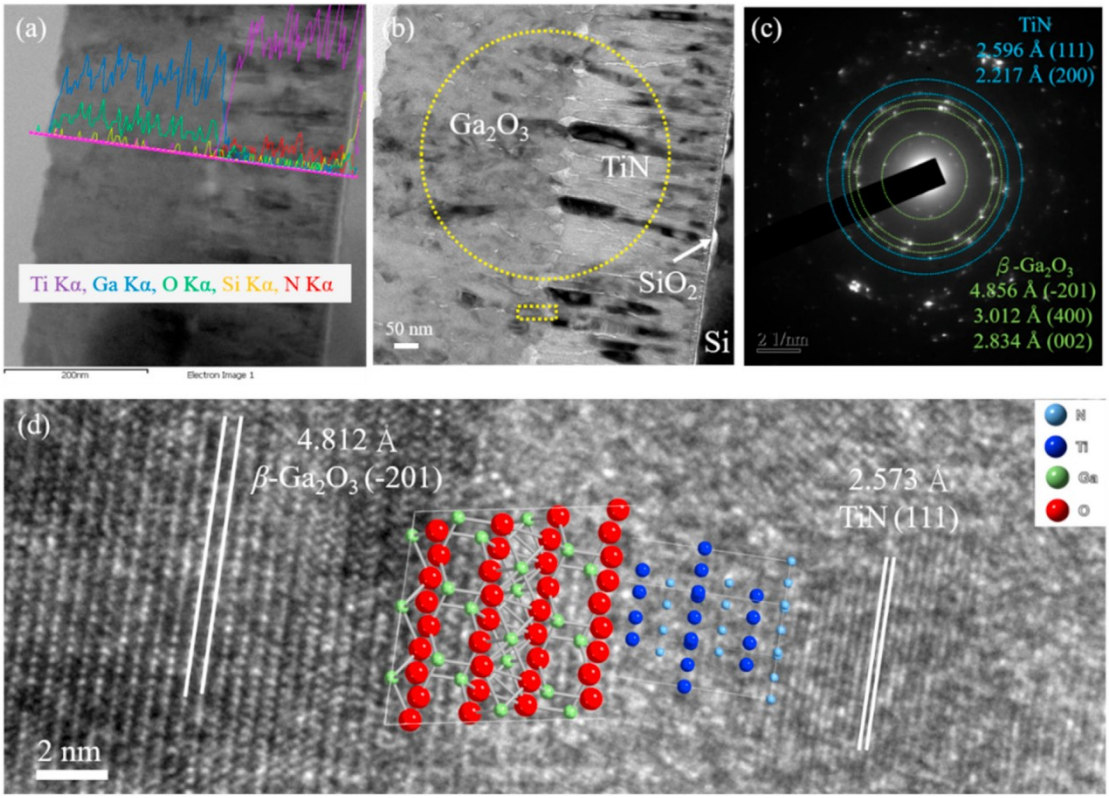


Fig. 7. (a) The TEM-Energy Dispersive Spectroscopy (EDS) line-scan profile across the Rapid Thermal Annealing (RTA) 800 °C β-Ga_2O_3/TiN/Si film, (b) the cross-sectional TEM image of the film, (c) the SAED patterns from the yellow circle as indicated in (b), and (d) the high-resolution TEM image from the yellow square as indicated in (b). Reproduced with permission from Ref. [64]

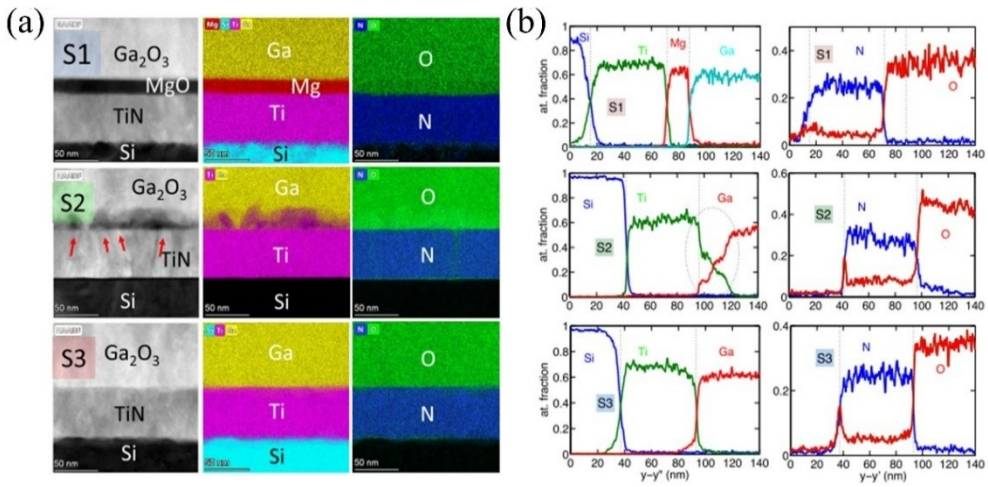


Fig. 8. Ga_2O_3 on TiN/Si cross-sectional TEM images for S1−S3. (a) STEM-HAADF cross-section with Z-contrast and EDS elemental-mapping, (b) element profile along a line-section approximately at the center of the STEM-HAADF images in (a). Reproduced with permission from Ref. [65]

Table 2 summarizes the representative properties and device performances reported for AlN-, 3C-SiC-, and TiN-buffered Ga_2O_3/Si heterostructures. Direct quantitative comparison among these studies should be treated with caution because the reported results were obtained using different growth conditions, film thicknesses, post-treatment processes, device architectures, and measurement protocols. For TiN-buffered structures, a lattice mismatch as low as 0.76% was reported in one study, [64] whereas a separate vertical-diode study demonstrated an on-resistance of 3.3 $m\Omega \cdot cm^2$. [65] These results indicate that TiN can provide advantages associated with its conductive and diffusion-barrier characteristics; however, the reported surface morphology is sensitive to annealing conditions, suggesting the need for careful process optimization. AlN-buffered Ga_2O_3/Si structures have demonstrated relatively smooth surfaces and high breakdown voltages, including an RMS roughness of 2.17 nm and a breakdown voltage of 178 V in the reported MOSFET structure. [26] AlN has also been employed in Ga_2O_3/Si photodetectors, indicating its potential for both electronic and optoelectronic integration. [31] In comparison, 3C-SiC buffer layers have enabled low-defect heterointerfaces and controllable growth of different Ga_2O_3 polymorphs, including α-, ε-, and β-phases, highlighting their potential for phase and orientation engineering. [63] Overall, the available studies suggest that AlN, TiN, and 3C-SiC offer different advantages rather than a universally superior buffer-layer

solution, and their suitability depends on the targeted growth process, interface requirements, and device architecture.

Table 2. Summary of material parameters, lattice mismatch, device performance and thin-film properties for β-Ga_2O_3/buffer layer/Si heterostructures.

Study	Buffer Layers	Lattice Mismatch	Key Thin Film Parameters	Typical Device	Key Device Performance
Singh et al.[26]	AlN	β-Ga_2O_3(-201)/AlN(002):3.85%	RMS = 2.17 nm Carrier mobility = 5.98 $cm^2 \cdot V^{-1} \cdot s^{-1}$	MOSFET	V_{br}= 178 V, I_{ds}(max) = 52 mA/mm, on/off ratio = 10^8, R_{on} = 33.53 m$\Omega \cdot cm^2$
Wang et al.[31]	AlN	β-Ga_2O_3(-201)/AlN(002):2.3% ~ 8.3%	RMS = 3.2 nm E_g = 4.65 eV	Self-powered solar-blind photodetector	Responsivity at 225 nm: 0.0027 A/W (0 V), 0.005 A/W (5 V)
Kukushkin et al.[62]	3C-SiC	Low mismatch	Pure β-phase,	/	/
Osipov et al.[63]	3C-SiC	No misfit dislocations	Surface roughness< 5 nm (α-phase optimal)	/	/
Yen et al.[64]	TiN	β-Ga_2O_3(-201)/TiN (111):0.76%	RMS = 1.98 nm (800 °C optimal)	Lateral SBD	V_{br} = 48 V, R_{on} = 3.03 × 10^4 m$\Omega \cdot cm^2$, BFOM = 7.60 × 10^{-2} kW/cm^2

Study	Buffer Layers	Lattice Mismatch	Key Thin Film Parameters	Typical Device	Key Device Performance
Mehta et al. [65]	TiN	β-Ga_2O_3(100)/TiN (100):1.01%	RMS = 9.4 nm	Vertical power diode	R_{on} = 3.3 mΩ·cm^2 V_{br} < 10 V

In addition, other buffer layers such as gallium nitride (GaN),[66] aluminum oxide (Al_2O_3),[67] strontium titanate ($SrTiO_3$),[68] and yttria-stabilized zirconia (YSZ)[69] have also been reported. Researchers have used these buffer layers to fabricate high-quality Ga_2O_3 films on Si substrates and applied them to various applications.

Collectively, these buffer-layer approaches demonstrate that substantial improvements in Ga_2O_3/Si heteroepitaxy can be achieved through interface and strain engineering. Nevertheless, because conventional heteroepitaxy still relies on crystalline nucleation and growth across dissimilar materials, lattice, thermal, and interfacial constraints cannot be completely avoided. This has motivated increasing interest in non-epitaxial integration strategies that physically decouple film formation from the target Si substrate.

4. Non-Epitaxial Integration of Ga_2O_3 on Silicon: Liquid Metal Printing Method

Unlike conventional heteroepitaxy, liquid metal printing (LMP) is a non-epitaxial integration route based on liquid-metal oxidation and van der Waals transfer.[70] It is discussed here as a complementary strategy for realizing Ga_2O_3/Si heterogeneous integration. Because the transferred Ga_2O_3 layer is coupled to the target substrate primarily through van der Waals interactions rather than coherent epitaxial bonding, LMP relaxes the strict lattice-matching requirement associated with conventional heteroepitaxy. This decoupling can reduce strain associated with direct lattice matching and avoids the high-temperature growth step required in many epitaxial processes. However, it does not eliminate all interfacial or thermal issues, particularly when post-printing annealing is required for crystallization. The key to this method lies in the unique surface chemistry of gallium. Gallium features a low melting point (29.7 ℃)

and can spontaneously form an atomically thin oxide layer under atmospheric conditions.[71] Therefore, this method employs liquid gallium (or gallium-based alloys) as the raw material, leveraging its Cabrera-Mott oxidation mechanism that enables spontaneous formation of atomically thin oxide layers in air.[72] As illustrated in ~~the~~ Fig. 9, by leveraging printing techniques such as extrusion printing, polydimethylsiloxane (PDMS) transfer, or surface tension modulation, two-dimensional (2D) gallium oxide (GaO or β-Ga_2O_3) can be controllably transferred onto Si-based substrates at room temperature. This approach enables large-scale fabrication ranging from centimeter-scale to wafer-scale, breaking through the cost and process bottlenecks associated with the large-area growth of 2D Ga_2O_3 on Si-based substrates.[73]

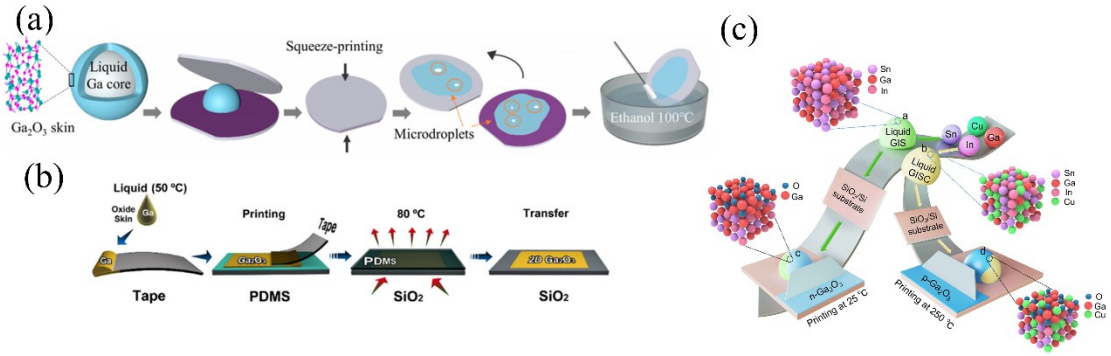


Fig. 9. 2D Ga_2O_3 printing and transfer techniques (a) extrusion printing. Reproduced with permission from Ref. [74] (b) PDMS transfer. Reproduced with permission from Ref. [75] (c) scraping liquid gallium on the substrate with PDMS assistance. Reproduced with permission from Ref. [76]

4.1 Direct Squeeze-Printing

Direct squeeze-printing is a promising low-temperature LMP strategy, enabling seamless Si/SiO_2 integration of atomically thin Ga_2O_3 via Cabrera-Mott self-limiting oxidation and van der Waals transfer. It inherently relaxes lattice mismatch and thermal stress, operating entirely without vacuum or high-temperature annealing.

Xu et al.[74] demonstrated a liquid metal squeeze-printing technique to transfer ultrathin 2D Ga_2O_3 films, formed via self-limiting oxidation of liquid gallium, onto SiO_2/Si substrates at 60 °C. As shown in Fig. 10 (a), the low-magnification TEM image reveals continuous, crack-free films. Corresponding elemental mapping in Fig. 10 (b) and Fig. 10 (c) confirms uniform distribution of Ga and O elements across the film region.

High-resolution TEM in Fig. 10 (d) and selected-area electron diffraction (inset) further verify the amorphous nature of the as-printed Ga_2O_3 film. X-ray Photoelectron Spectroscopy (XPS) spectra of Ga 3d and O 1s, shown in Fig. 10 (e) and Fig. 10 (f), confirm the formation of Ga_2O_3 with typical chemical states. This yielded continuous, uniform amorphous films with a thickness of ~ 3 nm and a surface roughness of 0.160 nm. Pt/ Ga_2O_3/n^+-Si memristors fabricated from these films exhibited forming-free bipolar resistive switching, with a retention time > 10^4 s and an ON/OFF ratio of ~ 100. The devices enabled multi-level resistance modulation and emulated canonical synaptic behaviors, including paired-pulse facilitation, long-term potentiation/depression, and spike-timing-dependent plasticity, establishing a promising 2D oxide platform for low-power neuromorphic computing.

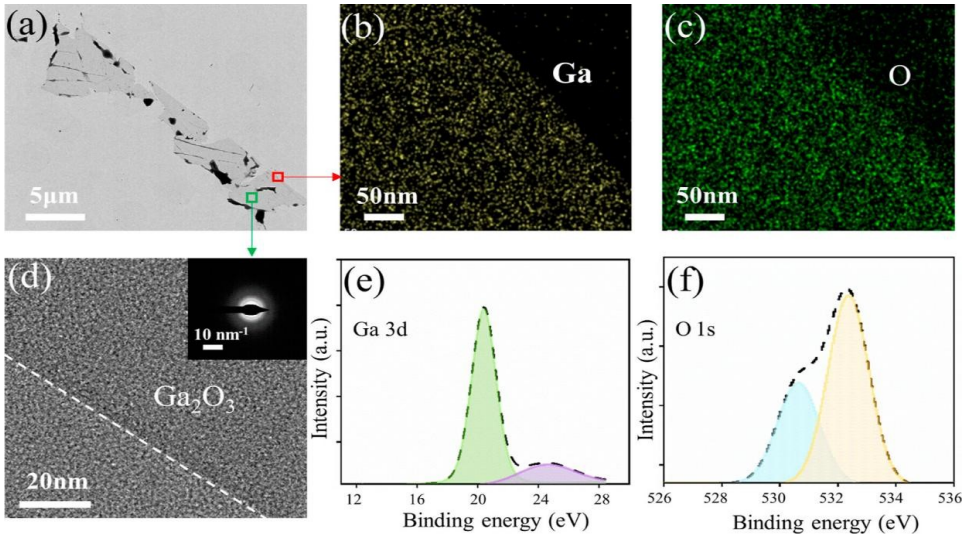


Fig. 10. Structural and chemical characterization of 2D gallium oxide nanosheets. (a) TEM and (b, c) energy-dispersive X-ray spectroscopy (EDS) elemental mapping images of 2D Ga_2O_3 nanosheets. (d) HRTEM image of the Ga_2O_3 nanosheet, the inset was the corresponding selected area electron diffraction (SAED) pattern. (e, f) XPS spectra of the synthesized Ga_2O_3 nanosheets in Ga 3d and O 1s regions. Reproduced with permission from Ref. [74]

Nevertheless, Huang et al.[77] revealed a fundamental limitation of conventional pressure-free LMP, which exclusively yields amorphous Ga_2O_3 with a root-mean-square surface roughness of 1.16 nm at 150 °C, whereas the application of 129 kPa uniaxial pressure enables direct low-temperature crystallization of polycrystalline β-Ga_2O_3 with a reduced roughness of 0.64 nm and near-stoichiometric

Ga/O ratio, as shown in Fig. 11, with both processes producing ~ 3 nm-thick films. Correspondingly, bottom-gate TFTs fabricated from pressure-free amorphous films remain insulating with no field-effect modulation, while those employing PA-LMP-derived polycrystalline channels deliver state-of-the-art low-temperature performance including a saturation mobility of 11.7 $cm^2 \cdot V^{-1} \cdot s^{-1}$, an ON/OFF current ratio of ~ 10^9 and a subthreshold swing of 163 mV/decade, and further enable high-performance NMOS and all-oxide CMOS inverters with a maximum voltage gain of 149 and an ultralow static power consumption of 20 nW for back-end-of-line (BEOL)-compatible circuit integration.

External pressure lowers β-Ga_2O_3 nucleation barriers via nanoconfinement, enabling crystallization and reduced defect density. Pressure-free LMP produced lower surface roughness in the reported memristor structures, whereas pressure-assisted LMP enabled crystallized channels suitable for transistor applications.

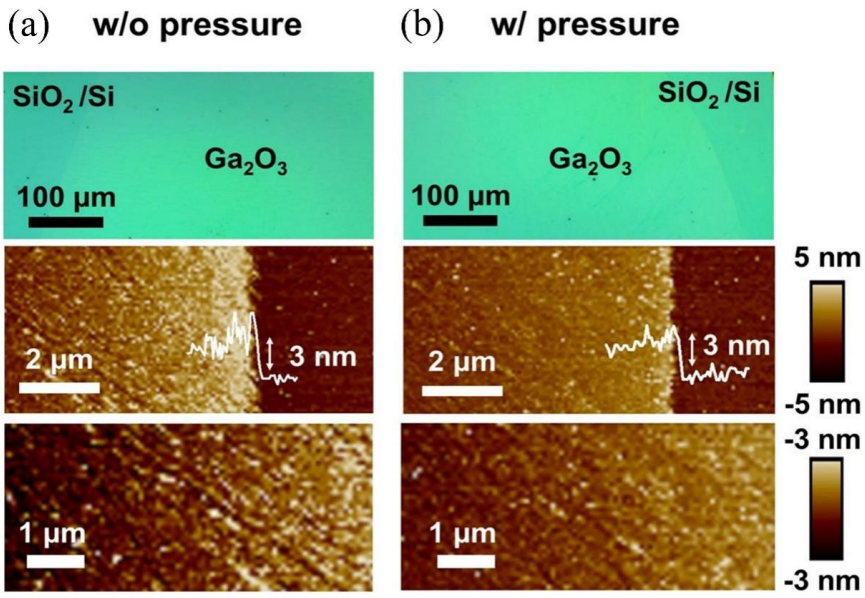


Fig. 11. Optical microscopy image and AFM image (including cross-sectional step-height profile) for the Ga_2O_3 nanosheet were prepared by (a) conventional liquid metal printing (LMP) (without applied printing process pressure) and (b) pressure-assisted liquid metal printing (PA-LMP) methods (applied printing process temperatures (T_p) of 150 °C and printing process pressure (P_p) of 129 kPa). Reproduced with permission from Ref. [77]

In addition, Zhang et al.[78] developed a strategy for centimeter-scale large-area printing: liquid gallium was dropped onto a sapphire substrate, and a motor was then utilized to

control target substrates (e.g., WS_2-modified SiO_2/Si substrates). By squeezing the droplets at 60 °C, large-area fabrication of Ga_2O_3 films was successfully achieved. Kongyang Yi et al.[79] proposed the use of extrusion printing for fabricating small-sized samples, and realized large-area/wafer-scale scalable preparation of Ga_2O_3 films via a surface tension-driven method.

While these direct printing approaches provide relatively simple and scalable routes for Ga_2O_3 transfer, further improvement in transfer controllability and film integrity has motivated the development of polymer-assisted printing and transfer techniques.

4.2 Polydimethylsiloxane-Assisted Blade Scraping and Dry Transfer Techniques

Polydimethylsiloxane (PDMS)-assisted liquid metal printing is a modified process developed on the basis of the direct squeeze-printing method. Its core lies in utilizing the excellent flexibility, tunable adhesion, and chemical inertness of PDMS to achieve nondestructive exfoliation and precise transfer of 2D Ga_2O_3 thin films. Compared with the direct squeeze-printing method, this process is milder, which can effectively avoid film fragmentation and substrate damage caused by mechanical pressure, while significantly reducing residual gallium metal contamination and supporting the construction of atomically clean interfaces. In addition, this method is compatible with both rigid (Si, sapphire) and flexible (PET, PI) substrates, and can conveniently realize the stacking of multilayer van der Waals heterostructures, providing an efficient solution for Si-based Ga_2O_3 hetero-integration and the fabrication of flexible electronic devices. At present, three main process branches have been developed: the PDMS scraping method, the PDMS transfer printing method, and the poly (propylene carbonate) PPC/PDMS composite transfer method.

As the foundational PDMS-assisted technique, PDMS scraping exploits van der Waals interactions between a cured PDMS block and the native oxide skin of liquid gallium to exfoliate and transfer GaO_x films to target substrates. This low-cost, scalable approach enables wafer-scale fabrication with thickness precisely modulated via scraping speed and applied pressure.

Cooke et al.[80] reported the Si-based implementation of this process. Liquid gallium droplets deposited on oxygen-terminated SiO_2/Si substrates were uniformly scraped with PDMS, yielding ultra-large-area (>1 mm^2) amorphous Ga_2O_3 films (2 nm thickness, 0.22 nm RMS roughness) at room temperature. As-deposited films contained 0–8 wt% residual metallic gallium, which was fully oxidized to phase-pure polycrystalline β-Ga_2O_3 via 1000 ℃ air annealing (30 min) without altering film thickness or morphology. Annealed films exhibited characteristic four-band photoluminescence with intensity enhanced by improved crystallinity. MSM photodetectors fabricated from these films demonstrated a dark current of 2.3 nA at 5 V bias and a responsivity of 0.12 A/W at 254 nm, rendering them promising for deep-ultraviolet optoelectronics and high-voltage electronics.

Li et al.[81] developed an alloy-driven liquid metal scraping printing strategy to eliminate metallic residues in pure gallium printing. As shown in Fig. 12, the process involves heating SiO_2/Si substrates, dripping GaInSn eutectic alloy, scraping the self-limiting oxidized 2D Ga_2O_3 skin, and cleaning with warm ethanol. Optical microscopy and AFM confirm the films have good continuity, with a single-step thickness of ~ 4.0 nm and a narrow distribution of 3.6–4.6 nm. In the reported process, the authors estimated an energy reduction of more than 90% relative to the specific CVD process used as the reference. Deep-UV photodetectors exhibit a responsivity of 12.3 A/W at 254 nm, ultrafast 18/22 μs rise/fall times, a detectivity of 2.1×10^{13} Jones, and retain > 90% performance after 1000 bending cycles.

To address film wrinkling and cracking in pure PDMS transfer, the PPC/PDMS composite transfer method incorporates a PPC sacrificial layer, enhancing transfer controllability and film integrity for multilayer stacks and high-precision heterojunctions. Moon et al.[82] developed a liquid gallium extrusion-PPC/PDMS dry-transfer process for high-performance Si-based β-Ga_2O_3 Metal-Insulator-Semiconductor Field-Effect Transistors (MISFETs). As shown in Fig. 13 (a), Raman spectroscopy confirms the crystalline phase of the transferred film, which exhibits characteristic β-Ga_2O_3 phonon modes at A_g^2, A_g^3, A_g^5, and A_g^6 positions. As shown in Fig. 13 (b), atomic force microscopy reveals that single- and bilayer 2D

GaO_x films have uniform thicknesses of ~ 4.5 nm and ~ 8.5 nm, respectively, with atomically flat surfaces. As shown in Fig. 13 (c) and (d), cross-sectional transmission electron microscopy further demonstrates that the amorphous 2D GaO_x forms an atomically sharp, defect-free interface with the underlying β-Ga_2O_3 channel, with no observable interdiffusion. The resulting MISFET with an 8.5-nm-thick bilayer GaO_x gate dielectric delivers a wide gate voltage swing of ~ + 5 V, an on/off current ratio exceeding 10^7 (stable at 250 °C), and a three-terminal breakdown voltage of 138 V, which outperforms non-field-plated β-Ga_2O_3 MESFETs (~ 113 V). It achieves a field-effect mobility of 6.8 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 25 °C (peaking at 7.4 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 150 °C, 4.1 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 250 °C), with negligible threshold voltage temperature dependence and gate leakage < 10^{-6} A at 250 °C, demonstrating the viability of this transfer approach for high-performance Si-integrated β-Ga_2O_3 power devices.

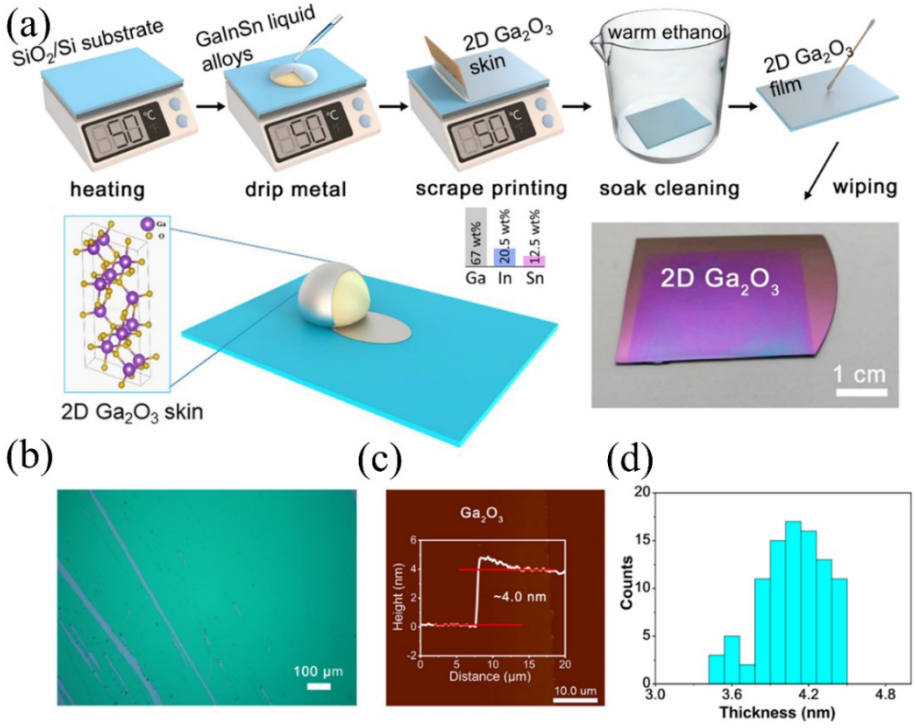


Fig. 12. (a) Schematic description of 2D Ga_2O_3 thin-film preparation from liquid GaInSn through liquid metal nanoprinting process. An optical image of large-area Ga_2O_3 layer on the 2 in. SiO_2 substrate is shown on the bottom right. (b) Optical image of the printed Ga_2O_3 on 300 nm SiO_2/Si. (c) AFM image of Ga_2O_3 film, where the inset was the height profile. (d) Thickness distribution of the printed 2D Ga_2O_3. Reproduced with permission from Ref. [81]

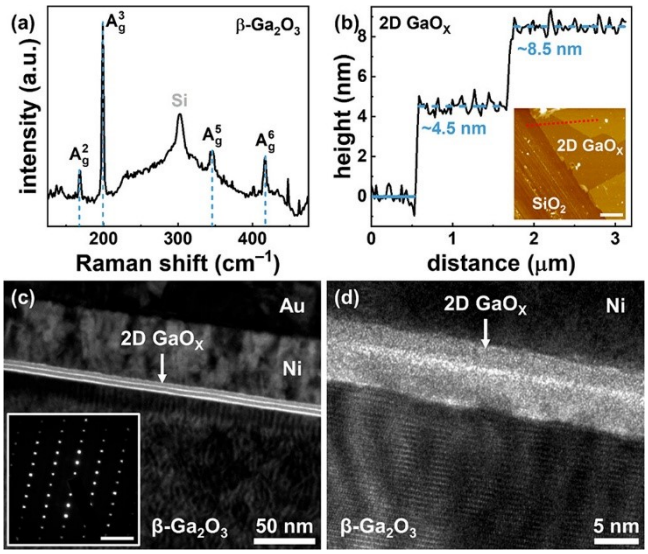


Fig. 13. (a) Raman spectrum of the β-Ga_2O_3 nanolayer of the 2D GaO_x/β-Ga_2O_3 MISFET. (b) AFM height profile of 2D GaO_x monolayer and bilayer. The inset shows an AFM image of the 2D GaO_x on a SiO_2/Si substrate (scale bar: 1 μm). (c, d) Cross-sectional TEM images of the 2D GaO_x/β-Ga_2O_3 MISFET at different magnifications. The inset in (c) shows the SAED pattern of the β-Ga_2O_3 channel (scale bar: 5 nm^{-1}). Reproduced with permission from Ref. [82]

In-situ doping during liquid-metal-based van der Waals printing provides an additional route for tailoring the conductivity and band structure of Ga_2O_3.

P-type doping has long been a critical bottleneck in the field of Ga_2O_3. Li et al.[76] reported Cu-doped p-type Ga_2O_3 films at 250 °C via van der Waals scraping using a Ga-In-Sn-Cu quaternary liquid alloy. Fig. 14 (a) shows sharp, uniform interfaces between the film and SiO_2 substrate, Fig. 14 (b) reveals an ultrasmooth surface morphology with a uniform thickness of approximately 20 nm, corresponding to ten layers. XPS analysis confirms the successful Cu doping and formation of Ga_2O_3. Fig. 14 (c) shows the characteristic Cu $2p_{3/2}$ and Cu $2p_{1/2}$ peaks, while Fig. 14 (d) presents the Ga 2p core-level spectrum consistent with Ga_2O_3. The p-type film has a hole concentration of ~ 3×10^{14} cm^{-3}; field-effect transistors based on it achieve a mobility of 25.5 ± 1.1 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and an on/off ratio of 10^6, and the first fully printed Ga_2O_3 homojunction diode was also realized with a rectification ratio up to 1056.

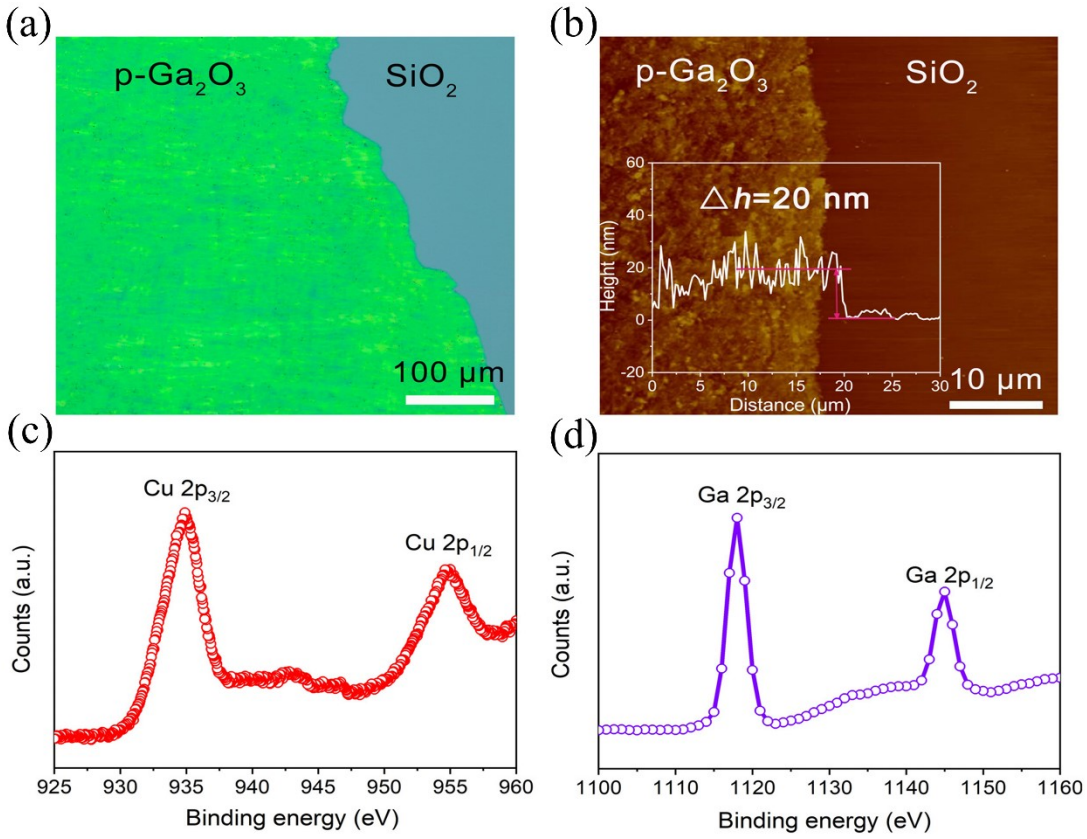


Fig. 14. Characterization of the printed Cu-doped p-type Ga_2O_3 film. (a) Optical image of the printed Cu-doped Ga_2O_3 layer indicating high degrees of homogeneity properties. (b) A standard AFM image of the printed Ga_2O_3 layer with ten prints and the height profile along with the yellow line in the inset. (c) and (d) XPS outcomes of the 2D p- Ga_2O_3 for the areas of interest, Cu 2p, and Ga 2p. (c) The characteristic doublets for the Cu 2p area, $2p_{1/2}$ and $2p_{3/2}$, are located at ~ 935.2 and ~ 954.8 eV. (d) The characteristic doublets for the Ga 2p area, $2p_{1/2}$ and $2p_{3/2}$, are at ~ 1144.8 and ~ 1118.1 eV, respectively. Reproduced with permission from Ref. [76]

Huang et al.[83] successfully prepared Bi-doped Ga_2O_3 thin films using Bi-Ga binary alloys with varying Bi contents, achieving continuous tunability of the bandgap. As the Bi content in the liquid alloy increases from 0 wt% to 15 wt%, the atomic percentage of Bi^{3+} in the thin film increases linearly from 0% to 6.7%, and the corresponding optical bandgap narrows continuously from 5.23 eV to 4.88 eV, while the work function decreases from 5.69 eV to 5.24 eV. This bandgap modulation originates from the lower bandgap and work function of Bi_2O_3; Bi atoms introduce impurity levels in the forbidden band and cause lattice distortion after incorporation into the Ga_2O_3 lattice. For the photodetector based on the film printed from the 15 wt% Bi–Ga alloy, a

responsivity of 959 mA/W, a calculated detectivity of 3.43×10^{11} Jones, and an EQE of 433% were obtained under 275 nm illumination at an incident intensity of 0.8 mW/cm^2 and a bias of 6 V, together with response/recovery times of 13/18 ms. The EQE exceeding 100% indicates the presence of internal photoresponse gain, although the specific microscopic gain mechanism was not further established in the original study. These results demonstrate competitive deep-UV photodetection performance under the reported measurement conditions.

Table 3. Comparison of key parameters and device demonstrations of Ga_2O_3 films fabricated via various printing/transfer strategies.

Study	Printing Method	Maximum Printed Area	Key Thin Film Properties	Fabricated Device Type
Xu et al. [74]	Direct Squeeze Printing	2-inch wafer-scale	Thickness ~ 3 nm, RMS = 0.160 nm.	Pt/Ga_2O_3/n^+-Si memristor
Huang et al. [77]	Pressure-Assisted LMP	1 × 1 cm^2	Thickness ~ 3 nm, RMS = 0.64 nm.	Bottom-gate TFTs, NMOS/CMOS inverters
Zhang et al. [78]	Centimeter-Scale Large-Area Squeeze Printing	Centimeter-scale (~ 1 cm^2)	Thickness ~ 1.2–3 nm, RMS ~ 0.4 nm.	WS_2 top-gate dual-gate transistors
Cooke et al.[80]	PDMS Scraping +High-Temperature Annealing	> 1 mm^2	As-deposited: ~ 2 nm thick, RMS roughness 0.22 nm, amorphous, after annealing: fully converted to pure polycrystalline β-Ga_2O_3,	MSM solar-blind UV photodetectors

Study	Printing Method	Maximum Printed Area	Key Thin Film Properties	Fabricated Device Type
Li et al. [81]	GaInSn Alloy-Driven PDMS Scraping	2-inch wafer-scale	Thickness ~ 4.0 nm, RMS ~ 0.16 nm.	Vertical-structure ITO/quasi-2D Ga_2O_3 solar-blind UV photodetectors
Moon et al. [82]	PPC/PDMS Composite Dry Transfer	Millimeter-scale large area	Monolayer ~ 4.5 nm, bilayer ~ 8.5 nm, RMS ~ 0.4–0.7 nm.	β-Ga_2O_3 top-gate MISFET
Li et al. [76]	In-Situ Cu-Doped LMP	Millimeter-scale large area	Thickness ~ 20 nm (10 layers).	p-type Ga_2O_3 FETs; all-printed Ga_2O_3 p-n homojunction diodes
Huang et al. [83]	In-Situ Bi-Doped LMP	Millimeter-scale large area	Thickness: ~ 2.0 nm (0% Bi), ~ 2.4 nm (1% Bi), ~ 2.7 nm (10% Bi), ~ 3.0 nm (15% Bi).	Ag interdigital 275 nm deep-UV photodetectors

In summary, a diverse range of LMP strategies has been developed for fabricating Si-based Ga2O3 thin films. As shown in Table 3, direct squeeze-printing, pressure-assisted LMP, PDMS-assisted scraping, PPC/PDMS composite transfer, and in-situ doping printing enable large-area preparation from millimeter-scale to 2-inch wafer-scale. The obtained films feature a thickness of 2–20 nm and a minimum surface roughness of 0.16 nm, with tunable amorphous and polycrystalline β-phase. Based on LMP, memristors, bottom-gate TFTs, CMOS inverters, deep-UV photodetectors, MISFETs, p-type FETs, and Ga_2O_3 homojunction diodes have been successfully demonstrated. Furthermore, in-situ Cu and Bi doping realize p-type conductivity and bandgap tuning.-Despite these advances, LMP still faces notable limitations. As-printed Ga_2O_3 films are typically amorphous and require post-annealing for crystallization,[84]

adding process complexity and thermal budget. Residual metallic gallium (up to 8 wt%) can persist in printed films, introducing unintended impurities.[80] Thus, while LMP provides a low-temperature integration route that largely circumvents the lattice-matching constraints of conventional heteroepitaxy, its limitations in crystallinity, thickness control, wafer-scale uniformity, residual metallic species, and process reproducibility indicate that it should presently be regarded as complementary to, not a replacement for, conventional epitaxial growth.

5. Conclusion

Heterogeneous integration of Ga_2O_3 with silicon has emerged as a promising route toward low-cost, large-area ultrawide-bandgap electronic and optoelectronic systems by combining the attractive material properties of Ga_2O_3 with the mature and scalable manufacturing platform of Si. Within conventional heteroepitaxial routes, surface pretreatment and buffer-layer engineering using materials such as AlN, 3C-SiC, and TiN can mitigate interfacial incompatibility, lattice mismatch, and growth-induced stress, thereby improving film quality and device performance. In parallel, liquid metal printing provides a distinct non-epitaxial integration route based on van der Waals transfer, relaxing the strict lattice-matching requirement of conventional heteroepitaxy and enabling low-temperature integration of ultrathin Ga_2O_3 with Si-based substrates. These two approaches should therefore be viewed as complementary rather than directly interchangeable, reflecting their distinct growth or integration mechanisms and application scopes. Further progress will require route-specific optimization, including improved interface and defect control for heteroepitaxial growth and enhanced crystallinity, thickness control, uniformity, and reproducibility for liquid-metal-printing-based integration.

Despite this progress, successful practical deployment still faces several key challenges, including the lack of standardized protocols for interfacial oxide removal, insufficient long-term stability and thermal management data for Ga_2O_3/Si heterostructures, and regulatory uncertainty in adopting new wide-bandgap materials into established semiconductor foundries. Future research should prioritize (i) buffer layer engineering

and surface pretreatment to further reduce interface defect density; (ii) hybrid integration strategies combining conventional epitaxial growth with liquid-metal-printing-based transfer; (iii) standardized, foundry-compatible processing and wafer-scale reproducibility; (iv) sustainable, low-temperature synthesis methods such as pressure-assisted LMP; (v) multifunctional monolithic integration platforms integrating power devices and on-chip sensing functions; (vi) computational modeling, such as Density Functional Theory (DFT), Technology Computer-Aided Design (TCAD) to predict strain, defect evolution, and thermal transport; and (vii) advanced in-situ and 3D characterization to monitor real-time nucleation and interface formation. Through interdisciplinary collaboration, rigorous material assessment, and harmonized industrial guidelines, Si-based Ga_2O_3 technologies can progress from laboratory research to commercially viable, high-performance power electronics and deep-UV optoelectronic devices that are both cost-effective and reliable.

Declaration of Competing Interests:

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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