An Integrated Broadband Low-Noise Microwave Source for Superconducting Quantum Circuits

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Scaling superconducting quantum processors increasingly relies on custom control electronics that can simultaneously satisfy spectral purity, multi-channel isolation, and long-term stability within a compact and integrated platform. Here we present Quantum microwave source (QMW), a classical three-channel broadband low-noise microwave source that consolidates qubit XY drive, readout excitation, and Josephson parametric amplifier (JPA) pump generation onto a single hardware module operating from 4 to 14 GHz with an output power range of −20 to +10 dBm. Electronic characterization yields a spurious-free dynamic range greater than 55 dB, equivalently a largest spur below −55 dBc, a phase noise as low as −110 dBc/Hz at 10 kHz offset for a 5 GHz carrier and below −103 dBc/Hz at the same offset across the full band, and output power stability within 0.1 dB over 24 hours. Integrated into the control chain of a 36-qubit superconducting processor, QMW pumps a JPA to 19.2 dB gain to enable high-SNR single-shot readout, while sustaining qubit coherence times of $T_1 = 60.1 \pm 0.8$ μs, $T_{2,\mathrm{Ramsey}} = 24.2 \pm 1.5$ μs, and $T_{2,\mathrm{echo}} = 58.6 \pm 2.1$ μs, and an average single-qubit gate fidelity of $99.95 \pm 0.05\%$ measured by randomized benchmarking. The compact and modular nature of QMW provides a scalable microwave generation solution for large-scale superconducting quantum processors, with potential extensions to other quantum hardware platforms and precision measurement applications.

Keywords: Superconducting quantum circuits, Superconducting qubit, Low noise microwave source

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I. INTRODUCTION

Superconducting quantum processors have rapidly advanced to hundreds of qubits [1–7], reaching a stage where system performance is increasingly limited not only by intrinsic qubit decoherence, but also by the classical control electronics that generate and deliver microwave signals for qubit manipulation and readout [8–12]. In particular, achieving high-fidelity quantum operations at scale demands microwave signals with low phase noise, high spectral purity, and precise amplitude stability, while simultaneously imposing stringent requirements on timing synchronization, channel uniformity, and multi-channel isolation [10, 11, 13–17].

Conventional control architectures based on discrete commercial instruments face inherent limitations in integration density, scalability, and multi-channel synchronization, which become increasingly severe as the number of qubits grows [14, 17–19]. Among the various control subsystems, high-quality microwave sources serving as local oscillators (LO) play a central role in both superheterodyne [13, 14, 16, 20] and direct-RF architectures [10, 21, 22], providing carrier references for qubit drive and readout signal synthesis as well as stable clock references for high-speed data converters. Due to bandwidth limitations of current data converters, external LOs remain necessary to cover the typical 4–8 GHz qubit operating range for drive and readout signal generation. Furthermore, quantum-limited amplification based on JPAs typically requires pump tones at approximately twice the signal frequency [23], extending the required microwave coverage beyond 12 GHz. The spectral purity and phase noise of these LO sources directly affect qubit dephasing, gate fidelity, and the operational stability of auxiliary devices such as the JPA [11, 24–26].

Existing microwave generation approaches are primarily based on traditional analog architectures [27] or integrated phase-locked loop (PLL) synthesis [28–30]. Analog solutions provide low phase noise but suffer from large footprint, limited integration, and slow frequency switching. PLL-based synthesis improves integration and switching speed, but often involves trade-offs between wideband coverage and spectral purity. Moreover, without careful isolation design, PLL-based sources are susceptible to digital noise and crosstalk in high-density

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multi-channel configurations [16, 31].

To address these challenges, we present Quantum microwave source (QMW), a classical microwave source dedicated to the microwave control of superconducting quantum circuits and optimized for the integration density, noise, stability, and synchronization requirements of quantum control. By consolidating qubit drive, readout, and JPA pump functionalities into a unified hardware platform, QMW achieves high integration density while maintaining low-noise, high-stability performance across 4–14 GHz. The architecture employs split-band filtering to suppress harmonic spurs and incorporates a high-precision digital attenuation chain, enabling a linear output power range of −20 to +10 dBm with 0.5 dB resolution and long-term power stability within 0.1 dB. Electronic characterization confirms reliable RF performance across the full bandwidth: the spurious-free dynamic range (SFDR) is greater than 55 dB; the single-sideband phase noise reaches −110 dBc/Hz at a 10 kHz offset for a 5 GHz carrier and remains below −103 dBc/Hz at the same offset across the full 4–14 GHz band; the channel-to-channel crosstalk is below −42 dB; and the frequency-switching times are 2 ms and 9 ms. Key specifications are summarized in Table I. A comparison of key metrics of QMW with three commercial microwave sources is given in Table II. Validation on a 36-qubit processor demonstrates that QMW meets the requirements of intermediate-scale quantum systems, with measured qubit coherence times and single-qubit gate fidelities consistent with high-fidelity quantum operations. The main advance is the architecture and the integration: three broadband, spectrally clean, phase-synchronized output channels covering both the qubit and the JPA pump bands within one compact low-power module.

TABLE I. **Overview of key metrics of QMW.**

Performance	Value
Output channels	3
Output frequency	4–14 GHz
Minimum frequency step	100 kHz
Output power	−20 to +10 dBm
Minimum power step	0.5 dB
Power flatness	< 0.3 dB
Long-term power stability	< 0.1 dB (over 24 hours)
SFDR	> 55 dB
Phase noise at 10 kHz	−110 dBc/Hz at 5 GHz, best case −103 dBc/Hz at 13 GHz, worst case
Frequency-switching time	< 9 ms
Channel-to-channel crosstalk	< −42 dB
Single-channel power consumption	30 W

II. ELECTRONIC DESIGN AND PERFORMANCE

The hardware architecture of the QMW system, as illustrated in Fig. 1(a), comprises four primary functional blocks: a PLL-based microwave signal module with RF front-ends, a digital control module driven by a microcontroller (MCU), a power management module employing a low-dropout regulator (LDO), and a high-stability clock distribution module. To meet the stringent low-noise and high-isolation demands of superconducting quantum circuits, a strict ground plane partitioning strategy is implemented in the printed circuit board (PCB) design to suppress power supply noise and digital crosstalk. Accordingly, the system is physically segregated into a digital control board and an RF board based on reference ground potentials, as shown in Fig. 1(b). In the prototype assembly, the digital control board (280×130 mm^2) hosts the power management and digital control circuitry, while the RF board (220×200 mm^2) integrates the microwave signal generation and clock distribution modules. Inter-board power delivery and digital communication are established via DC harnesses and ribbon cables, respectively.

The digital control module coordinates system operations, executing instruction parsing, sequence scheduling, and system state monitoring. Based on an embedded MCU, it integrates universal asynchronous receiver-transmitter (UART), serial peripheral interface (SPI), and general-purpose input/output (GPIO) interfaces to coordinate distributed functional blocks. For external connectivity, the system incorporates a UART interface for remote host control and a local keypad for manual operation, ensuring operational flexibility and efficient debugging across diverse experimental setups. Regarding the underlying hardware control architecture, a dual-channel SPI topology is implemented to ensure real-time data throughput. The first channel (SPI 1) is dedicated to configuring PLL registers, facilitating rapid frequency synthesis and locking. The second channel (SPI 2) drives the liquid crystal display (LCD) for parameter updates, enabling simultaneous command execution and status visualization. Additionally, GPIO ports provide logic-level control for RF switches and the digital step attenuator (DSA). Through this architecture, the MCU translates user commands into digital signals, governing the frequency and power of the broadband microwave output.

To optimize power integrity, the system employs a strict power plane partitioning strategy, separating digital and analog domains. Front-end isolation is achieved via two independent DC-DC converter modules, establishing dedicated power and ground planes for each domain. Furthermore, a rigorous power budget analysis is conducted for individual load paths. Power components are selected to ensure sufficient operating headroom, thereby guaranteeing high-efficiency DC-DC conversion and effective thermal management across the system, resulting in an average power consumption of 30 W per channel.

For the analog supply, a two-stage noise suppression architecture is implemented. The first stage utilizes a high-efficiency DC-DC converter to step down the +12 V input to an intermediate bus voltage, while the second stage employs LDO regulators for precision regulation, delivering stable power to ripple-sensitive components. This hybrid configuration balances conversion efficiency with noise suppression, mitigating the excessive thermal dissipation associated with large voltage drops in single-

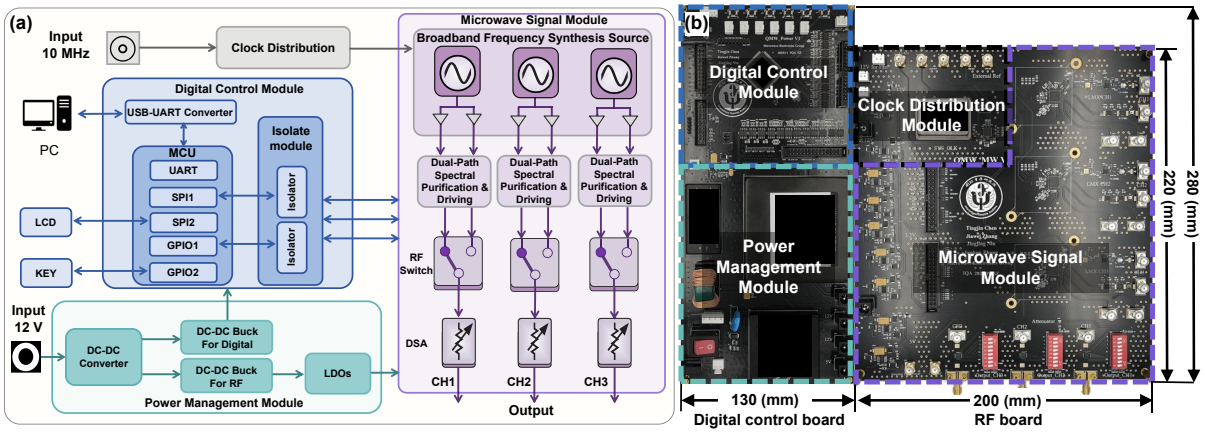


FIG. 1. **System architecture of QMW**. (a) Functional block diagram of the hardware, comprising the microwave signal module, digital control module, power management module, and clock distribution module. (b) Photograph of the prototype, with the same four modules indicated on the digital control board (280×130 mm^2) and RF board (220×200 mm^2).

stage linear regulation. The core analog rail employs Analog Devices LT3045 [32], offering a power supply rejection ratio exceeding 90 dB at 1 kHz and low root mean square (RMS) noise of 0.8 μV_{RMS}. This ensures a stable supply rail for the noise-sensitive RF blocks. Furthermore, to meet the high output current requirements of the multi-channel design, a parallel LDO topology is adopted. This configuration extends the maximum drive current to 4.5 A while further reducing the noise floor by averaging uncorrelated noise sources.

The spectral purity and phase stability of microwave drive and readout signals are critical for achieving high-fidelity superconducting quantum operations. These metrics depend on the quality of the system's reference clock. To ensure high output stability and minimize phase noise, we develop a clock distribution module based on a low-additive-jitter architecture [24]. The reference configuration offers flexibility, supporting both internal oscillators and external inputs. The internal path utilizes a high-stability oven-controlled crystal oscillator [33]. With a frequency stability better than ± 3 ppb and a single-sideband phase noise of -140 dBc/Hz at a 100 Hz offset, it establishes a low-noise baseline. To satisfy the stringent global phase coherence requirements of cascaded measurement architectures, the module is also compatible with external high-precision atomic clocks.

A clock multiplexing unit at the input stage enables switching between internal and external reference sources. To maintain signal integrity, external references are coupled via SMA interfaces with 50 Ω impedance matching, suppressing reflection-induced spurious components. Subsequently, single-ended inputs are converted into the low-voltage differential signaling (LVDS) format, mitigating common-mode noise and timing jitter during board-level transmission. The clock distribution minimizes additive noise using a TI LMK series ultralow-noise clock buffer, with a noise floor of -164 dBc/Hz and additive jitter below 60 fs at a 156.25 MHz carrier. At the physical layer, the PCB layout strictly implements differential trace length matching and controlled impedance to minimize transmission skew and signal reflections. These design measures ensure the delivery of phase-synchronized, low-jitter reference clocks to the three output channels, providing a reliable timing reference for high-fidelity microwave synthesis.

The phase noise of the microwave source directly limits qubit coherence: excessive phase noise exacerbates qubit pure dephasing, thereby limiting the transverse coherence time [11]. To minimize phase noise while maintaining broad frequency coverage, the core frequency generation unit employs the Texas Instruments LMX2820 wideband PLL synthesizer [34], which spans up to 22 GHz with a flicker noise figure of merit of -134 dBc/Hz and a wideband noise floor figure of merit of -236 dBc/Hz. As illustrated in Fig. 2(a), the synthesizer operates in a fractional-N PLL topology referenced to a stable 10 MHz clock (f_{ref}). The phase-frequency detector (PFD) compares the divided reference signal with the VCO feedback signal; the resulting phase error is filtered by a loop filter to suppress out-of-band noise and lock the VCO to the target frequency. The VCO output is then divided by a programmable output divider to generate the desired microwave signal. The output frequency is determined by the following relation [34]:

$$f_{\mathrm{RF}} = f_{\mathrm{ref}} \cdot \underbrace{\left(\frac{M}{D}\right)}_{\text{Ref. Path}} \cdot \underbrace{(N_{\mathrm{int}} + N_{\mathrm{fra}})}_{\text{N-Divider}} \cdot K_{\mathrm{out}}, \qquad (1)$$

where f_{RF} denotes the final output frequency. The reference input f_{ref} is first conditioned by a programmable multiplier M and divider D in the reference path, then compared with the VCO feedback signal at the PFD. The feedback path employs an N-divider comprising an integer part N_{int} and a fractional part N_{fra}, enabling fine frequency resolution. The VCO output is scaled to the target frequency through the output factor K_{out}, which operates in three modes: a doubler mode ($K_{\mathrm{out}} = 2$)

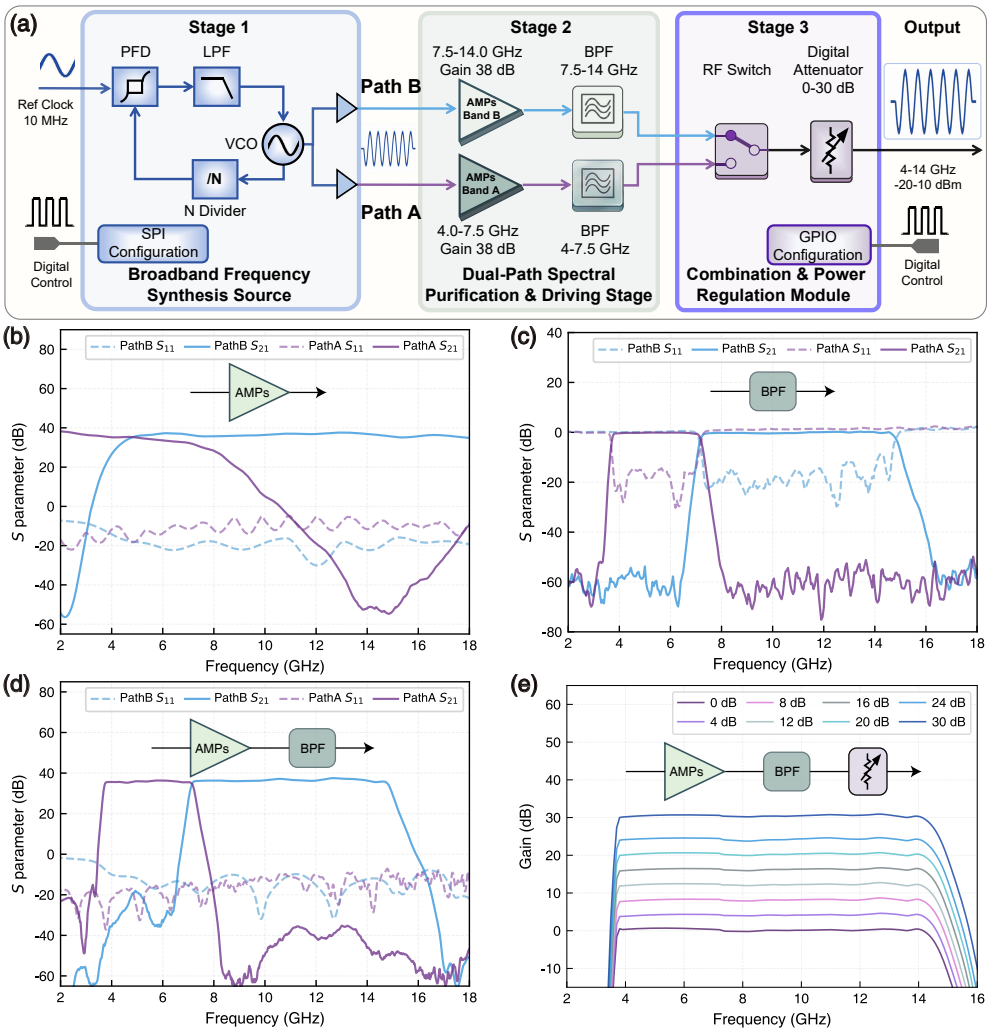


FIG. 2. **Configuration of the microwave signal module components.** (a) Schematic diagram of the microwave signal module architecture. The system comprises a broadband frequency synthesis source, a dual-path spectral purification and driving stage, and a signal combination and power regulation module. The blue shaded region represents the broadband frequency synthesis source; the green region corresponds to the dual-path spectral purification and driving stage; and the purple region highlights the combination and power regulation module. (b) S-parameter characterization of the dual-path amplification chain. Utilizing a cascaded amplification topology, both paths achieve a flat gain greater than 38 dB within their respective passbands. (c) S-parameter measurements of the filtering networks. The low-frequency and high-frequency paths define passbands of 4–7.5 GHz and 7.5–14 GHz, respectively. Both paths exhibit out-of-band rejection better than 40 dB and insertion loss below 2 dB. (d) Overall transmission characteristics of the dual-path spectral purification and driving stage. Across the full 4–14 GHz band, the gain in both passbands is better than 38 dB, with out-of-band rejection better than 40 dB. The insertion loss below 2 dB refers to the filtering networks in (c). (e) Output power calibration via the digital step attenuator. By sweeping the DSA setting from 0 to 30 dB attenuation in 0.5 dB steps, the module delivers a linear output power range of -20 to $+10$ dBm at the output channel.

for frequencies above 11.3 GHz, a fundamental mode ($K_{\text{out}} = 1$) covering the 5.65–11.3 GHz range, and a divider mode ($K_{\text{out}} < 1$) for extending coverage below the VCO fundamental range when required. This architecture enables complete frequency coverage of the superconducting qubit measurement and control band. The fractional-N synthesis approach provides high-precision frequency tuning: by appropriately configuring N_{fra}, sub-kHz frequency resolution can be achieved in principle. However, excessively fine frequency steps introduce severe fractional spurs near integer boundaries, degrading phase noise performance [34]. To balance spectral purity with frequency agility for high-fidelity quantum gate operations, the system is configured with a minimum programmable frequency step of 100 kHz.

Qubit control and readout performance depend critically on the spectral purity and power stability of the microwave drive signals. High-order harmonics and spurious components in the drive signal can induce unintended transitions between qubit energy levels [11]. Fur-

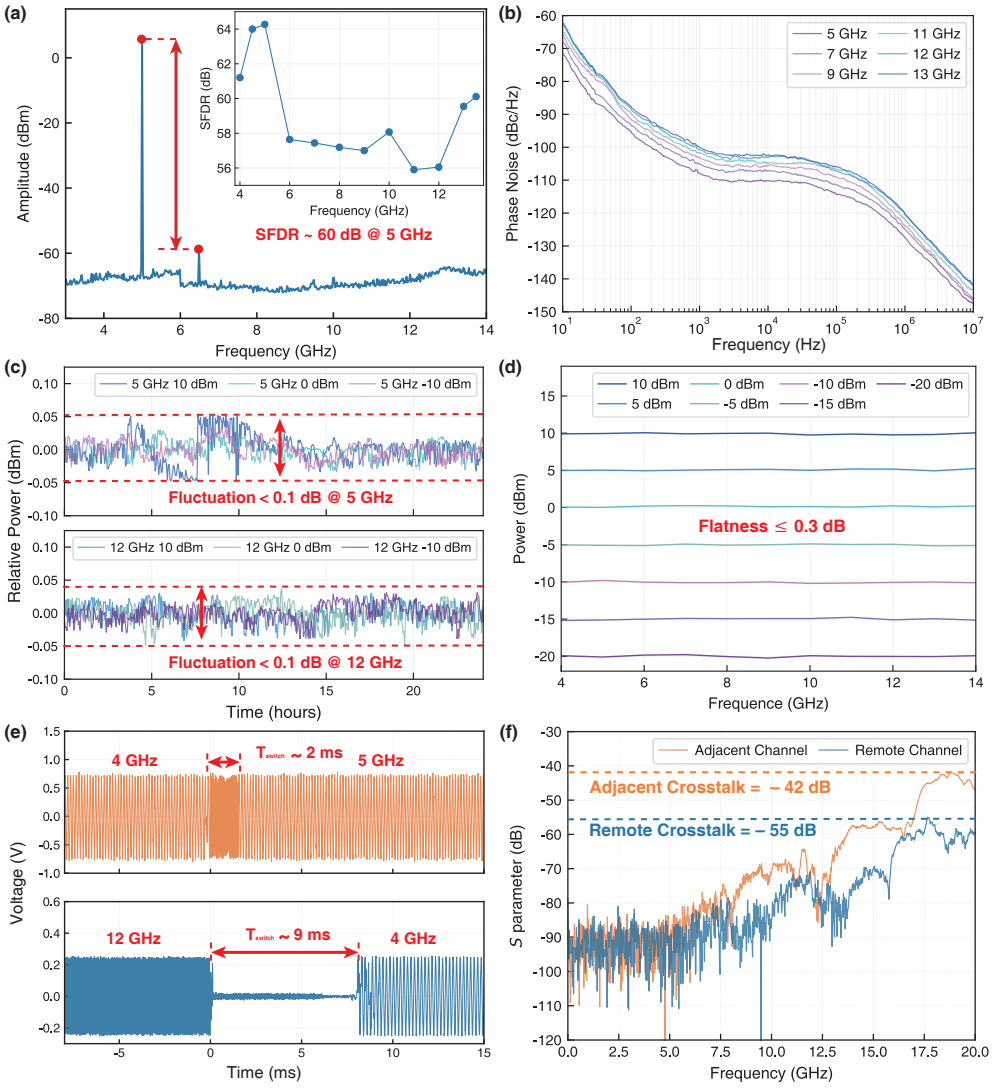


FIG. 3. **Electronic performance.** (a) Output spectrum and SFDR characterization, where an SFDR of 60 dB, corresponding to a largest spur at −60 dBc, is measured for a 5 GHz output signal. Inset: SFDR over the entire bandwidth of 4–14 GHz, remaining better than 55 dB, equivalently a largest spur below −55 dBc. (b) Phase noise for different output frequencies. The phase noise reaches −110 dBc/Hz at a 10 kHz offset for a 5 GHz carrier and remains below −103 dBc/Hz at the same offset across the full 4–14 GHz band, with the worst case at 13 GHz, under nominal operating conditions of room temperature, internal OCXO reference, and 0 dBm output. (c) Long-term stability test at different power levels, where the output power at typical frequencies of 5 GHz and 12 GHz is set to −10 dBm, 0 dBm, and +10 dBm, showing a peak-to-peak power fluctuation of less than 0.1 dB over 24 hours. (d) Output power flatness and linearity, measured by sweeping the 4–14 GHz band in 100 MHz steps, that is at 101 frequency points, with 7 output-power settings at each point; the power variation remains within 0.3 dB over the full band. (e) Frequency switching time test, showing a switching time of 2 ms from 4 GHz to 5 GHz, and 9 ms from 12 GHz to 4 GHz. (f) Channel-to-channel crosstalk measurement, showing an S_{21} below −42 dB between adjacent channels and below −55 dB between remote channels.

thermore, amplitude fluctuations in the readout excitation can degrade the signal-to-noise ratio (SNR), consequently lowering the qubit readout fidelity [35–37]. In practice, direct outputs from broadband frequency synthesizers inherently contain such spectral impurities, including digital spurs, power supply noise, and reference clock feedthrough. Additionally, the limited and nonlinear power range of the raw output does not meet the amplitude precision required for high-fidelity gate operations. To address these challenges, the system implements a dual-path spectral purification and driving stage with a precision power control module, as illustrated in Fig. 2(a).

To suppress harmonic spurs, the system employs a split-band processing architecture. Covering the 4–14 GHz frequency range required for superconducting quantum control, the signal path is divided into a low-frequency path spanning 4–7.5 GHz and a high-frequency

path covering 7.5–14 GHz, labeled A and B in Fig. 2(a). This partitioning ensures that the second-order harmonic of any tone within a given sub-band falls above the upper cutoff of that sub-band, preventing in-band second-harmonic interference within each path. Residual higher-order harmonics are subsequently suppressed by the LTCC filtering networks. In terms of amplification, both paths use a cascaded topology, with measured S-parameters presented in Fig. 2(b). For the low-frequency path, a Mini-Circuits CMA series low-noise amplifier (LNA) is cascaded with a power amplifier (PA) [38]; this configuration yields a noise figure (NF) below 1.5 dB while delivering a saturated output power exceeding 30 dBm. For the high-frequency path, a two-stage cascade of PMA series LNAs [38] is adopted, achieving a gain greater than 38 dB across the 7.5–14 GHz range, with a cascaded NF below 1.5 dB. Measurement results confirm that both paths achieve a flat gain greater than 38 dB within their respective passbands.

To enhance the spectral purity of the output signal, the filtering network is implemented using low-temperature co-fired ceramic (LTCC) technology; its S-parameter response is illustrated in Fig. 2(c). In the low-frequency path, an LFCN series low-pass filter and a BFCN series band-pass filter (BPF) [39] are cascaded to define the 4–7.5 GHz frequency band. The high-frequency path uses the BFCQ series BPF [39] to define the 7.5–14 GHz high-frequency band. Both filtering paths attain out-of-band rejection better than 40 dB and exhibit passband insertion loss below 2 dB. The overall transmission characteristics of the cascaded dual-path amplification and filtering chains are illustrated in Fig. 2(d). The system exhibits two high-gain passbands with out-of-band rejection better than 40 dB across the entire 4–14 GHz measurement and control frequency range.

Subsequently, the RF signals processed by the dual-path chains are routed to a high-isolation, low-insertion-loss microwave switch. This component maintains an insertion loss below 0.4 dB and an isolation better than 60 dB across the DC–18 GHz bandwidth. The control system dynamically activates the appropriate path based on the target frequency, employing switching logic to achieve frequency-selective signal routing while physically isolating noise feedthrough from inactive bands. Final power regulation is performed by a Peregrine Semiconductor PE43610 DSA [40]. Featuring a fine step size of 0.5 dB, this component provides a linear power adjustment range of -20 to $+10$ dBm as shown in Fig. 2(e), satisfying the amplitude precision requirements for superconducting qubit drive signals.

To comprehensively evaluate the electronic performance of the QMW, systematic characterization is conducted on key metrics, including SFDR, phase noise, power stability, power flatness, frequency switching time, and channel crosstalk. Spectral purity is characterized using a Rohde & Schwarz FSL spectrum analyzer. At a representative output frequency of 5 GHz, the measured SFDR is 60 dB, corresponding to a largest spur at -60 dBc. As shown in Fig. 3(a), the SFDR remains better than 55 dB across the entire 4–14 GHz operating band, indicating effective suppression of spurious components and harmonics.

Single-sideband phase noise is measured with a Rohde & Schwarz phase noise analyzer. Measurement results across the full operating band are presented in Fig. 3(b). At 5 GHz, the phase noise is as low as -110 dBc/Hz at a 10 kHz offset. Across the full 4–14 GHz band, the phase noise remains below -103 dBc/Hz at the same offset, with the worst case at 13 GHz. All values are measured at room temperature with the internal OCXO reference and 0 dBm output. By integrating the phase noise spectrum from 10 Hz to 10 MHz, the RMS timing jitter is calculated to be 65 fs, indicating low-jitter clock performance across the measured offset frequency range.

The output power stability and flatness are further evaluated using the FSL spectrum analyzer. Long-term stability measurements are performed at 5 GHz and 12 GHz for output powers of -10, 0, and $+10$ dBm. As shown in Fig. 3(c), the power fluctuation remains within 0.1 dB over 24 hours for all tested conditions. For flatness characterization, the QMW is swept across the 4–14 GHz band with a frequency step of 100 MHz. The measured power variation remains within 0.3 dB over the full bandwidth, as shown in Fig. 3(d), confirming stable amplitude performance across the operating range. The dynamic response capability of the system is characterized through frequency-switching measurements using a Tektronix DPO72004 high-speed oscilloscope, to which the output channel under test was directly connected. As shown in Fig. 3(e), for a frequency hop from 4 GHz to 5 GHz, the settling time is measured to be 2 ms. A larger transition from 12 GHz to 4 GHz requires 9 ms, demonstrating rapid and stable frequency reconfiguration. Channel-to-channel crosstalk is characterized using a Rohde & Schwarz ZNB vector network analyzer by measuring inter-channel transmission coefficients across the DC–20 GHz range. As shown in Fig. 3(f), the crosstalk is below -42 dB between adjacent channels and below -55 dB between remote channels, ensuring low inter-channel interference in multi-channel operation.

Deterministic phase synchronization of the three output channels is implemented by the trigger distribution architecture in Fig. 4(a). The MCU trigger enters a trigger distribution unit that fans it out over length-matched traces to the three output channels and provides three external trigger outputs and one external trigger input for multi-module operation. The distributed trigger drives the phase-synchronization input (PSYNC) of the LMX2820 synthesizers, resetting the MASH modulator and the feedback divider of each PLL, so that the output phase of every channel is tied to the trigger instant. The residual fixed offset between channels is removed by digital skew calibration, which shifts the output phase of each synthesizer by programming the seed of its MASH modulator. The two functions together allow the same relative phase to be recovered after each power-up and

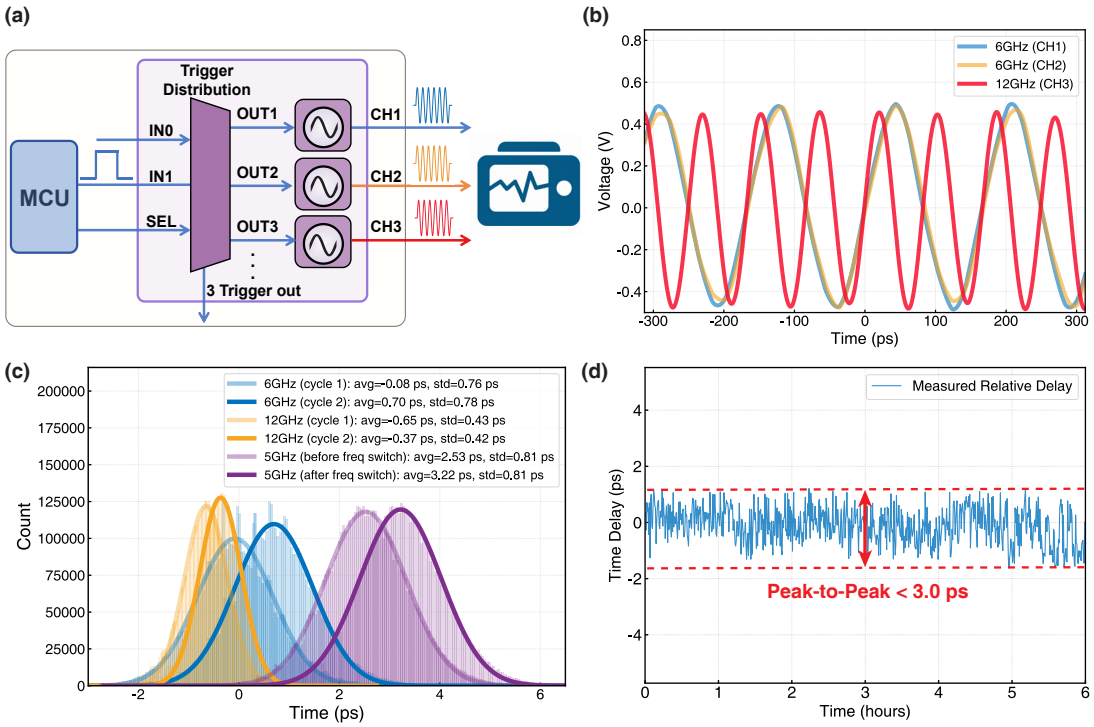


FIG. 4. **Deterministic inter-channel phase synchronization.** (a) Trigger distribution. The trigger issued by the MCU is fanned out to the three output channels over length-matched traces; three external trigger outputs and one external trigger input allow several modules to be referred to the same synchronization event. (b) Persistence-mode waveforms of the three output channels operating simultaneously: CH1 and CH2 at 6 GHz, and CH3 at 12 GHz. (c) Distributions of the relative time delay between two output channels, recorded before and after a power cycle at 6 and 12 GHz, and at 5 GHz before and after an excursion to 12 GHz and back. The width of each distribution is the scatter of a single measurement; the mean shifts by less than 0.8 ps in every case. (d) Relative time delay under simultaneous full-power operation at 6 GHz, drifting by 0.63 ps with a peak-to-peak variation below 3.0 ps over 6 hours.

after each frequency change.

The three output channels are of identical design and are aligned by the same trigger, so they are equivalent with respect to synchronization. The quantitative results below were recorded for a representative pair, connected to two channels of a Tektronix DPO72004 oscilloscope through equal-length cables. The relative time delay was obtained with the skew measurement of the DPOJET jitter and timing analysis package. A single skew measurement has a standard deviation between 0.4 and 0.8 ps depending on the carrier frequency, and each value reported below is the mean of about 5×10^6 skew measurements, so that the statistical uncertainty of the mean is below 1 fs. The quantities reported are changes of the relative time delay, for which the static skew of the cables and of the oscilloscope is common to the two states and cancels; these values are therefore an upper bound on the contribution of the module.

Simultaneous operation of the three output channels, with CH1 and CH2 at 6 GHz and CH3 at 12 GHz, is shown in Fig. 4(b). Under power cycling, frequency switching, and long-term simultaneous operation, as shown in Figs. 4(c) and (d), the mean relative time delay between two output channels is displaced by 0.78 ps at 6 GHz and by 0.28 ps at 12 GHz between independent power-up events, and by 0.69 ps at 5 GHz across a frequency excursion to 12 GHz and back, with the measured delay changes corresponding to carrier-phase variations of no more than 1.7° across the tested conditions. Under simultaneous full-power operation at 6 GHz it drifts by 0.63 ps over 6 hours, with a peak-to-peak variation below 3.0 ps. The measurements reported here characterize the relative synchronization between output channels within a single QMW module.

Table II summarizes representative specifications of QMW together with those of three commercial microwave sources available in our laboratory. Sources A and C are bench-top instruments and Source B is a compact USB module; the model designations are omitted. The QMW values are obtained from the measurements reported here, whereas those for Sources A–C are taken from the manufacturers' datasheets; the table is therefore a reference for the operating range and key source-level specifications rather than a direct performance ranking. Most recently reported custom control platforms are built around data converters and take their 4–14 GHz local oscillators from external commercial instruments, so the comparison is made at the level of the

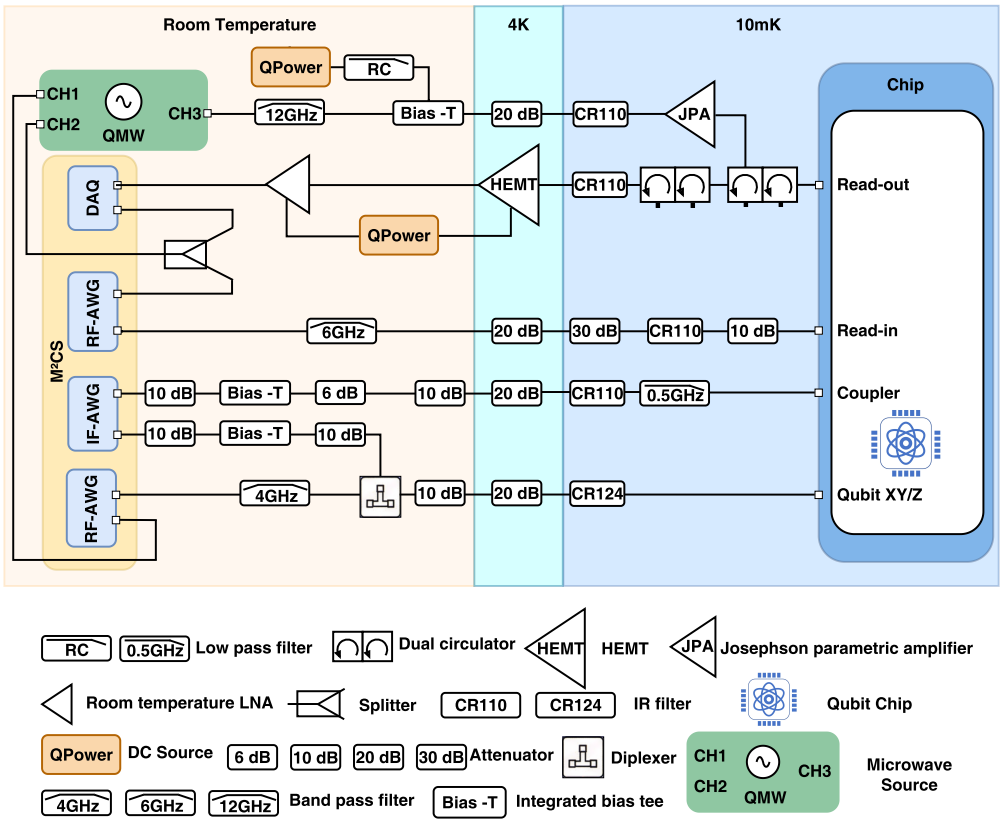


FIG. 5. **Schematic diagram of the measurement and control circuitry for superconducting quantum chips.** The QMW supplies LO signals to the M^{2}CS, enabling the RF-AWG module to synthesize XY-axis microwave drive signals and readout excitations. These components collectively realize qubit manipulation and readout, while Z-axis control signals are supplied by the IF-AWG module. In the readout pathway, microwave pulses generated by the RF-AWG module are injected into the quantum chip via cryogenic transmission lines. The reflected quantum state response signals undergo isolation through circulators before entering the JPA, where RF pumping provided by the QMW enables low-noise parametric amplification of the readout signal. Subsequently, the signals experience multi-stage gain enhancement through a HEMT and room-temperature low-noise amplifiers prior to demodulation and digitization by the M^{2}CS DAQ module. Three QMW microwave channels are utilized to support XY microwave drive generation, readout excitation, and JPA pumping.

microwave source. Sharing the reference, control, and power-management circuitry across the three channels reduces the per-channel materials cost substantially relative to using one bench-top instrument per channel.

QMW integrates three phase-synchronized output channels in one module, whereas each of the three commercial sources provides a single output. Its phase noise, minimum frequency step, and frequency-switching time do not match the best values listed, but are sufficient for the intended use: fine detuning is provided by the intermediate-frequency waveforms rather than by the local oscillator, frequency changes are made between experiments rather than within a pulse sequence, and the measured phase noise supports the coherence times and gate fidelity reported below.

III. BENCHMARK WITH SUPERCONDUCTING QUBITS

We integrate the QMW into the microwave measurement and control system (M^{2}CS) [14, 19] of a 36-qubit superconducting quantum processor. To evaluate its performance under realistic experimental conditions, we select a representative qubit for detailed characterization. As shown in Fig. 5, the QMW simultaneously provides the microwave pump for the JPA at the mixing chamber stage, the LO signal for the RF-AWG generating qubit XY control and readout excitation pulses, and the LO signal for the DAQ module performing down-conversion of qubit response signals during readout. Both the quantum processor and the JPA are thermally anchored to the mixing chamber stage of a dilution refrigerator operating below 10 mK. The qubit control and measurement chain employs multi-stage attenuation,

TABLE II. **Comparison of key metrics of QMW with three commercial microwave sources.**

Performance	QMW (this work)	Source A	Source B	Source C
Output channels	3	1	1	1
Frequency range (GHz)	4–14	0.9–12	2–8	2–20
Minimum frequency step (kHz)	100	< 0.1	0.1	< 0.1
Maximum output power (dBm)	+10	+18	+10	+18
Power flatness (dB)	< 0.3	< 1	< 2	< 4
Largest spur (dBc)	−55	−55	−40	−60
Phase noise at 10 kHz (dBc/Hz)	−110 at 5 GHz −103 at 13 GHz	−118 at 6 GHz	−84 at 6 GHz	−104 at 6 GHz
Frequency-switching time (ms)	< 9	< 20	0.1	8
Height (U)	2	2	1	3
Power consumption per channel (W)	30	150	3.25	200

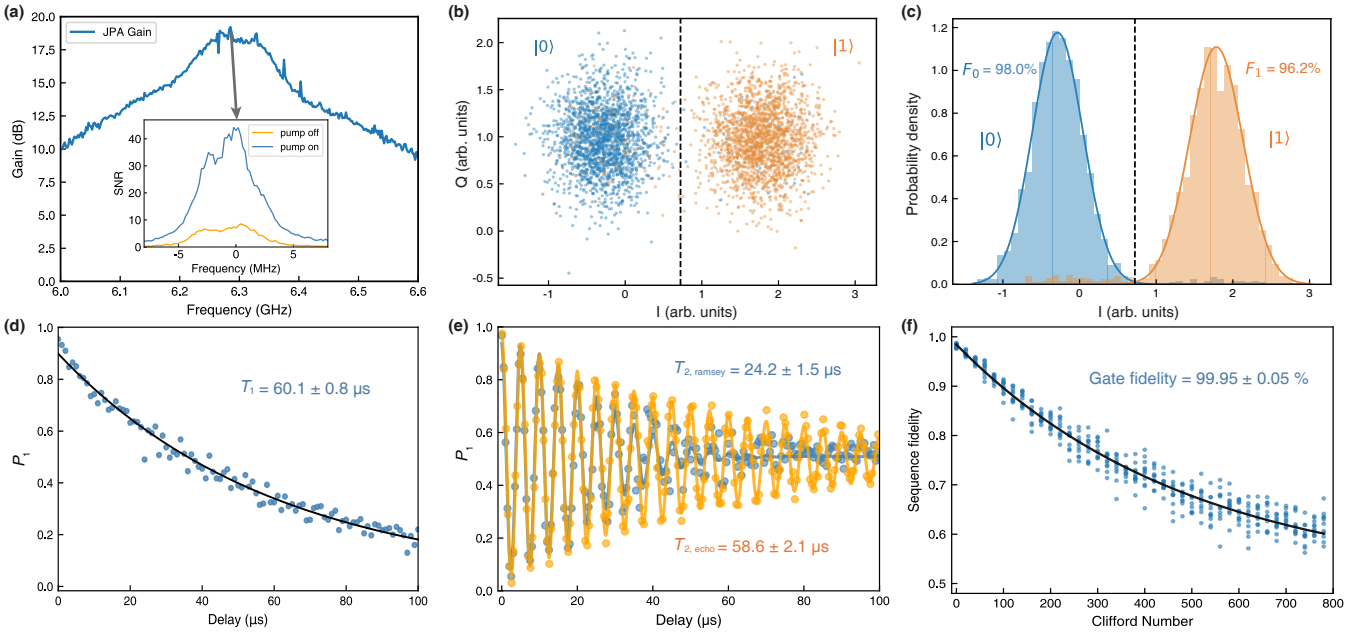


FIG. 6. **Benchmarking QMW with superconducting qubits.** (a) JPA gain spectrum, showing a signal gain of 19.2 dB at the 6.2840 GHz readout frequency. Inset: single-shot qubit-state readout SNR with and without JPA pump. (b) IQ scatter plot of the qubit prepared in the ground state $|0\rangle$ (blue) and the first excited state $|1\rangle$ (orange), where the black dashed line indicates the optimal state discrimination threshold, and the in-phase (I) and quadrature (Q) data are represented in arbitrary units. (c) Projected histogram of the data from (b) on the IQ plane, showing a readout fidelity of 98.0% for the ground state $|0\rangle$ and 96.2% for the excited state $|1\rangle$. (d), (e) Qubit coherence benchmark, showing $T_1 = 60.1 \pm 0.8$ μs, $T_{2,\mathrm{Ramsey}} = 24.2 \pm 1.5$ μs (blue), and $T_{2,\mathrm{echo}} = 58.6 \pm 2.1$ μs (yellow). (f) Single-qubit randomized benchmarking, yielding an average single-qubit gate fidelity of $99.95 \pm 0.05\%$.

filtering, and amplification to suppress thermal noise throughout the cryogenic system. Probe signals generated by the RF-AWG undergo attenuation and filtering before entering the quantum chip, while the weak quantum response signals experience sequential amplification through the base-temperature JPA, the cryogenic high electron mobility transistor (HEMT) amplifier, and a room-temperature low-noise amplifier (LNA) before digitization by the M^{2}CS DAQ module.

The JPA operates in a flux-pumped configuration and is driven by the QMW-generated pump tone. As a quantum-limited preamplifier, the JPA places stringent requirements on the spectral purity, phase noise, and power stability of its pump source [25, 41–43]. In this experiment, the 12.6 GHz pump signal is synthesized directly by the QMW. Under optimized operating conditions, with a pump power of 1 dBm and appropriate flux bias applied to the JPA, the readout signal is effectively amplified. As shown in Fig. 6(a), at a typical readout resonator frequency of 6.2840 GHz, the JPA provides a gain of 19.2 dB and improves the readout SNR by more than a factor of six, indicating stable pump operation

with low-noise readout performance.

With the JPA engaged, the qubit performance is further characterized at the operating frequency $\omega_q/2\pi = 4.8023$ GHz. The single-shot readout IQ distributions for the ground state $|0\rangle$ and excited state $|1\rangle$ are shown in Figs. 6(b) and (c), yielding readout fidelities of 98.0% and 96.2%, respectively. The well-separated IQ clusters confirm effective JPA-assisted signal discrimination and stable QMW-driven readout operation.

Qubit coherence is further characterized through the energy relaxation time T_1, Ramsey dephasing time $T_{2,\mathrm{Ramsey}}$, and spin-echo coherence time $T_{2,\mathrm{echo}}$, as shown in Figs. 6(d) and (e). From exponential fitting of the excited-state population $P_1(\tau)$, the relaxation time is extracted as $T_1 = 60.1 \pm 0.8$ μs. Ramsey interferometry measurements yield a dephasing time of $T_{2,\mathrm{Ramsey}} = 24.2 \pm 1.5$ μs from the decay envelope of the oscillatory response. By introducing a refocusing π pulse in a Hahn echo sequence to suppress low-frequency $(1/f)$ noise, the coherence time is extended to $T_{2,\mathrm{echo}} = 58.6 \pm 2.1$ μs. The gap between $T_{2,\mathrm{Ramsey}}$ and $T_{2,\mathrm{echo}}$ indicates that dephasing is dominated by low-frequency noise. This qubit was biased at 4.8023 GHz, away from its flux sweet spot, so the dominant contribution is attributed to $1/f$ flux noise, with additional contributions from two-level-system and thermal-photon fluctuations. The microwave source contributes negligibly: its integrated RMS jitter of 65 fs over 10 Hz–10 MHz corresponds to an RMS phase error of about 2 mrad at the qubit frequency.

We further evaluate the microwave drive performance of QMW in gate-level experiments using randomized benchmarking (RB) [44, 45]. Clifford sequences containing up to 800 gates yield an average single-qubit gate fidelity of $99.95 \pm 0.05\%$ (Fig. 6(f)). A single QMW module also supports simultaneous control and frequency-multiplexed readout of six qubits sharing one feedline. Across these qubits, T_1 ranges from 33.9 to 60.1 μs and $T_{2,\mathrm{echo}}$ from 27.6 to 58.6 μs. Single-qubit RB fidelities range from 99.909% to 99.951%, with an average of 99.927%. Readout fidelities are at least 98.0% for $|0\rangle$ and 94.0% for $|1\rangle$. The qubit shown in Fig. 6 has the longest coherence times among the six qubits reported here.

IV. CONCLUSION

We present QMW, a highly integrable, modular broadband microwave source tailored for large-scale superconducting quantum measurement and control. Built around the LMX2820 wideband PLL synthesizer, complemented by a dual-path spectral purification and driving stage and a precision power regulation module, the system achieves low-noise, spectrally pure microwave generation across 4–14 GHz. Electronic characterization confirms key performance metrics: (i) an SFDR better than 55 dB across the full operating band, (ii) phase noise as low as -110 dBc/Hz at a 10 kHz offset for a 5 GHz carrier and below -103 dBc/Hz across the full band, (iii) long-term power stability within 0.1 dB, and (iv) a linear output power range of -20 to $+10$ dBm with 0.5 dB resolution, all at a single-channel power consumption of 30 W. Within a unified hardware platform, QMW simultaneously supports qubit XY drive, readout excitation, and JPA pump generation. The main advance is the integration of three broadband, spectrally clean, phase-synchronized output channels covering the qubit and JPA pump bands within one compact module.

Integration with a 36-qubit superconducting quantum processor validates QMW within a complete measurement and control chain. With the QMW-generated pump tone applied, the JPA achieves a signal gain of 19.2 dB at the readout frequency, supporting high-SNR single-shot qubit readout. Qubit coherence characterization confirms that the control and readout signals generated by QMW do not limit the measured coherence times, and randomized benchmarking on the same qubit yields an average single-qubit gate fidelity of $99.95 \pm 0.05\%$, demonstrating stable gate-level performance under extended Clifford gate sequences. A single module further supports simultaneous control and frequency-multiplexed readout of six qubits. These results indicate that QMW provides the spectral purity, amplitude stability, and deterministic phase synchronization between its three output channels required for high-fidelity quantum control and readout. The synchronization results reported here are obtained between output channels within a single QMW module; the extension to several modules follows from the trigger architecture and remains to be verified experimentally.

Owing to its compact modular architecture and broad frequency coverage, the QMW design provides a scalable pathway toward the multi-channel requirements of large-scale superconducting quantum processors. Its architecture is further extensible to other quantum hardware platforms, including semiconductor spin-qubit systems [46–49], and to precision measurement applications such as microwave kinetic inductance detectors [50–52] and phased array radar systems, making QMW a candidate broadband microwave generation solution applicable beyond superconducting quantum computing. Looking forward, QMW can be improved along several directions: replacing the microcontroller with a field-programmable gate array and rebuilding the clock chain around a low-noise clock management device, so as to increase the channel density and refine the synchronization timing; extending the trigger distribution demonstrated within one module to several modules; and reducing the phase noise and the residual spurs with a lower-noise frequency synthesis unit and filters of higher out-of-band rejection.

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