Shadow-Masked Angled Ion Milling for Junction Integration in Silicon-based Tantalum Superconducting Qubits

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Abstract

Surface dielectric loss remains a primary bottleneck limiting the energy relaxation time (T_1) of superconducting qubits. In particular, the amorphization damage introduced by *in-situ* argon ion milling on silicon (Si) substrates during junction fabrication constitutes a critical local loss channel. Addressing the vulnerability of the junction substrate in the conventional Manhattan process, we propose a bandage-free, shadow-masked angled ion milling technique that is fully compatible with existing mask layouts to enhance the coherence of Ta-on-Si transmons. This process leverages the geometric masking effect of a high-aspect-ratio bilayer resist, combined with a 45° azimuthal ion beam alignment, to isolate the sensitive cross-junction region from direct ion bombardment while ensuring reliable superconducting interconnections under gentle milling conditions. Cryogenic characterization across three independent cooldowns demonstrates that the 45° angled milling effectively enhances qubit performance, with the sample-average T_1 improving from 67.4 μs in the standard 0° process to 98.7 μs, and the average quality factor (Q) increasing from 2.0×10^6 to 2.5×10^6. This work offers a practical nanofabrication strategy to suppress junction-region processing loss, providing a viable pathway for high-coherence silicon-based quantum processors.

Keywords: Quantum computation architectures and implementations, Josephson devices, Ion beam impact and interactions with surfaces, Dielectric loss and relaxation.

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1. Introduction

Superconducting circuits have become a leading platform for quantum information processing [1,2]. Recent progress spans high-fidelity two-qubit gates [3–8], multilevel control of superconducting systems [9–11], and variational quantum algorithms with error-mitigation strategies on noisy processors [12,13]. Demonstrations

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of below-threshold quantum error correction and quantum computational advantage further underscore the need for reproducible devices with low and stable physical error rates [14–16]. While the execution of these complex quantum algorithms relies heavily on the development of highly stable and scalable room-temperature measurement and control electronics [17,18], improving the intrinsic coherence at the hardware level remains equally fundamental. At the device level, the energy-relaxation time T_1 imposes a relaxation-limited bound on operation fidelity and contributes to error accumulation in long quantum circuits. Extending and stabilizing T_1 therefore remains an important objective in the materials engineering and fabrication of superconducting quantum processors.

In planar superconducting qubits, dielectric loss associated with two-level-system (TLS) defects at surfaces and interfaces constitutes a major device-dependent relaxation channel [19–21]. Its contribution depends on both material loss and the electric-field participation of the relevant interfaces [22–24]. The junction-integration step is particularly sensitive. In the overlap Manhattan-style process considered here, in situ argon (Ar) ion milling is performed after resist patterning and before junction-lead evaporation to remove native oxide from exposed base-layer contact pads. Although this step enables a low-resistance galvanic connection, the ion beam can also modify the cleaned metal surface and the neighboring exposed substrate.

For Nb-based resonators, Ar milling has been reported to alter the surface oxide and increase TLS-related microwave loss by approximately an order of magnitude under the conditions studied [25]. More generally, fabrication residues and aggressive surface treatments have been linked to excess substrate-related loss in superconducting circuits [26]. Under a specific junction-milling recipe, cross-sectional microscopy further revealed an amorphous Si layer approximately 3.9 nm thick, with less damage observed on sapphire [27]. Such collateral modification may introduce an additional TLS-related dielectric-loss channel near the junction, depending on the milling conditions and local electric-field participation.

Several junction-integration schemes have been developed to reduce this exposure. A separately patterned bandage can suppress junction-region processing loss but requires additional lithography and metallization [27]. In situ bandaged junctions [28] and patch-integrated cross-type (PICT) processes [29] reduce this overhead by incorporating the contact patch into junction fabrication. However, the patch geometry remains coupled to the resist profile and evaporation angles. A bandage-free method that retains the standard Manhattan workflow while reducing direct ion exposure of the central junction substrate is therefore highly desirable. Tantalum (Ta) films provide an ideal platform for such a scheme. Beyond enabling transmons with long coherence times [30], native tantalum oxide (TaO_x) exhibits a significantly lower physical sputtering threshold than aluminum oxide (AlO_x) [31,32]. This intrinsic material property allows complete oxide removal at a drastically lower ion milling dose. Consequently, reliable Ohmic connections can be achieved under ultra-low-energy and short-duration milling conditions, which minimizes organic contamination from resist sidewall resputtering even under oblique incidence angles.

Here, we introduce a bandage-free, shadow-masked angled ion-milling process for Ta-on-Si transmon qubits. By adjusting the azimuthal incidence angle of the argon ion beam relative to the junction arms, the standard bilayer resist mask naturally shadows the sensitive cross-junction region during surface oxide removal while leaving the contact areas accessible. This geometry-enabled self-shadowing approach prevents substrate damage without adding extra lithography or metallization steps. Across multiple fabrication batches, the process demon-

strates reliable junction fabrication and a normal-state resistance coefficient of variation of $\sim 4.3\%$. In paired cryogenic measurements, qubits fabricated with this optimized milling geometry exhibit higher sample-mean T_1 values than conventional controls, alongside a more modest change in quality factor (Q) and comparable temporal stability in T_1, offering a practical, scalable alternative to patch-based integration.

2. Fabrication of Superconducting Qubit

High-resistivity silicon (Si) wafers were selected as the substrates because they are intrinsically more susceptible to ion-milling-induced amorphization, thereby amplifying the observable effects of our angled ion milling technique. The superconducting qubits were fabricated following a standard superconducting quantum circuit process flow. Initially, the high-resistivity Si wafers underwent a pretreatment using a buffered oxide etch (BOE) for 90 s to remove the native silicon dioxide layer, which is a known source of decoherence. Subsequently, the samples were immediately transferred into a magnetron sputtering system, where a 200-nm-thick tantalum (Ta) film was deposited under ultra-high vacuum conditions. Following this, S1813 photoresist was spin-coated at 3000 rpm. A direct-write laser lithography system was utilized to define the base circuit patterns, encompassing superconducting readout resonators, control lines, and transmon capacitor pads. The patterns were then transferred into the Ta film via reactive ion etching (RIE). Next, oxygen plasma ashing was employed to strip the fluorocarbon polymer 'crust' generated during the RIE process. The resist was then removed by immersing the samples in a heated N-Methyl-2-pyrrolidone (NMP) solution. Finally, a 5-minute piranha solution clean was performed to thoroughly eradicate any remaining organic residues, yielding an atomically clean Ta base-layer circuitry.

Subsequently, the superconducting Josephson junctions (JJs) were fabricated using the conventional Manhattan-style process. Given that typical qubits operate at frequencies of approximately 3–5 GHz, the corresponding junction dimensions are on the order of hundreds of nanometers; therefore, electron-beam lithography (EBL) was utilized to define the JJ patterns. A bilayer resist stack consisting of P(MMA 8.5 MAA) EL11 and PMMA 950K A7 was spun to a total thickness of approximately 1.2 μm. Following EBL exposure and development to form the requisite undercut profile, the samples were loaded into an electron-beam evaporator for JJ deposition under ultra-high vacuum conditions.

Subsequently, the Josephson junctions (JJs) were fabricated using a modified Manhattan-style process that incorporates our shadow-masked ion milling technique. Given that typical qubits operate at frequencies of approximately 3–5 GHz, the corresponding junction dimensions are on the order of hundreds of nanometers; therefore, electron-beam lithography (EBL) was utilized to define the JJ patterns. A bilayer resist stack consisting of P(MMA 8.5 MAA) EL11 and PMMA 950K A7 was spun to a total thickness of approximately 1.2 μm. Following EBL exposure and development to form the requisite undercut profile, the samples were loaded into an electron-beam evaporator for *in-situ* milling and junction deposition under ultra-high vacuum conditions.

To mitigate substrate amorphization while establishing a reliable electrical connection between the JJs and the base-layer circuitry, we replaced the conventional ion milling with our proposed "Shadow-Masked Angled Ion Milling" technique under a mild milling condition (accelerating voltage of 300 V and beam current of 21 mA). Specifically, the wafer stage was set to a fixed polar incidence angle of $\theta = 45^\circ$ relative to the wafer normal for both processes. In our proposed configuration, the wafer was rotated in-plane to set the

azimuthal angles to $\phi_1 = 45°$ and $\phi_2 = 135°$ for the two sequential milling steps. This directly contrasts with the conventional Manhattan process, where the two milling steps are performed at azimuthal angles of $\phi_1 = 0°$ and $\phi_2 = 90°$ (aligned parallel to the orthogonal junction arms). By steering the in-plane projection of the ion beam to intersect the cross-junction electrodes at 45°, and provided that the geometric condition $h\tan(45°) > L/\sin(45°)$ is satisfied—where h is the resist thickness and L is the junction side length (assuming equal lengths for the orthogonal arms)—the bilayer resist mask effectively acts as a physical barrier, shadowing and shielding the substrate at the cross-junction center from direct ion bombardment. Following the milling step, standard double-angle evaporation was executed to form Al/AlO_x/Al superconducting JJs on the pristine, undamaged Si substrate.

Initially, *in-situ* argon (Ar) ion milling was required to establish a reliable electrical connection between the JJs and the base-layer circuitry. For this step, we employed a mild milling condition (accelerating voltage of 300 V and beam current of 21 mA) within the proposed "Shadow-Masked Angled Ion Milling" technique. Specifically, the wafer stage was set to a fixed polar incidence angle of $\theta = 45°$ relative to the wafer normal for both processes. In our proposed configuration, the wafer was rotated in-plane to set the azimuthal angles to $\phi_1 = 45°$ and $\phi_2 = 135°$ for the two sequential milling steps. This contrasts with the conventional Manhattan process, where the two milling steps are performed at azimuthal angles of $\phi_1 = 0°$ and $\phi_2 = 90°$ (parallel to the orthogonal junction arms). By steering the in-plane projection of the ion beam to intersect the cross-junction electrodes at 45°, and provided that the geometric condition $h\tan(45°) > L/\sin(45°)$ is satisfied—where h is the resist thickness and L is the junction side length (assuming equal lengths for the orthogonal arms)—the bilayer resist mask effectively acts as a physical barrier, shadowing and shielding the substrate at the cross-junction center from direct ion bombardment.

Following the Shadow-Masked Angled Ion Milling process, standard double-angle evaporation was executed to form Al/AlO_x/Al superconducting JJs on the pristine, undamaged Si substrate. Upon completion of the deposition, the wafer was diced and subjected to a lift-off process, yielding standard four-qubit chips. The detailed fabrication steps and the resulting devices are illustrated in Fig. 1.

3. Results and Discussion

To comprehensively evaluate the efficacy and reliability of the proposed shadow-masked 45° angled ion beam etching (IBE) technique, we performed a systematic, multi-tiered electrical characterization. First, macroscopic wafer-level room-temperature resistance measurements were conducted to assess process yield and spatial uniformity without necessitating layout modifications. Subsequently, the fabricated chips were cooled in a dilution refrigerator to extract their quantum coherence metrics in the milli-Kelvin regime. The following sections detail the junction resistance statistics, the comparative results of the qubit energy relaxation time (T_1) and dephasing time (T_2), as well as a rigorous analysis of the T_1 temporal stability. Together, these datasets quantitatively validate the engineering robustness of this novel technique and its superiority in achieving and sustaining high quantum coherence.

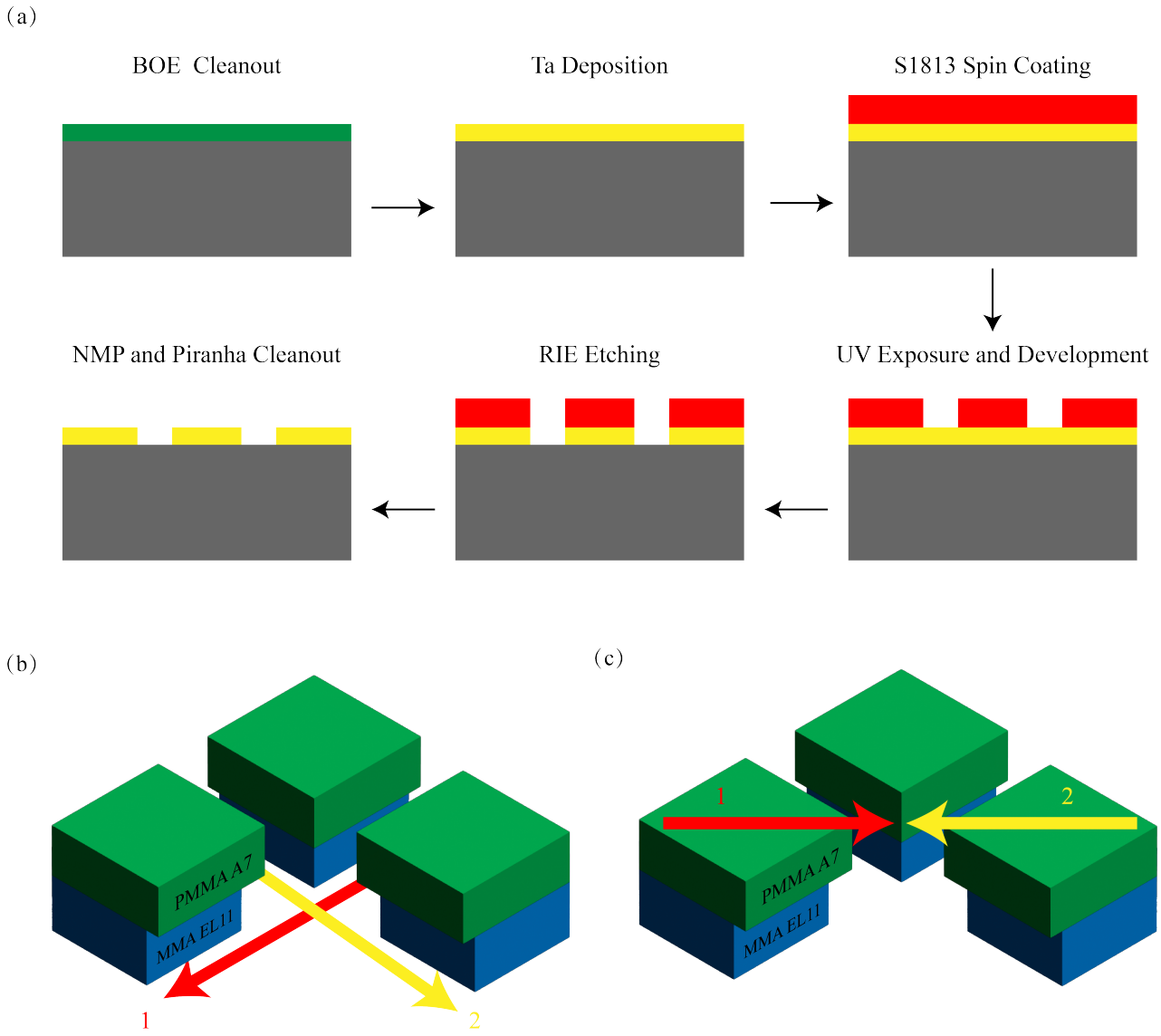


Figure 1: Schematic of the superconducting qubit fabrication process. **(a)** Standard process flow for defining the Ta base-layer circuitry on high-resistivity Si substrates. The color scheme is as follows: dark gray for the high-resistivity Si substrate, green for the native oxide layer, yellow for the superconducting Ta film, and red for the photoresist. The sequence includes BOE pretreatment, magnetron sputtering of Ta, UV lithography using S1813 resist, pattern transfer via reactive ion etching (RIE), and thorough residue removal using NMP and piranha solutions. **(b)** Conventional Manhattan-style milling configuration ($\theta = 45°$, $\phi_1 = 0°$ and $\phi_2 = 90°$), where the sequential ion beams are aligned parallel to the orthogonal junction trenches, leaving the central junction substrate fully exposed to ion bombardment. **(c)** Configuration of the proposed shadow-masked angled ion milling technique ($\theta = 45°$). The in-plane projections of the two sequential Ar ion beams (indicated by arrows 1 for $\phi_1 = 45°$ and 2 for $\phi_2 = 135°$) intersect the PMMA/MMA cross-junction trenches at a 45° azimuthal angle. This geometry leverages the physical height of the thick bilayer resist to shadow and shield the central junction substrate from ion-induced amorphization.

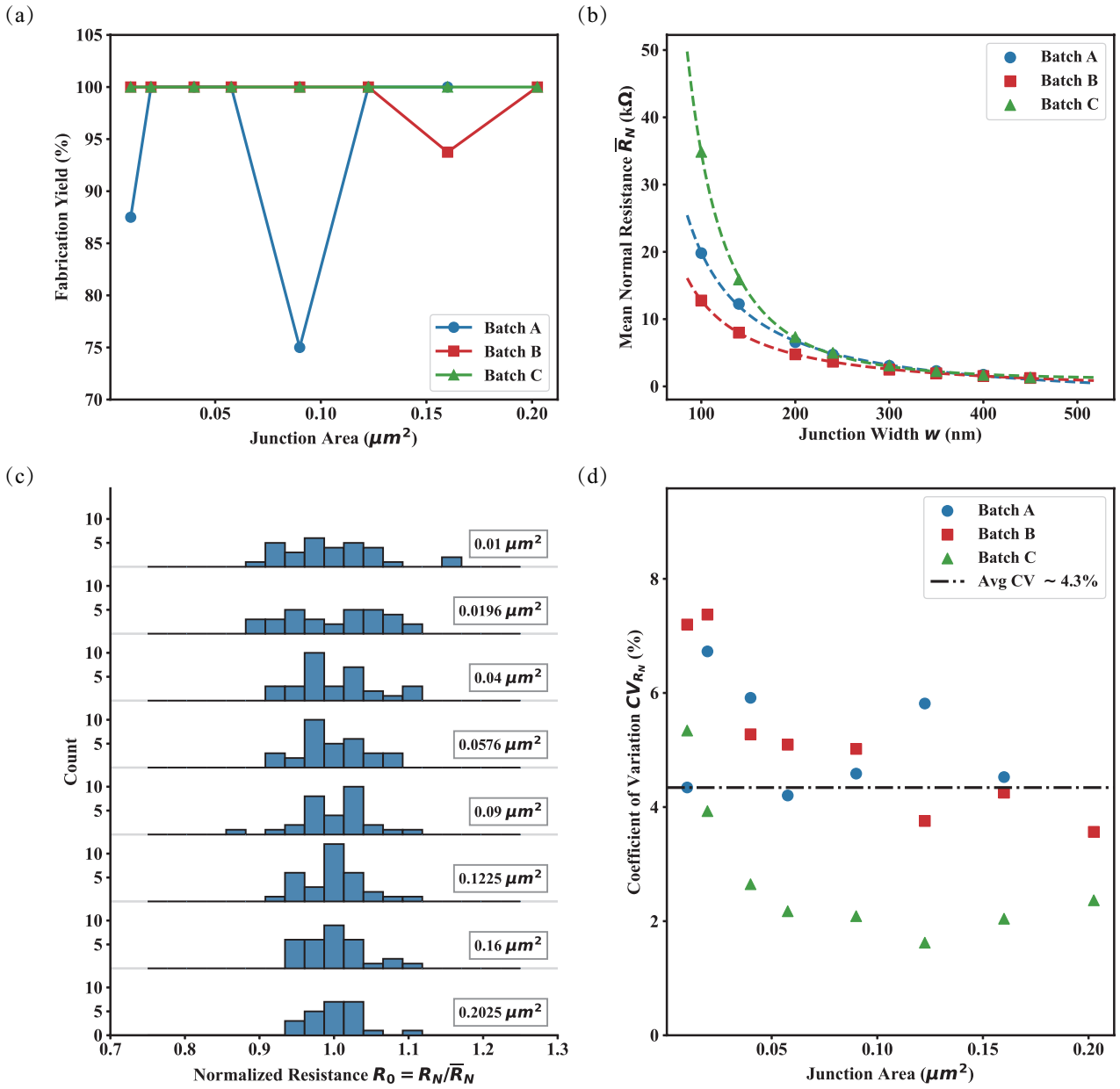


Figure 2: Wafer-level room-temperature resistance statistics of the Josephson junctions fabricated with the shadow-masked 45° angled IBE process across three independent batches with varying oxidation conditions. **(a)** Fabrication yield as a function of the junction area. **(b)** Mean normal-state resistance ($\overline{R}_N$) versus junction design linewidth (w). The dashed lines represent fits to the geometric scaling model $R_N(w) = \rho_n/(w - \delta w)^2 + R_{\text{series}}$ to extract the fabrication bias (δw), specific resistance (ρ_n), and parasitic series contact resistance (R_{series}). **(d)** Measured coefficient of variation (CV_{R_N}) as a function of the junction area, showing an average fluctuation of ~4.3%.

3.1. Junction Resistance Yield and Uniformity Testing

To comprehensively evaluate the macroscopic metrics, we collected statistical room-temperature resistance data from three independent fabrication batches. In these batches, the effective in-situ oxidation conditions were varied to target different normal-state resistance-area products ($R_N A$), which is a standard procedure for tuning eventual qubit frequencies. Specifically, while the nominal static oxidation target was set to 30 Torr for 5 minutes across all batches, the distinct R_N branches were achieved through practical equipment-induced variations. These included altered chamber base pressure following routine equipment maintenance (Batch B) and inherent chamber-to-chamber variations from utilizing a second identical electron-beam evaporator system (Batch C). The measured junction design linewidths range from 100 nm to 450 nm. Aggregating these systematic measurements allows us to precisely quantify both the fabrication yield and the spatial homogeneity across different resistance regimes. The comprehensive statistical results are summarized in Fig. 2.

Figure 2(a) illustrates the fabrication yield as a function of the junction area for the three batches. Across the operational design window, the angled milling strategy maintains an exceptionally high survival rate. It is worth noting that the isolated yield drop observed at the 0.09 μm^2 area (300 nm linewidth) in Batch A is merely an artifact of the wafer-edge effect, where test structures in a specific quadrant were located too close to the wafer periphery, leading to incomplete UV exposure of the underlying base circuitry. Even at the deep sub-micron scale (e.g., 100 nm), the process exhibits robust reproducibility across all oxidation conditions. This indicates that the 45° angled IBE is a gentle pattern transfer method that avoids catastrophic resist collapse or mask degradation.

The dimensional control of the process is evaluated in Fig. 2(b), which plots the mean room-temperature resistance ($\overline{R}_N$) against the junction design linewidth (w). Physically, the normal-state resistance scales inversely with the effective junction area, defined as $R_N(w) = \rho_n / A_{\text{eff}}$, where ρ_n is the specific resistance. To accurately capture the scaling physics and extract the lithographic and etch bias (δw), the effective area is expressed as $A_{\text{eff}} = (w - \delta w)^2$, leading to the geometric scaling model:

$$R_N(w) = \frac{\rho_n}{(w - \delta w)^2} + R_{\text{series}} \tag{1}$$

where R_{series} accounts for the parasitic series contact resistance. The three datasets clearly form distinct parallel branches corresponding to their oxidation parameters, yet all excellently follow the fitted model. This macroscopic scaling consistency confirms that the angled milling accurately and predictably transfers the junction dimensions without inducing severe nonlinear edge damage, allowing for reliable targeting of junction resistances.

To assess the global uniformity independent of the specific oxidation targets, we plot the layered distributions of the normalized resistance, $R_0 = R_N / \overline{R}_N$, categorized by junction sizes in Fig. 2(c). Regardless of the junction dimension or the absolute resistance values from different batches, the normalized resistances are tightly clustered around the ideal value of 1.0. This indicates an excellent global spatial homogeneity of the tunnel barriers formed by our technique.

Finally, Fig. 2(d) presents the coefficient of variation (CV_{R_N}) of the junction resistance versus the junction area. Due to the limited sample volume per specific size, a strict geometry-dominated divergence (which typically scales as $1/\sqrt{A}$) is not perfectly resolved. Instead, the measured CV_{R_N} displays a scattered distribution with

a highly consistent average of approximately 4.3% across all sizes and batches. It is important to emphasize that a resistance variation in this regime is well within a reasonable and acceptable window for state-of-the-art superconducting junction fabrication. This constant variation validates that the angled IBE process preserves global junction integrity without introducing dimension-dependent degradation, demonstrating stable and well-controlled junction resistance fluctuations throughout the process.

3.2. Comparison and Time-Stability of Qubit Lifetime

Building upon the room-temperature yield and uniformity results, we present a systematic comparison of the quantum coherence metrics—specifically the energy relaxation time (T_1) and dephasing time (T_2)—between qubits fabricated using the proposed shadow-masked 45° angled IBE and the conventional 0° normal-incidence IBE. Because T_1 and its temporal fluctuations are sensitive indicators of microscopic two-level system (TLS) defects and surface participation ratios, these measurements provide crucial insights into fabrication-induced dielectric loss. We first examine the baseline coherence times achieved by both etching strategies, followed by a statistical analysis of the T_1 temporal stability to further elucidate the effect of the angled milling process.

To rigorously eliminate variations in the cryogenic thermal environment, electromagnetic shielding, and wiring attenuation, the coherence performance was evaluated using carefully designed paired measurements. During each dilution refrigerator cooldown, a multi-qubit chip fabricated with the shadow-masked 45° IBE and a counterpart fabricated with the 0° IBE were mounted and measured simultaneously. As summarized in Table 1, this back-to-back testing protocol was repeated across three independent cooldown runs, allowing us to gather statistics from multiple individual qubits. To ensure a rigorous comparison, the T_1 values were extracted from data collected during time windows where the relaxation time remained consistently stable. Notably, for Q_{1E} in the 0° IBE baseline chip, its relaxation time was severely suppressed beyond the reliable characterization threshold due to a strong Purcell effect. Specifically, its high qubit frequency ($f_{01} = 5.977$ GHz) yields a small detuning of only 452 MHz from its associated readout resonator ($f_r = 6.429$ GHz). Because this lifetime degradation originates strictly from an architectural parameter detuning rather than fabrication-induced material loss, Q_{1E} is excluded from the statistical coherence averages to ensure an unbiased comparison between the two etching strategies. It is also worth noting that the conventional 0° IBE typically induces more severe over-etching of the mask profile, resulting in a larger effective junction area and consequently higher qubit frequencies compared to the shadow-masked 45° IBE. To mitigate the influence of this inherent frequency shift, our coherence comparison relies on the quality factor (Q), which normalizes the frequency difference. Across all three consecutive runs, the devices treated with the shadow-masked 45° angled IBE demonstrated a clear enhancement in energy relaxation time (T_1). Meanwhile, the quality factors (Q) exhibited a marginal improvement, indicating that the optimized etching profile benefits the coherence performance without introducing additional degradation channels.

To visually capture these statistical distributions, Fig. 3 presents the individual qubit measurements for both fabrication processes. The data points are displayed as jittered scatter plots to reveal the full distribution without overlapping, accompanied by their respective mean (μ) and standard deviation (σ) values. This statistical representation corroborates our observations: it clearly highlights the pronounced upward shift in the T_1 averages for the 45° IBE devices, while reflecting a more comparable, yet slightly optimized, distribution of Q values.

Table 1: Summary of individual qubit coherence metrics across three independent dilution refrigerator cooldowns. In each run, a multi-qubit chip fabricated with the shadow-masked 45° IBE and a counterpart with the 0° IBE were measured simultaneously to ensure an identical cryogenic environment. The quality factor is extracted using $Q = 2\pi f_{01} T_1$. (†For Q_{1E}, its lifetime is heavily suppressed below the characterization limit due to Purcell decay arising from a small detuning of 452 MHz between the qubit frequency and its readout resonator at 6.429 GHz, and is thus omitted from statistical averages.)

Cooldown	Process	Qubit	f_{01} (GHz)	T_1 (μs)	T_2 (μs)	Q ($\times 10^6$)
Run 1	45° IBE	Q_{1A}	4.949	41.57	17.37	1.29
		Q_{1B}	3.500	83.65	24.16	1.84
		Q_{1C}	3.577	156.41	95.23	3.51
		Q_{1D}	3.538	120.70	22.54	2.68
	0° IBE	$Q^\dagger_{1E}$	5.977	-	-	-
		Q_{1F}	4.433	37.43	24.73	1.04
		Q_{1G}	4.424	86.73	55.56	2.41
		Q_{1H}	4.491	17.60	28.84	0.50
Run 2	45° IBE	Q_{2A}	4.085	97.42	21.19	2.99
		Q_{2B}	4.081	96.39	17.81	2.47
		Q_{2C}	4.187	71.88	10.71	1.89
		Q_{2D}	4.262	134.20	24.04	3.59
		Q_{2E}	4.240	116.71	18.57	3.11
	0° IBE	Q_{2F}	5.036	102.12	16.01	3.23
		Q_{2G}	5.010	95.79	25.72	3.02
		Q_{2H}	4.619	77.57	17.58	2.25
		Q_{2I}	4.756	115.37	17.22	3.45
		Q_{2J}	4.706	94.80	34.72	2.80
Run 3	45° IBE	Q_{3A}	3.998	96.50	29.53	2.42
		Q_{3B}	4.057	101.32	11.20	2.58
		Q_{3C}	4.081	25.35	4.67	0.65
		Q_{3D}	4.037	90.76	13.28	2.30
		Q_{3E}	4.012	130.00	12.63	3.28
	0° IBE	Q_{3F}	5.050	62.59	18.57	1.99
		Q_{3G}	4.949	45.45	10.52	1.41
		Q_{3H}	4.987	22.15	11.54	0.69
		Q_{3I}	5.060	61.91	19.06	1.97
		Q_{3J}	5.280	56.59	20.06	1.88

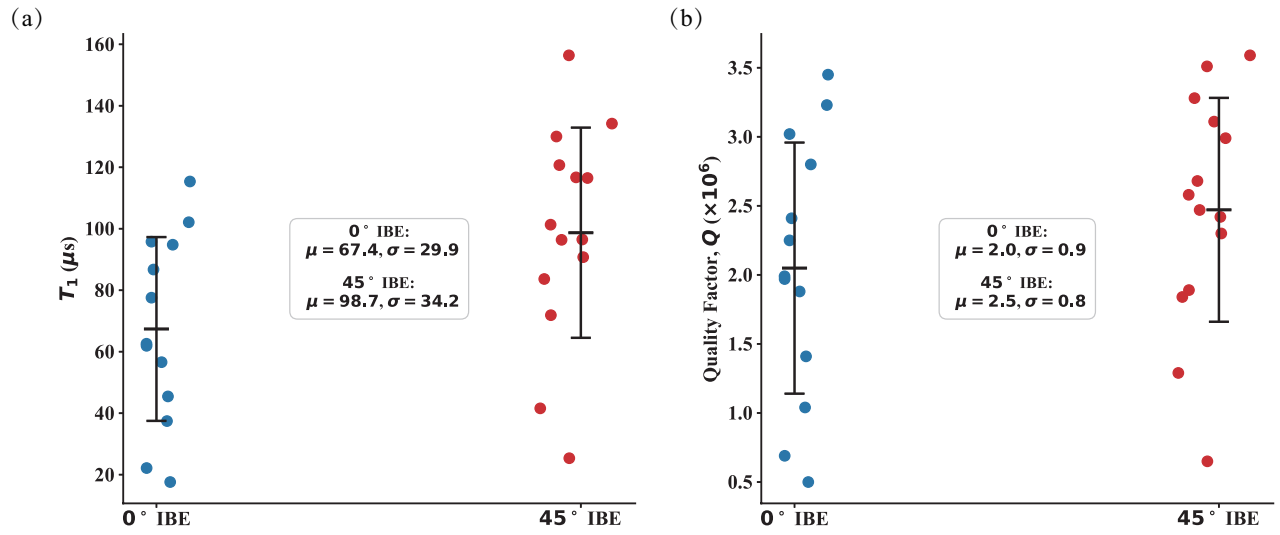


Figure 3: Statistical distribution of qubit coherence metrics fabricated with 0° IBE (blue) and shadow-masked 45° IBE (red). **(a)** Energy relaxation time (T_1) and **(b)** Quality factor (Q). The data are presented as jittered scatter plots to display all individual qubit measurements without overlapping. The solid black horizontal lines and error bars denote the mean (μ) and standard deviation (σ) of each distribution, respectively. The corresponding numerical values for μ and σ are annotated in the center of each panel.

To further evaluate the robustness of the coherence enhancement, we investigated the temporal stability of T_1 over continuous measurement periods. Superconducting qubits inevitably experience temporal fluctuations in relaxation times, primarily attributed to their interactions with a changing configuration of strongly coupled two-level system (TLS) defects. As depicted in Fig. 4, the T_1 values of both the 0° IBE and the shadow-masked 45° IBE devices were continuously monitored across the three independent dilution refrigerator cooldown runs. As observed, the qubits treated with the shadow-masked 45° IBE not only exhibit an enhanced T_1, but also demonstrate temporal stability comparable to their conventional 0° IBE counterparts during the same measurement run. This indicates that our shadow-masked 45° IBE process can yield qubits with both extended lifetimes and robust stability.

3.3. Discussion on Coherence Enhancement and Process Comparison

At this stage, we primarily attribute the observed coherence enhancement to the effective protection of the substrate-base metal interface during the IBE process. Previous efforts to mitigate substrate amorphization include the Bandage process [27]. While it effectively shields the junction substrate and eliminates interface two-level system (TLS) losses, the requisite additional lithography and deposition steps prolong the fabrication cycle and increase the risk of interlayer contamination.

The patch-integrated cross-type (PICT) process [28,29] avoids these extra lithography steps but introduces its own set of limitations. First, its strict geometric constraints create strong parameter coupling: layout dimensions, resist thickness, and evaporation angles are highly interdependent. This makes bandage formation highly sensitive to wafer-level resist uniformity, significantly narrowing the process window. Second, PICT relies on microscopic stripes for electrical connection. This reduced contact area can induce extra resistance

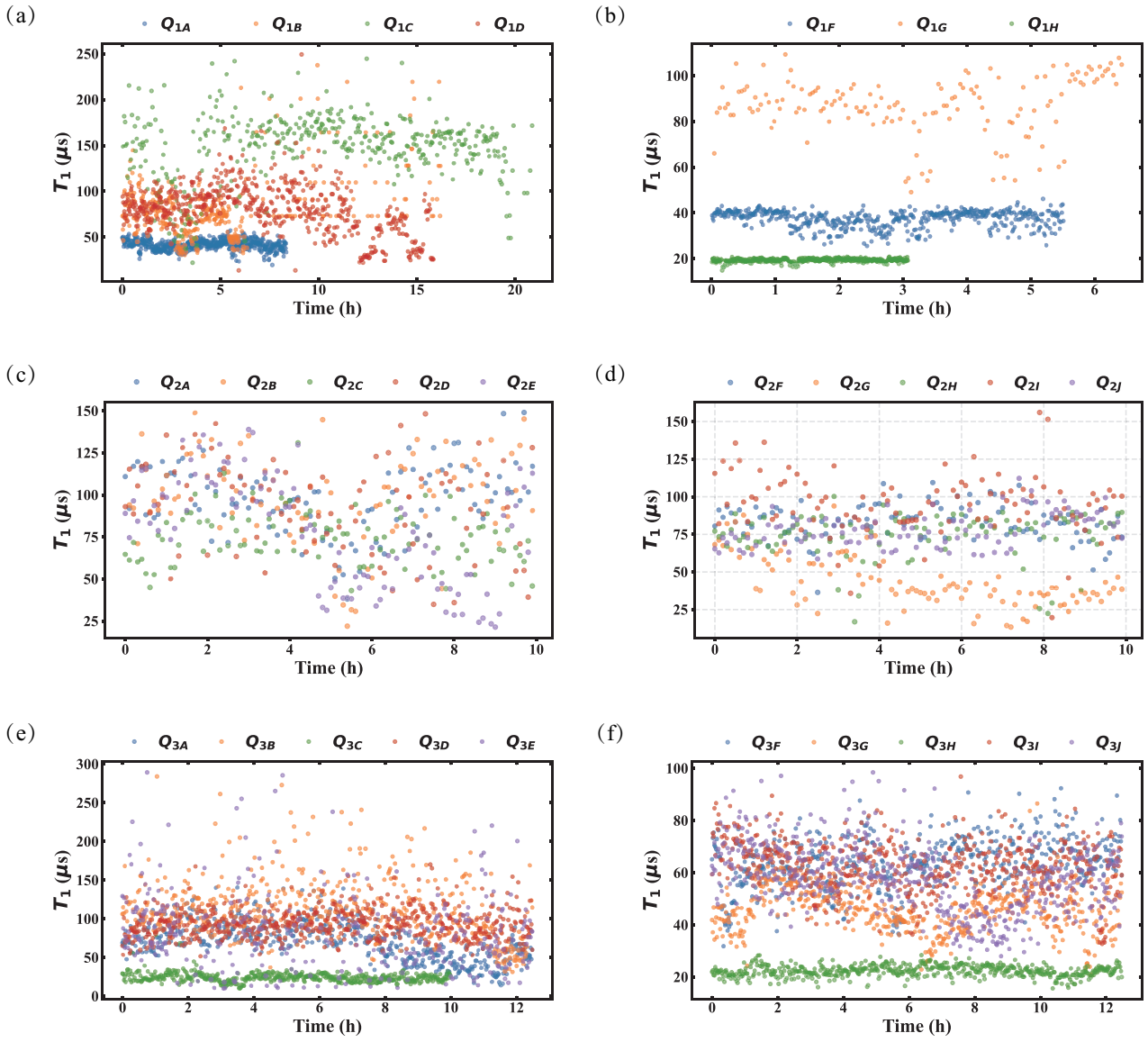


Figure 4: Temporal stability of the energy relaxation time (T_1) measured over continuous periods. The data are presented for three independent dilution refrigerator cooldown runs, labeled as **(a)(b)** Cooldown 1, **(c)(d)** Cooldown 2, and **(e)(f)** Cooldown 3.

fluctuations during room-temperature probing, complicating the accurate characterization of junction resistance.

In contrast, our shadow-masked angled ion milling technique offers a straightforward alternative. By leveraging the physical height of the bilayer resist and adjusting the ion beam's azimuthal angle, this method effectively protects the cross-junction interface. It requires no extra fabrication steps and imposes no stringent geometric layout constraints, thereby achieving a clear coherence improvement while preserving the simplicity and reproducibility of the standard Manhattan workflow.

4. Conclusion and Outlook

In summary, we have developed and experimentally validated a shadow-masked angled ion milling technique to mitigate substrate amorphization in the fabrication of silicon-based tantalum (Ta-on-Si) superconducting qubits. By simply adjusting the azimuthal angle of the Ar ion beam to 45°, the bilayer resist effectively shields the fragile cross-junction substrate from direct ion bombardment. Wafer-level characterizations demonstrate that this technique maintains exceptional device yield and junction resistance uniformity, validating its high reproducibility. Cryogenic measurements across multiple cooldowns confirm a clear enhancement in quantum coherence, with the average energy relaxation time (T_1) improving from 67.4 μs to 98.7 μs, alongside robust temporal stability. Crucially, this method bypasses the geometric constraints and additional processing steps associated with alternative interface-protection strategies, offering a highly practical solution for scalable quantum chip manufacturing.

Looking forward, several avenues can be explored to further refine this process and maximize qubit performance. First, a systematic multidimensional optimization of the ion beam incidence geometry—including both the tilt angle relative to the wafer plane and the azimuthal angle relative to the orthogonal junction arms—could provide a more precise control over the shielding profile, potentially yielding further coherence improvements. Additionally, while angled milling significantly suppresses substrate amorphization, oblique incidence might introduce subtle interactions with the resist sidewalls. To address this, future processes could incorporate a hybrid milling strategy: following the primary shadow-masked angled milling with an ultra-low-energy 0° conventional IBE sweep. This secondary gentle cleaning step would serve to eradicate any potential trace organic residues at the contact interface, ensuring pristine Ohmic connectivity while strictly preserving the protective benefits of the shadow-masking technique.

Appendix A: Experimental Setup and Cryogenic Wiring

All coherence and gate performance measurements were conducted in a dilution refrigerator with a base temperature below 10 mK, with the full room-temperature electronics and cryogenic wiring schematic illustrated in Fig. 5. To ensure phase stability, the room-temperature control system—comprising AWG2000, DC1000, and CTP1000 modules—is locked to a high-precision rubidium atomic clock and trigger system, driving four parallel input and output lines (×4). Along the input path (*Probe in & drive*), microwave and DC signals are progressively thermalized from 300 K down to the mixing chamber (10 mK) using a series of inline attenuators (20 dB at 4 K, 0 dB feedthroughs at intermediate plates, and a cascaded 36 dB attenuation at 10 mK). Before reaching the multi-qubit sample, the input signals pass through an 8 GHz low-pass filter and a CR-110 infrared

filter to suppress thermal and high-frequency radiation. On the output path (*Probe out*), the reflected readout signals are isolated by three cascaded circulators/isolators at 10 mK to protect the qubits from amplifier noise, followed by a low-noise HEMT amplifier at 4 K (3 dB attenuator inline) and room-temperature amplification before acquisition.

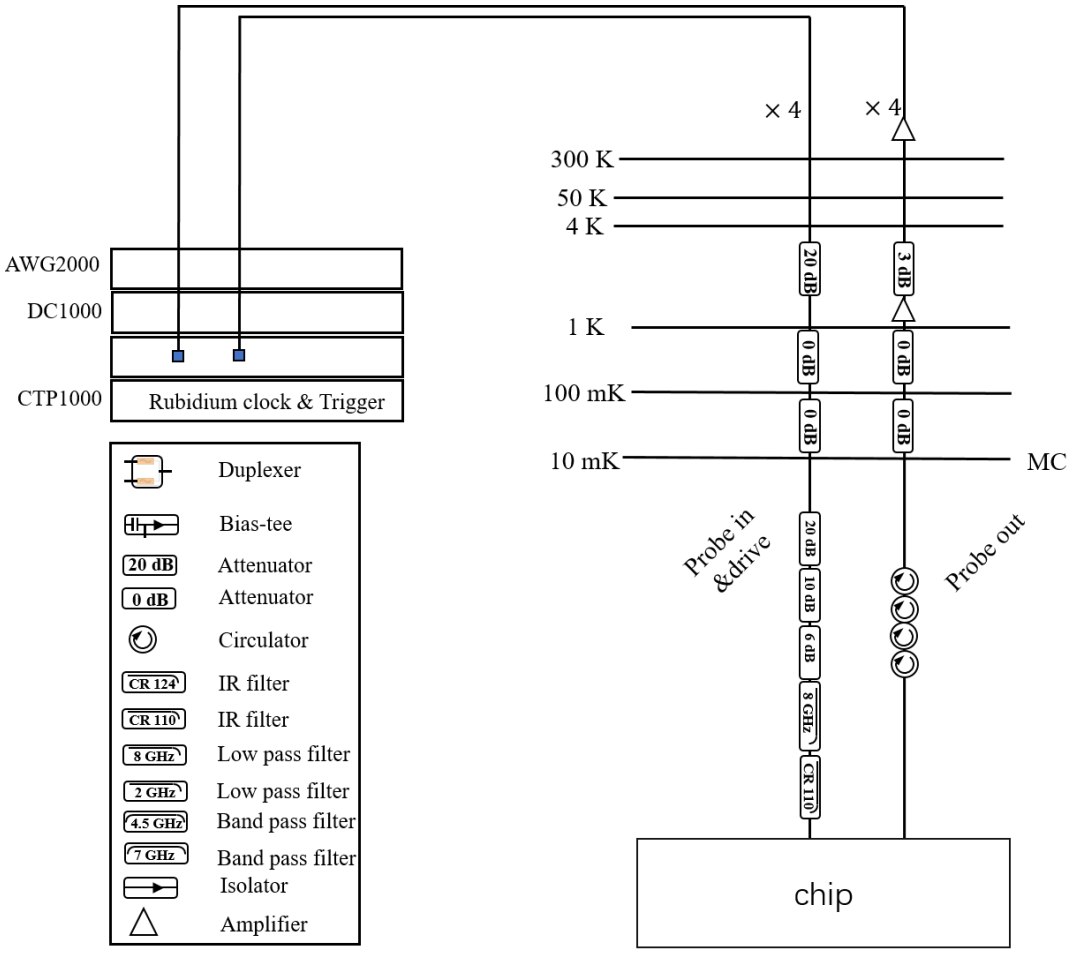


Figure 5: Schematic of cryogenic wiring and control electronics.Diagram showing room-temperature instrumentation, attenuation, filtering, and amplification chains across cryogenic stages down to 10 mK.

Appendix B: Scanning Electron Microscopy of Shadow-Masked Josephson Junctions

To evaluate the structural integrity and geometric fidelity of the fabricated devices, high-resolution scanning electron microscopy (SEM) characterization was performed. Figure 6(a) displays a large-field-of-view SEM image of the SQUID loop architecture and surrounding contact pads, illustrating the complete layout processed with the shadow-masked 45° angled ion beam etching (IBE). The image confirms clean, unetched substrate regions without post-process contamination or fence-like redeposition artifacts. Figure 6(b) shows a high-magnification SEM view of the cross-junction overlap area, detailing the Al/AlO_x/Al Josephson junction formed by two orthogonal aluminum leads. The close-up view demonstrates crisp edge definition, uniform overlap geometry, and robust metallic continuity across the junction interface.

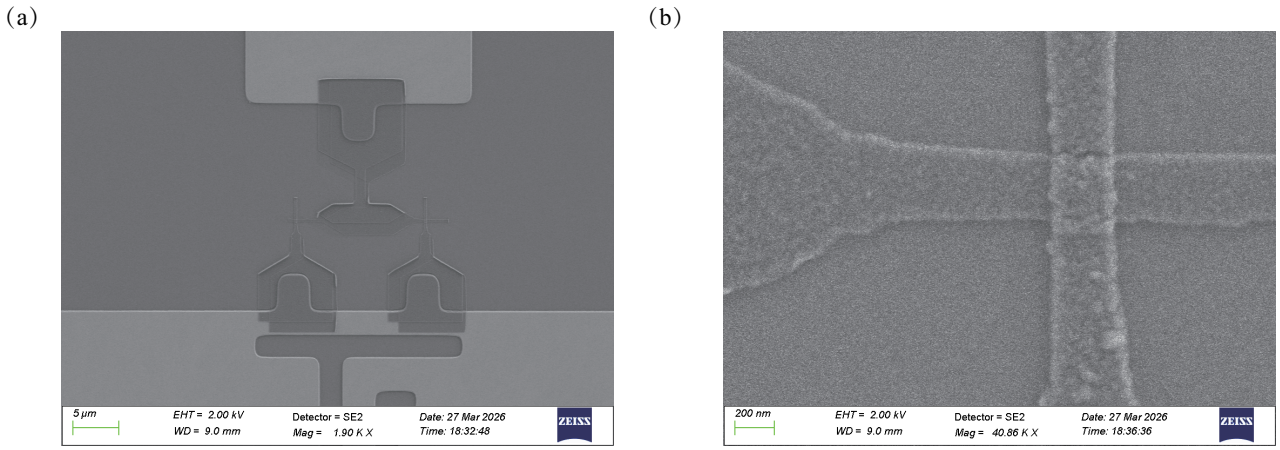


Figure 6: **Scanning electron micrographs of the fabricated Josephson junction. (a)** Overview SEM image showing the SQUID loop, junction leads, and surrounding capacitor pads defined via the shadow-masked 45° angled IBE process. **(b)** High-magnification close-up of the overlap region forming the Al/AlO_x/Al Josephson junction, showcasing sharp boundary profiles and a clean, uniform interface.

Data availability statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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