Forward and reverse voltage stress-induced degradation of 1.55kV p-NiO/n-Ga_2O_3 heterojunction barrier Schottky diode

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Abstract

To assess the reliability of Ga_2O_3 power diodes during the periodic switching between forward-conduction and reverse-blocking states of DC-DC converters or inverters, this study investigates the electrical degradation behavior and underlying mechanisms of p-NiO/n-Ga_2O_3 heterojunction barrier Schottky (HJBS) diodes under 5 V pulsed forward bias (PFB) and -600 V/448K high-temperature reverse bias (HTRB) stresses. To enable this study, a high-performance p-NiO/n-Ga_2O_3 HJBS diode with designed edge termination is fabricated, exhibiting suppressed high-temperature reverse leakage, a significantly enhanced breakdown voltage (BV) of 1550 V, and a specific on-resistance ($R_{on,sp}$) of 5.6 m$\Omega \cdot$ cm^2. Using this device, the post-stress degradation and subsequent temperature-dependent recovery of J_F–V_F characteristics and C–V analysis reveal that, under PFB stress, only a 0.02 V increase in turn-on voltage (ΔV_{on}) and a 1.4% decrease in current capability (ΔR) are observed, which are attributed to electron capture and rapid emission from shallow surface acceptor-like traps. Owing to the suppression of self-heating effects, the degradation observed under PFB stress is significantly less pronounced than that under DC forward bias (DFB) stress. Under HTRB stress, a 0.12 V increase in ΔV_{on} and a 13% degradation in ΔR are observed, which are presumed to be caused by elevated temperature and strong surface electric fields that induce an increase in near-interface traps. Then, some electrons are subsequently captured by bulk traps via variable range hopping (VRH). These findings provide important insights for improving the reliability of Ga_2O_3 power devices.

Keywords: p-NiO/n-Ga_2O_3, PFB, HTRB, Reliability

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1. Introduction

β-Ga_2O_3 has emerged as one of the most promising ultra-wide bandgap semiconductor materials due to its ultra-wide bandgap of approximately 4.8 eV, a high critical breakdown electric field around 8 MV/cm, and excellent thermal stability and radiation robustness [1–7]. Since its bulk crystals can be grown using the melt growth method [8–12], some research institutions have successfully developed 6-inch β-Ga_2O_3 single crystals within just a few decades [13,14]. As a result, the cost of β-Ga_2O_3 substrates is expected to decrease significantly in the foreseeable future. Moreover, the development of the p-NiO/n-Ga_2O_3 heterojunction structure has significantly enhanced the breakdown voltage (BV) of Ga_2O_3-based power diodes [15–23] and even some studies have also reported its avalanche capability [24,25].

Owing to these advantages, Ga_2O_3 diodes are regarded as promising candidates for rectifiers, inverters and DC–DC converter circuits, as well as other high-power electronic system applications. Under such operating conditions, Ga_2O_3 diodes undergo rapid dynamic switching and are repeatedly subjected to alternating Pulsed Forward Bias (PFB) stress during conduction and High-Temperature Reverse Bias (HTRB) stress during the off-state. Since the simultaneous exposure to high electric fields, dynamic switching transients, and elevated temperatures can trigger serious reliability issues (such as threshold voltage instability, interface state generation, and thermal degradation), evaluating and understanding Ga_2O_3 device reliability under combined PFB and HTRB stresses is paramount for ensuring long-term operational stability in power electronics systems [26–29]. Several studies have reported the reliability of Ga_2O_3 diodes under continuous forward bias stress, revealing that the degradation can be attributed to either an increased concentration of compensating acceptor-like traps [30] or the Ga-vacancy-related acceptor-like traps [31,32]. However, continuous forward bias stress leads to self-heating due to the poor thermal conductivity of Ga_2O_3 ($\sim$ 0.27 W/(cm·k)). The elevated junction temperature may affect the semiconductor's bandgap, electron affinity, carrier mobility and so on, which inevitably influences degradation behavior and reliability analysis. For example, junction heating has been shown to oxidize Ni into NiO [33], while 200°C continuous forward stress increases interface trap density [34]. To realistically assess the reliability of Ga_2O_3 diodes in high-power electronic systems, it is essential to eliminate thermal influences. Therefore, pulsed forward bias (PFB) stress is employed in this work instead of continuous forward bias stress. In addition, there have been only a few studies on reliability in Ga_2O_3 diodes under reverse bias conditions [35,36], and even fewer studies have focused on high-temperature reverse bias (HTRB) stresses [37,38]. Moreover, the lack of explanation for the degradation mechanisms makes it difficult to improve the robustness of Ga_2O_3 devices.

In this work, the electrical degradation of Ga_2O_3 heterojunction barrier Schottky (HJBS) diodes under pulsed forward bias (PFB) and high-temperature reverse bias (HTRB) stresses is systematically investigated. The corresponding mechanisms induced by trap effects are confirmed by post-stress degradation and subsequent temperature-dependent recovery of J_F–V_F characteristics. Furthermore, the density of near-surface shallow-level acceptor traps and the presence of bulk deep-level traps are determined through C–V analysis. Finally, the electron transport from surface traps to bulk traps via Variable Range Hopping

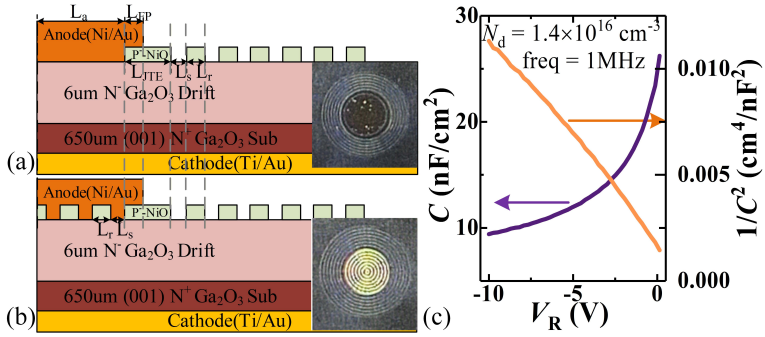


图 1: The schematic cross section and top view of designed composite termination (a) Ga_2O_3 SBDs, (b) Ga_2O_3 HJBS. (c) C-V characteristic and extracted $N_d = 1.4 \times 10^{16} cm^{-3}$ of the Ga_2O_3 SBDs.

(VRH) is elucidated by temperature-dependent leakage current characteristics.

2. Device Structure and Electrical Characteristic

The Ga_2O_3 SBDs and p-NiO/n-Ga_2O_3 HJBS diodes with designed edge terminations are fabricated to investigate reliability, as illustrated in Figures 1(a) and 1(b). The anode radius (L_a) is set to 50 μm for all diodes, and the designed edge termination comprises an 8 μm-wide p-NiO junction termination extension ($L_{JTE} = 8\mu m$), a 3 μm-wide anode field plate ($L_{FP} = 3\mu m$), and 5 floating field limiting rings (FLRs), each with a width of 3 μm and spaced 3 μm apart ($L_s = 3\mu m$, $L_r = 3\mu m$). These devices consist of a 640 μm-thick highly Sn-doped (1×10^{18} cm^{-3}) (001) n-type Ga_2O_3 substrate and 6 μm-thick lightly Si-doped (1.4×10^{16} cm^{-3}, determined via capacitance–voltage (C–V) measurement, as shown in Figure 1(c)) n-type Ga_2O_3 drift layer grown by halide vapor phase epitaxy (HVPE). The fabrication process begins with the deposition of a Ti/Au (30/200 nm) backside electrode via evaporation, followed by annealing at 475 °C for 1 minute in a nitrogen (N_2) atmosphere to form a low-resistance Ohmic contact. Subsequently, a 250 nm-thick p-type NiO layer with a doping concentration of 8×10^{17} cm^{-3} (determined via hall measurement) is deposited on the Ga_2O_3 surface by RF magnetron sputtering. The deposition was carried out using a 99.99% pure NiO_x target under an applied RF power of 150 W and a chamber pressure of 3 mTorr. An Ar:O_2 gas flow ratio of 12:1 was employed to achieve the desired hole concentration, resulting in a deposition rate of approximately 1.2 nm/min. Finally, an anode Schottky contact is deposited with Ni/Au (50/250 nm) by electron beam evaporation.

Based on the fabricated Ga_2O_3 SBDs and HJBS, the electrical characteristics and high-temperature stability of these devices are investigated. Figure 2(a)-2(d) show the temperature-dependent forward current density (J_F)–forward voltage (V_F) characteristics and corresponding specific on-resistance ($R_{on,sp}$) of the Ga_2O_3 SBDs and HJBS, respectively, measured using the PULSE IV mode of the Keysight B1500A semiconductor parameter analyzer. The pulse conditions (100 μs width, 10 ms period) effectively suppressed self-heating, as evidenced by the nearly constant $R_{on,sp}$. A slight increase beyond 3 V is attributed to the relatively high thermal resistance of the small anode with only 50 μm radius. As the temperature

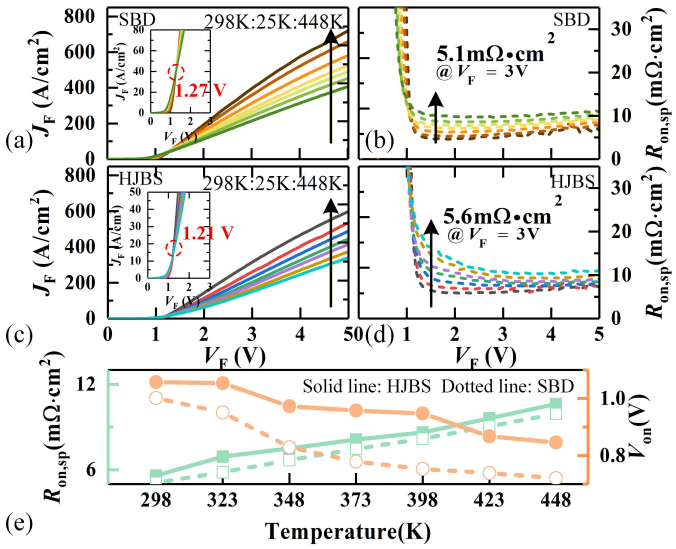


图 2: Temperature dependence of forward J_F-V_F characteristics and the corresponding $R_{on,sp}$ curves of (a), (b) Ga_2O_3 SBD and (c), (d) Ga_2O_3 HJBS diode. (e) Extracted V_{on} and $R_{on,sp}$ versus temperature (solid line: Ga_2O_3 HJBS diode; dashed line: Ga_2O_3 SBD).

(T) increased from 298 K to 448 K, the J_F at V_F=5 V decreased from 713 A/cm^2 to 402 A/cm^2 for the Ga_2O_3 SBDs, and from 600 A/cm^2 to 344 A/cm^2 for the Ga_2O_3 HJBS. The zero-temperature-coefficient (ZTC) points of the Ga_2O_3 SBD and HJBS diodes are 1.27 V and 1.21 V, respectively. The corresponding temperature dependence of $R_{on,sp}$ (extracted at $V_F = 3$ V) and V_{on} (extracted by linear extrapolation method) are summarized in Figure 2(e). As the T increases from 298K to 448K, the V_{on} of Ga_2O_3 SBDs decreased from 0.98 V to 0.72 V, while its $R_{on,sp}$ increased from 5.1 to 9.9 m$\Omega \cdot cm^2$. For the Ga_2O_3 HJBS, V_{on} decreased from 1.09 V to 0.85 V, and $R_{on,sp}$ increased from 5.6 to 10.5 m$\Omega \cdot cm^2$, indicating that its high-temperature current capability is comparable to that of SBDs.

Figure 3(a) shows the breakdown voltages (BV) measured by a Keysight B1505A high-voltage semiconductor parameter analyzer. Owing to the edge termination designed by TCAD simulation, the BV of Ga_2O_3 SBD is significantly improved from 500V to 1kV, while the Ga_2O_3 HJBS (W Ter) further exhibited a higher BV of 1.55 kV. On the one hand, the p-NiO junction termination extension and field-limiting rings (FLRs) broaden the depletion region, increase the radius of curvature, and thereby significantly mitigate the electric field crowding at the edge termination. On the other hand, the depletion extension of the NiO/Ga_2O_3 heterojunction in the cell region effectively clamps the leakage through the Metal/Ga_2O_3 interface, thus alleviating both the image-force barrier lowering effect and tunneling leakage at the Schottky junction surface. The electric field modulation mechanism of the designed edge termination is performed by TCAD simulations. Figure 3(b) illustrates the surface electric field distributions of the Ga_2O_3 SBDs without termination (w/o Ter), with termination (w Ter), along with the electric field contours of Ga_2O_3 SBDs with Ter under a reverse bias (V_R) of 0.5 kV. The result shows that the edge termination effectively shifts the peak electric field (E_{peak}) from the anode edge to JTE edge, and reduces its magnitude from

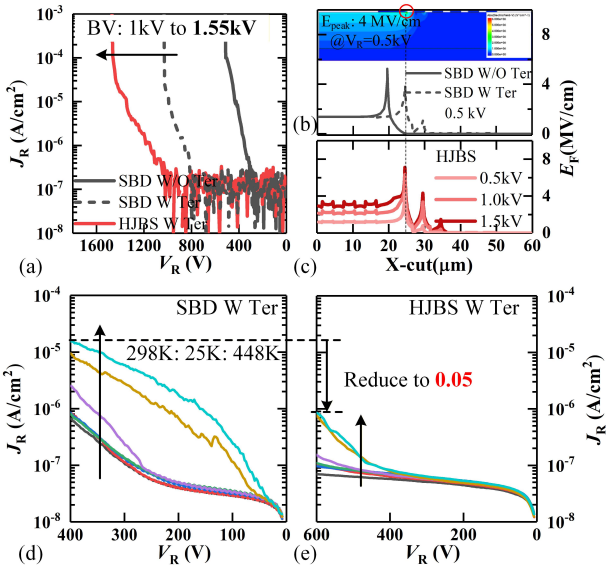


图 3: (a) Log-scale breakdown characteristics. (b) The surface electric field distribution of Ga_2O_3 SBDs without Ter and with Ter under V_R=0.5 kV. (inset: electric field contours of Ga_2O_3 SBDs with Ter.) (c) The surface electric field distribution of Ga_2O_3 HJBS with Ter under V_R=0.5, 1, 1.5 kV. Temperature dependence of J_R-V_R characteristics from 298K to 448K: (d) Ga_2O_3 SBDs, (e) Ga_2O_3 HJBS.

5.8 MV/cm to 4 MV/cm. And Figure 3(c) illustrates the surface electric field distributions of the Ga_2O_3 HJBS with Ter under a reverse bias (V_R) of 0.5, 1, 1.5 kV. The corresponding E_{peak} at the JTE edge are 4, 6, and 7 MV/cm, respectively, all of which are below the critical breakdown field of Ga_2O_3(8 MV/cm). In addition, the reverse leakage (J_R) characteristics under elevated temperatures are also evaluated in Figure 3(d) and 3(e). As the T increased from 298 K to 448 K , the J_R (at $V_R = -400V$) of the Ga_2O_3 SBD significantly degraded from 7×10^{-5} A/cm^2 to 2×10^{-3} A/cm^2. In contrast, J_R (at $V_R = -600V$) of the Ga_2O_3 HJBS increased from 8.5×10^{-6} A/cm^2 to only 1×10^{-4} A/cm^2 , which is merely 0.05 times that of the SBDs. The above results indicate that under elevated temperatures, Ga_2O_3 HJBS exhibits more stable electrical characteristics compared to Ga_2O_3 SBD.

3. The Degradation Behaviors and Mechanisms

Accordingly, the subsequent focus is on investigating the reliability and degradation mechanisms of Ga_2O_3 HJBS under pulsed forward bias (PFB) and HTRB stresses. Firstly, the degradation behavior under PFB stress is investigated. As shown in Figure 4(a), the 5 V PFB stress, with a pulse width of 100 μs and a period of 10 ms, effectively suppresses self-heating. The pulsed J_F-V_F (PIV) characterization is performed under the same conditions as previously described. All measurements are conducted at room temperature by placing the device on the probe station chuck, while the PFB stress and PIV modules of the B1500A are switched rapidly during the process. After PFB stress, the hysteresis pulsed J_F-V_F characteristics of the Ga_2O_3 HJBS is presented in Figure 4(b). The Ga_2O_3 diode exhibits a constant

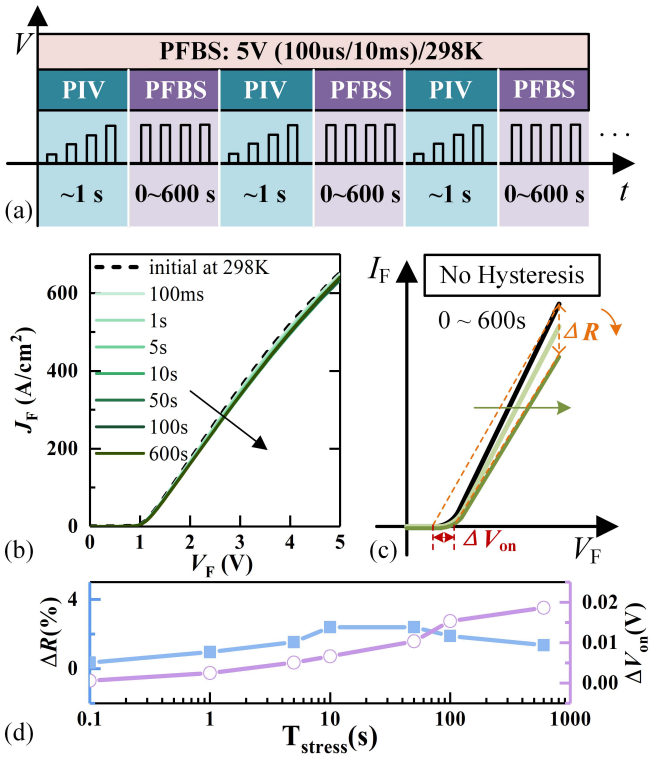


图 4: (a) The test scheme of PFB stress, (b) the pulsed J_F-V_F characteristics measured after PFB stress, (c) schematic of the degradation process, (d) extracted ΔR and V_{on} from (b).

resistance once turned on, thereby ensuring that self-heating and temperature-induced variations in electrical characteristics are effectively eliminated during PFB stress testing. The forward and reverse sweep J_F-V_F curves show negligible hysteresis, while a slight degradation in J_F and a gradual increase in V_{on} are observed with increasing stress time (T_{stress}). The corresponding degradation schematic is illustrated in Figure 4(c), where the degradation in V_{on} is denoted as $\Delta V_{on} = V_{on,afterstress} - V_{on,initial}$, extracted via the linear extrapolation method. Meanwhile, the relative degradation in current capability at V_F=5 V is defined as $\Delta R = R_{afterstress} - R_{intial}$, based on the dynamic resistance relation $R = (V_F - V_{on})/I_F$. As shown in Figure 4(d), the extracted ΔV_{on} is only 0.02 V, and ΔR increased by merely 1.4%, both of which are in stark contrast to the severe current degradation exceeding 10% and the V_{on} reduction of more than 0.5 V reported in Ref. [30–32]. This indicates that the degradation mechanism under PFB stress differs from that under DC forward bias (DFB) stress.

Subsequently, the degradation of Ga_2O_3 HJBS under HTRB stress is investigated. Figure 5(a) illustrates the stress scheme, where the diodes are tested at 448 K under a V_R of –600 V applied using the Keysight 2410 source meter. After each stress interval, the measurement is rapidly switched to the PIV module of the B1500A within 1s. The hysteresis pulsed J_F-V_F (PIV) characteristics under identical pulse conditions as PFB stress (100 μs width, 10 ms period) and the corresponding degradation schematic after HTRB are shown in Figs. 5(b) and 5(c), respectively. The extracted method of ΔR and ΔV_{on} is consistent with that described previously. The reverse sweep current in each PIV scan is significantly higher than the forward sweep current, and its value remains consistently lower than the initial before the

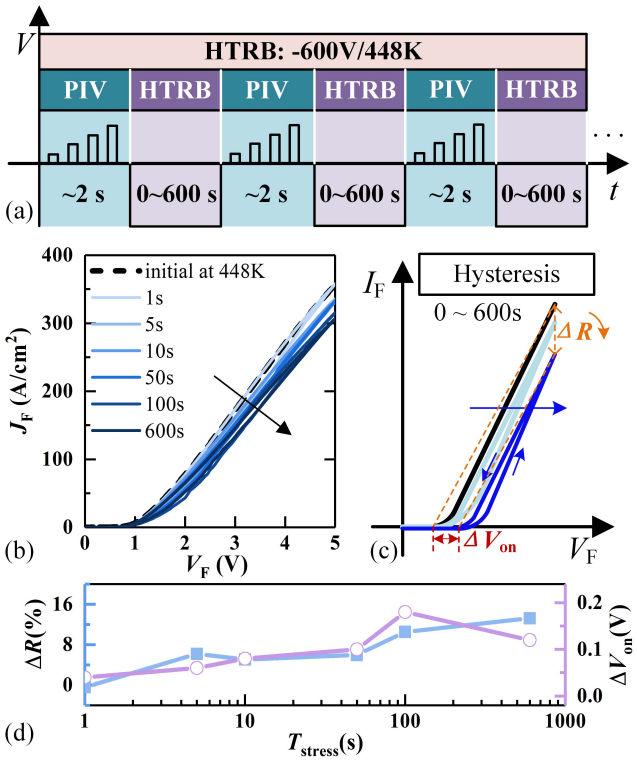


图 5: (a) The test scheme of HTRB stress, (b) the pulsed J_F-V_F characteristics measured after HTRB, (c) schematic of the degradation process, (d) extracted ΔR and V_{on} from (b).

HTRB stress. This behavior differs from the nearly hysteresis-free J_F-V_F characteristics observed after PFB stress, and is presumed to arise from partial recovery of degradation at elevated temperatures. After 600 s' HTRB stress, the ΔR degraded by as much as 13%, and the ΔV_{on} increased by 0.12 V (11%), as shown in Figure 5(d), which is comparable to the results reported in [35], where ΔR degraded by 10% and ΔV_{on} increased by 17% after -600 V/298 K stress for 600 s.

To further elucidate the degradation mechanisms of the device under PFB and HTRB stresses, its recovery behavior was characterized, as illustrated in Figure 6. Under PFB stress, the Ga_2O_3 HJBS exhibited complete recovery of its current capability within 200s. Moreover, the recovery rate accelerated as the temperature increased from 293K to 303K, suggesting that the PFB-induced degradation is dominated by shallow-level traps with an emission time constant (τ_e(PFB)) of less than 200s. Actually, the presence of traps is ubiquitous throughout the fabrication process of Ga_2O_3 power devices. For instance, oxygen vacancies (V_O) formed during high-temperature epitaxial growth, or extrinsic defects introduced by microfabrication steps, particularly dry etching, which often induces localized lattice damage and amorphous surface layers [1]. Furthermore, the deposition of dielectrics (such as p-NiO_x) and subsequent thermal processing can exacerbate interface state density, collectively contributing to the observed electrical instability and dynamic performance degradation [2]. In contrast, after 600 V HTRB stress for 600 s at temperatures ranging from 398 K to 448 K, the current capability showed almost no recovery under dark conditions. This initial observation suggested that the HTRB-induced degradation might be associated with deep-level traps or even permanent degradations (such as lattice damage). To clarify the under-

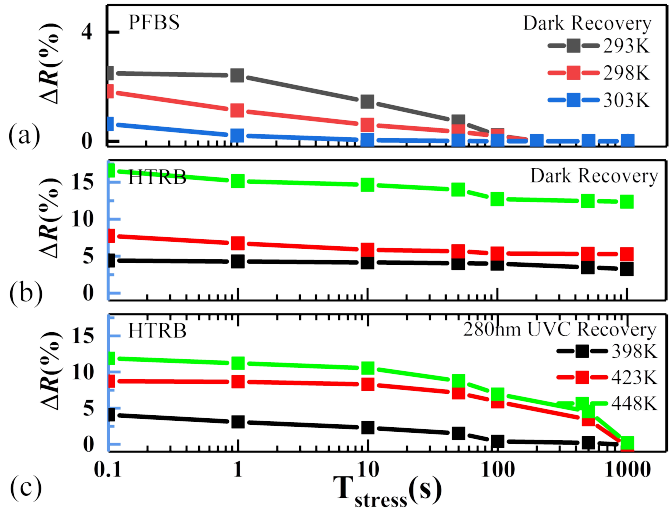


图 6: The current capability recovery behavior of the Ga_2O_3 HJBS after (a) $5V$/600s PFB stress at 293K, 298K, 303K in dark conditions, and (b) $600V$/600s HTRB stress at 398K, 423K, 448K under dark conditions or (c) 280nm UVC LED illumination.

lying physical origin, UVC LED illumination (280 nm, $70\mu W/cm^2$) was applied. The device achieved full recovery within 1 ks, where the photon energy (4.43 eV) was sufficient to excite and de-trap the captured electrons back into the conduction band [45,46]. This complete restoration rules out permanent structural damage and confirms that the HTRB-induced degradation is dominated by deep-level acceptor traps ((τ_e(HTRB)) $>$ 1ks). Thanks to the effective mitigation of self-heating, the trap dynamics induced by electrical stress are believed to be primarily voltage- and current-driven. Accordingly, the following section elucidates the degradation mechanism by analyzing the evolution of the energy band structure before and after stress application.

The energy band diagrams of the device subjected to PFB and HTRB stresses are presented in Figure 7 and Figure 8, respectively. As shown in Figure 7(a), the initial barrier height and width are represented by $q\varphi_{bi}$ and W_d, which are determined by the work function of anode metal and the interface trap states at the Ga_2O_3 surface. Numerous studies have reported the existence of trap states at the Ga_2O_3 surface [25–28], with energy levels above $q\varphi_0$ corresponding to acceptor-like traps and those below $q\varphi_0$ to donor-like traps, whose activation rates are determined by their positions relative to the Fermi energy level (E_F). As shown in Figure 7(b), under 5 V PFB stress, a downward bending of the Ga_2O_3 surface energy band, which is confined within a narrow region of approximately 36 nm (determined by $W_b = \sqrt{\varepsilon_0\varepsilon_r k_B T/q^2 N_d} \approx 36$nm). This indicates that the degradation primarily occurs near the Ga_2O_3 interface, where the E_F above the energy levels of the near-interface acceptor-like traps, leading to electron trapping. As shown in Figure 7(c), When the PIV test is performed immediately after the PFB stress, the acceptor-like traps have not yet released electrons, resulting in an increase in the barrier height and width, which ultimately leads to a rise in V_{on} and a reduction in R. This is believed to be the most likely degradation mechanism under PFB stress.

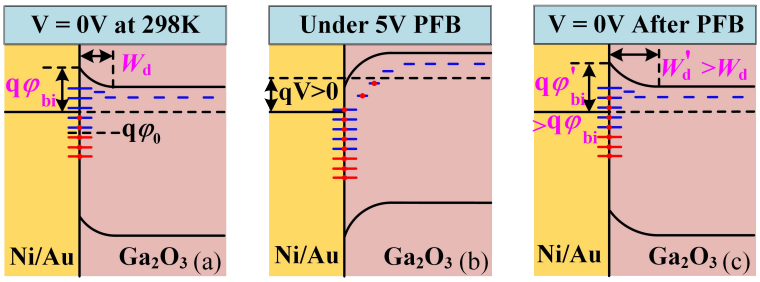


图 7: Energy band diagrams of the Ga_2O_3 surface under (a) 0 V at 298K, (b) 5 V PFB stress, (c) 0 V after PFB stress.

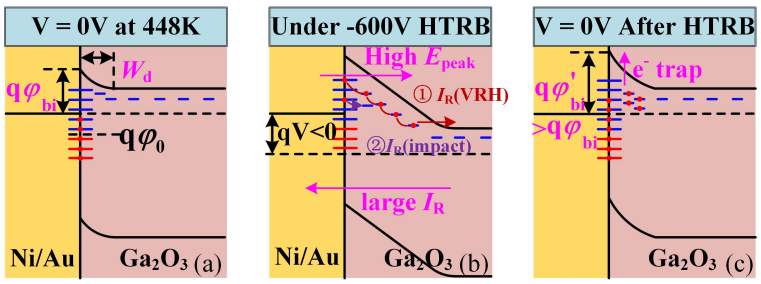


图 8: Energy band diagrams of the Ga_2O_3 surface under (a) 0 V at 448K, (b) -600 V HTRB stress, (c) 0 V after HTRB stress.

Then, an analysis of the HTRB degradation mechanism, based on the energy band diagram, is illustrated in Figure 8. As shown in the initial band diagram at 448 K in Figure 8(a), the elevated temperature enhances the thermal emission of electrons from the interface trap states and increases the intrinsic carrier concentration owing to the bandgap narrowing. Consequently, the effective barrier height is reduced, which is consistent with the observed temperature dependence of the V_{on} shown in Figure 2(e). As shown in Figure 8(b), under –600 V HTRB stress, the energy band of Ga_2O_3 surface exhibits a pronounced upward band bending. Due to the nearly unchanged E_F, the qφ_0 at the Ga_2O_3 surface shifts closer to the E_F, which causes the acceptor-like traps above E_F to release the captured electrons. However, the V_{on} degradation after HTRB stress is more severe than that observed after PFB, presumably due to the formation of additional acceptor-like traps capture electrons near the Ga_2O_3 surface between the qφ_0 and the E_F. This is possibly caused by the enhanced leakage current at elevated temperatures, which undergoes impact ionization under the strong surface electric field (determined by $E_{surf} = \sqrt{2qN_d.V_R/\varepsilon_r\varepsilon_0}$ =1.75 MV/cm), thereby aggravating the density of surface state defects. Apart from a slight increase in the V_{on}, the R exhibits significant degradation, which is considered to indicate that the degradation after HTRB stress does not merely occur at the Ga_2O_3 surface. In this state, the drift region is fully depleted ($W_D = \sqrt{2\varepsilon_r\varepsilon_0.V_R/qN_d}$ =6.96 μm), allowing electrons to be captured by acceptor-like bulk traps [39–42], which possibly leads to a significant degradation in R.

According to the previous discussion, the degradation behaviors under PFB and HTRB stresses are considered to be dominated by acceptor-like traps. To further verify this, capacitance–voltage (C–

V) analysis is conducted using the Tonghui TH513 semiconductor C–V analyzer. The RC equivalent circuit [47] considering acceptor-like traps effects is shown in Figure 9 (a). The corresponding formula for total capacitance is expressed as C_{total}=C_{d}+$C_{\text{it}}/(1+(2\pi f\tau_{\text{it}})^2)$+$C_{\text{bt}}/(1+(2\pi f\tau_{\text{bt}})^2)$, where C_d denotes frequency-independent capacitances such as the Schottky junction capacitance and the p-NiO/n-Ga_2O_3 junction capacitance, and R_d represents the diode resistance. C_{it} and C_{bt} correspond to the capacitances associated with near-interface and bulk acceptor-like traps, while R_{it} and R_{bt} represent the resistances used for calculating the corresponding traps' time constants (e.g., $R_{\text{it}} = \tau_{\text{it}}/C_{\text{it}}$). Based on this formula, it can be inferred that when acceptor-like traps capture electrons, the depletion region expands, leading to a reduction in the effective C_{it}, C_{bt} and C_{total}. Furthermore, as the frequency f gradually increases, the term $C_{\text{it}}/(1+(2\pi f\tau_{\text{it}})^2)$ continuously decreases, resulting in a gradual reduction of C_{total}. As presented in Figure 9(b), the capacitance of Ga_2O_3 HJBS continuously shifts downward with increasing HTRB stress time. After 600 s stress, C at $V_{\text{R}} = 0\ V$ decreases from 62 nF/cm^2 to 38 nF/cm^2, indicating a significant increase in the near-interface trap density [48–50]. By comparing C at the initial state and after 100 s, the increased interface trap density (ΔN_{it}) is estimated to be approximately 1.11×10^{12} cm^{-2}. Moreover, the capacitance difference (ΔC) between the 100 s and 600 s curves increases from 15.5 nF/cm^2 to 19.8 nF/cm^2 as V_{R} rises from 0 V to 100 V. This indicates the occurrence of a pronounced bulk trap capture effect, with the bulk trap concentration calculated as

$$\Delta N_{bt} = \frac{1}{qd}\int_{0\ \text{V}}^{100\ \text{V}} \Delta C(V)\,dV = 4.2\times10^{15}\ \text{cm}^{-3},$$

where d represents the depletion region width of 2.82 μm at $V_{\text{R}} = 100\ V$. As presented in Figure 9 (C), the C–V measurements are performed by sweeping the bias voltage from +1 V to –600 V across a frequency range of 100 kHz to 1.5 MHz to investigate the frequency dispersion behavior. As the frequency increases, the entire C–V curve shifts downward, indicating an increased density determined by $\Delta N_{\text{it}}(1\ \text{M} < f < 1.2\ \text{M}) = C.\Delta V/q = 1.28\times10^{12}$ cm^{-2}. Moreover, the increasing gap between adjacent frequency curves implies that the dominant trap response frequency (f_{it}) exceeds at least 1.2 MHz, which explains the pronounced current hysteresis observed after HTRB stress. Therefore, under PFB stress, although the high-density near-surface acceptor-like traps capture electrons, their rapid emission results in only 0.02 V in ΔV_{on} and 1.4% reduction in ΔR. In contrast, under HTRB stress, the combined effects of elevated temperature and high electric field drive electrons to transfer from near-surface acceptor traps to bulk traps, thereby resulting in 0.12 V ΔV_{on} degradation and a 13% reduction in ΔR. These findings suggest that Ga_2O_3 diodes still suffer from a considerable density of acceptor-type traps.

To further investigate the electrons transition process from near-surface acceptor traps to bulk traps under HTRB stress, the leakage mechanism was first studied over the temperature (T) range of 398 K–498 K first, as shown in Figure 10 (a). The J_{R} increases sharply and exhibits an obvious temperature dependence at V_{R} above 360 V, indicating that the leakage mechanism has changed [43,44]. To investigate the leakage mechanism at V_{R} exceeding 360 V, the relationships between J_{R}, surface electric field (E), and T are shown in Figure 10 (b) and Figure 10 (c). The results indicate that when the E exceeds 1.4 MV/cm (corresponding to $V_{\text{R}} = 380\ V$), the ln(J_{R}) versus E shows a linear dependence. Moreover,

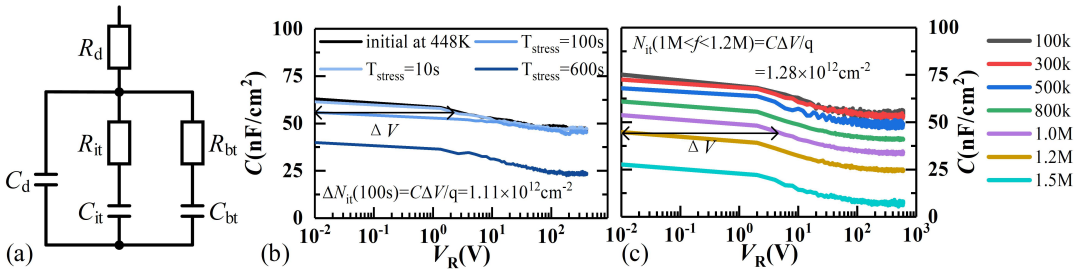


图 9: (a) The RC equivalent circuit of Ga_2O_3 HJBS. (b) C–V characteristics measured at 1 MHz: initial at 448 K before HTRB stress, and 10 s, 100 s, 600 s after HTRB stress. (c) C–V characteristics measured from 100 kHz to 1.5 MHz.

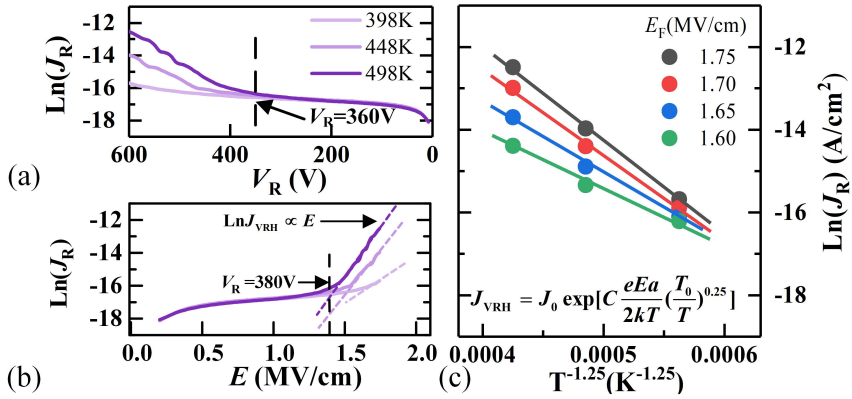


图 10: (a) J_R-V_R characteristics in a log plot and (b) ln(J_R)-surface electric field (E) in a semilog plot at 398 K to 498 K. (c) ln(J_R)- $T^{-1.25}$ at the E of 1.60, 1.65, 1.70, 1.75 MV/cm.

ln(J_R) also varies linearly with $T^{-1.25}$, which can be described by the following expression for the variable-range hopping (VRH) mechanism: $J_{VRH}=J_0 \cdot \exp[C\frac{eEa}{2KT} \cdot (T_0/T)^{1/4}]$. In this formula, J_0 is the low-field current density, C is a constant, a is the localization radius of the electron wave function, and T_0 is a characteristic temperature parameter [41,43]. This confirms that the leakage mechanism of the Ga_2O_3 HJBS under 600 V/448 K HTRB stress is dominated by the variable-range hopping (VRH) process and the presence of buffer traps in the Ga_2O_3 drift region.

In conclusion, this study demonstrates that the degradation mechanisms of Ga_2O_3 HJBS under PFB and HTRB stresses are dominated by near-surface shallow-level acceptor-like traps and bulk-related deep-level traps, respectively. Under PFB stress, electrons are captured by shallow-level acceptor traps near the surface, causing slight increases in V_{th} of 0.02 V and R_{on} of 1.4%, which exhibit rapid recovery within 200 s under dark conditions. In contrast, under HTRB stress, the combination of high surface electric fields and elevated temperatures induces an increase in near-surface traps. These electrons are subsequently captured by bulk traps via the variable-range hopping (VRH) mechanism, resulting in severe degradation in V_{th} of 0.12 V and R_{on} of 13%, which shows no sign of recovery even after 1000 s under dark conditions. Therefore, future efforts must focus on mitigating trap effects to enhance Ga_2O_3 device performance.

For example, shallow-level acceptor traps (e.g., Ga_O), typically located at $E_c - 0.2$ to $E_c - 0.7$ eV, arise from interface states at dielectric/semiconductor heterojunctions. These can be suppressed by optimizing MBE growth flux or utilizing in-situ PEALD combined with post-deposition annealing [52,53]. Conversely, deep-level traps ($< E_c - 0.7$ eV), often associated with V_O or V_{Ga}, govern long-term reliability and leakage. Mitigating these deep defects requires ultra-high-purity precursors and high-temperature oxygen-ambient annealing to promote lattice reconstruction [51–54]. These improvements will significantly enhance the robustness of Ga_2O_3 power diodes and strengthen their competitiveness in power electronic systems.

4. Conclusion

In this letter, a minor positive threshold voltage (V_{th}) shift of 0.02 V and a 1.4% increase in on-resistance (R_{on}) under pulsed forward bias (PFB) stress, alongside a severe positive V_{th} shift of 0.12 V and a 13% rise in R_{on} under high-temperature reverse bias (HTRB) stress, are demonstrated in a 1.55 kV Ga_2O_3 HJBS. Current and capacitance characterization reveal that the degradation under PFB stress is caused by the fast capture and emission dynamics of acceptor-like interface traps. In contrast, under HTRB stress, the high surface electric field induces an increase in near-interface traps, which are subsequently captured by bulk traps via variable-range hopping (VRH). This work provides critical insights for trap states distribution information and reliability optimized design of Ga_2O_3 power devices.

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