

Spiking activity in a meminductive and memristive emulator-based bionic circuit

Chengyu Zhang(张晨宇), Weiwei Fan(范伟伟), Huagan Wu(武花干), Ning Wang(王宁), Mo Chen(陈墨), Yibing Wang(王一冰), and Quan Xu(徐权)

Citation: Chin. Phys. B, 2026, 35 (**6**): 068707. DOI: 10.1088/1674-1056/ae4c72
http://cpb.iphy.ac.cn; http://iopscience.iop.org/cpb

What follows is a list of articles you may be interested in

Effect of 3.1-THz radiation on pathological progression in *Caenorhabditis elegans* Alzheimer's disease model

Lei Wang(王磊), Meng Wang(王萌), Xumei Zhang(张绪梅), and Mingxia He(何明霞)
Chin. Phys. B, 2025, 34 (**11**): 118702. DOI: 10.1088/1674-1056/ade06a

Computational model investigating the effect of magnetic field on neural-astrocyte microcircuit

Li-Cong Li(李利聪), Jin Zhou(周瑾), Hong-Ji Sun(孙洪吉), Peng Xiong(熊鹏), Hong-Rui Wang(王洪瑞), Xiu-Ling Liu(刘秀玲), and Chang-Yong Wang(王常勇)
Chin. Phys. B, 2021, 30 (**6**): 068702. DOI: 10.1088/1674-1056/abea81

Continuous non-autonomous memristive Rulkov model with extreme multistability

Quan Xu(徐权), Tong Liu(刘通), Cheng-Tao Feng(冯成涛), Han Bao(包涵), Hua-Gan Wu(武花干), and Bo-Cheng Bao(包伯成)
Chin. Phys. B, 2021, 30 (**12**): 128702. DOI: 10.1088/1674-1056/ac2f30

Polarization conversion metasurface in terahertz region

Chen Zhou(周晨), Jiu-Sheng Li(李九生)
Chin. Phys. B, 2020, 29 (**7**): 078706. DOI: 10.1088/1674-1056/ab9295

Adjustable polarization-independent wide-incident-angle broadband far-infrared absorber

Jiu-Sheng Li(李九生), Xu-Sheng Chen(陈旭生)
Chin. Phys. B, 2020, 29 (**7**): 078703. DOI: 10.1088/1674-1056/ab8892

SPECIAL TOPIC — Biophysical circuits: Modeling & applications in neuroscience

Spiking activity in a meminductive and memristive emulator-based bionic circuit

Chenyu Zhang(张晨宇), Weiwei Fan(范伟伟), Huagan Wu(武花干), Ning Wang(王宁), Mo Chen(陈墨), Yibing Wang(王一冰), and Quan Xu(徐权)†

Wang Zheng School of Microelectronics, Changzhou University, Changzhou 213159, *China*

(Received 3 February 2026; revised manuscript received 22 February 2026; accepted manuscript online 3 March 2026)

Bionic circuits can reproduce the firing activities of excitable biological neurons, which are the potential hardware foundation for artificial intelligent applications. This paper builds a meminductive and memristive emulator-based bionic circuit by referring to the electrophysiological microstructure of the lipid bilayer membrane of a biological neuron, within which an S-type memristor and a flux-controlled meminductor are employed to characterize the ion channels and their internal electromagnetic induction, respectively. The schematic of the bionic circuit only involves a capacitor, a memristor, a meminductor, and an external direct current (DC) source. Numerical simulations demonstrate that the bionic circuit can generate abundant chaotic and periodic spiking activities for the external stimulus, memristor-, and meminductor-related parameters. Moreover, a printed circuit board (PCB)-based hardware circuit is manually fabricated, upon which experimental measurements are performed to verify the chaotic and periodic spiking activities. This exploration demonstrates the feasibility of the bionic circuit in generating spiking activities and provides a hardware foundation for spike-based applications.

Keywords: spiking activity, meminductive emulator, memristive emulator, bionic circuit

PACS: 87.50.–a, 87.19.ll, 87.23.Kg, 87.19.ln

DOI: 10.1088/1674-1056/ae4c72 **CSTR:** 32038.14.CPB.ae4c72

1. Introduction

Spiking activity is the foundation for information integration and transmission in biological systems, which has attracted extensive attention in spike-based applications.[1,2] Scientists have expressed great concern about the generation and regulation of neuron-like spiking activities, although they cannot replicate the spiking activities of biological neurons.[3,4] From the circuit dynamics viewpoint, bionic circuits have been built by referring to the neuronal functionalities or the electrophysiological microstructure of biological neurons, which can equivalently express the process of electrical signal processing in biological neurons.[5,6]

Bionic circuits can be designed by equivalently realizing existing neuron models,[7,8] directly building via consideration of microstructure,[9,10] and macroscopically constructing via consideration of neuronal functionality.[11,12] In the literature, discrete circuit components,[6] CMOS-based technology,[13] and field-programmable gate array (FPGA)- and STM32 microcontroller-based digital platforms[14,15] were frequently employed to implement these bionic circuits to reproduce spiking activities. In recent years, physical mem-elements were deployed to build bionic circuits with a combination of discrete circuit components or CMOS-based technology.[16] These approaches have the features of high integration and low energy consumption, since mem-elements possess nano-scale structures.[17]

To date, physical memristors have been employed to construct bionic circuits to realize different neuronal functionalities. These include a Mott memristor to implement an afferent nerve,[18] a diffusive memristor to achieve a spiking circuit,[19] a locally active memristor (LAM) to build a super-reduced neuron circuit,[20] and a stacked memristor for a leaky integrate-and-fire circuit,[21] among others. Moreover, physical memcapacitors have been employed to build bionic circuits to reduce static energy, including a ferroelectric memcapacitor for multilevel operation,[22] a hafnium oxide-based memcapacitor array for neuromorphic computing,[23] a memcapacitive device for self-powered electronics,[24] and an analog memcapacitive device for spiking neuromorphic systems.[25] Lagging behind the development of memristive and memcapacitive devices, meminductive devices have been deployed in neuromorphic computing.[26] Owing to the commercial unavailability of physical mem-elements, using mem-element emulators to design bionic circuits[27,28] and to perform verification experiments is a feasible approach.[29,30]

LAM is a special kind of memristor, which possesses the prominent features of a locally active domain with negative differential conductance and the edge of chaos. These features are the origin of spiking activity. LAMs contain S-type (current-controlled) and N-type (voltage-controlled)

†Corresponding author. E-mail: xuquan@cczu.edu.cn

© 2026 Chinese Physical Society and IOP Publishing Ltd. All rights, including for text and data mining, AI training, and similar technologies, are reserved.

ones.[31] From the circuit modeling viewpoint, S-type LAMs are frequently connected in a branch with a known current, while N-type LAMs are often connected with a known voltage. In previous literature, locally active memristors were deployed to characterize the electrophysiological properties of ion channels by employing their plasticity to construct bionic circuits, including memristive Hodgkin–Huxley circuits,[32] Morris–Lecar circuit,[33] and Wilson circuit, etc. In addition, LAMs were used to build a memristor synapse-based neural network.[34,35] These studies indicate that LAMs share similar dynamical properties with biological ion channels and synapses.

The meminductor restricts the constitutive relation between current and flux, thereby having current-controlled and flux-controlled types.[36] Meminductors have been used to construct chaotic circuits in a general approach.[37] High-frequency CMOS meminductors with high operating frequency and low power consumption were developed, demonstrating the integrability of meminductors in electronic circuits.[13,38] In addition, charge-controlled meminductors have been realized using a second-generation current conveyor (CCII) and differential-output second-generation current conveyor (DO-CCII) as core active components.[39] A compact electronically tunable meminductive emulator based on metal–oxide–semiconductor field-effect transistor-capacitor (MOSFET-C) technology has been designed, which can be used in adaptive learning bionic circuits and mimic behavioral responses of amoeba under varying environments such as temperature.[40] Besides, multiplier-free floating and grounded charge-controlled meminductive emulators have been proposed by employing CDTA and VDCC, which have the features of low component count and ease of integration, highlighting their applicability to neuromorphic computing.[41] These meminductive emulators are equivalently implemented, which is different from meminductive devices.[26] These meminductive emulators and devices exhibit sensitivity to flux, which can emulate electromagnetic induction effects according to Maxwell's electromagnetic theory. Recent theoretical studies have shown that electromagnetic induction can significantly modulate neuronal firing rhythms and membrane potential evolution.[42–45] Thus, this paper employs a meminductor to characterize electromagnetic induction inside ion channels.

Biological neurons respond to external stimuli. In theoretical studies, dynamical behaviors and firing patterns for direct current (DC), alternating current (AC), pulse, and noise inputs were explored in neuron models and bionic circuits. Fast–slow dynamics for bursting, stochastic resonance, and regular bifurcation routes were investigated via numerical simulations and experimental measurements. Moreover, previous studies have explored improved neuron models capable of reasonably representing electromagnetic induction effects, i.e., a modified discrete Rulkov neuron model coupled with memristors to describe electromagnetic induction effects.[46] These investigations enrich neuronal dynamics and enable flexible modulation of firing patterns, which inspires more comprehensive modeling of bionic circuits.

The main content of this paper is organized as follows. Section 2 presents the modeling of the meminductive and memristive emulator-based bionic circuit. Section 3 reveals dynamical behaviors and spiking activities associated with an external DC stimulus, memristor- and meminductor-related parameters via double- and single-parameter bifurcation diagrams, Lyapunov exponents, and time-domain waveforms. Section 4 implements a printed circuit board (PCB)-based analog hardware circuit and conducts experimental measurements to validate the numerical results. Finally, conclusions are drawn in Section 5.

2. Modeling of the meminductive and memristive emulator-based bionic circuit

This section proposes an S-type memristive emulator and a flux-controlled meminductive emulator and then investigates their properties. After that, the meminductive and memristive emulator-based bionic circuit is built, and its circuit state equations are modeled.

2.1. Memristive and meminductive emulators

Figure 1 shows the circuit schematic of the memristor emulator and the meminductor emulator. Figure 1(a) is for the S-type (current-controlled) memristive emulator, which contains a current-feedback operational amplifier (C-FOA) U_1, an inverting integrator module implemented via operational amplifiers (op-amps) $U_{\rm A}$, and four analog multiplier modules M_1 to M_4. The S-type memristive emulator includes an integration capacitor C_1 whose terminal voltage v_σ represents the internal state variable of the S-type memristor. The circuit state equation of the S-type memristor can be expressed as

$$\begin{cases} v_{\rm M} = g_4(g_2 v_\sigma^2 - E_{\rm M}) i_{\rm M} R_{\rm M}, \\ C_1 \dfrac{{\rm d}v_\sigma}{{\rm d}t} = \dfrac{g_1 i_{\rm M}^2 R_{\rm M}^2}{R_1} - \dfrac{g_2 v_\sigma^2}{R_2} - \dfrac{g_3 v_\sigma i_{\rm M} R_{\rm M}}{R_3}, \end{cases} \tag{1}$$

where $i_{\rm M}$ and $v_{\rm M}$ denote the input current and the across voltage of the memristor, respectively. g_1 to g_4 are the voltage gains of multipliers M_1 to M_4. The memristive function is $M = g_4(g_2 v_\sigma^2 - E_{\rm M})R_{\rm M}$. Typical parameters of the S-type memristive emulator are $g_1 = g_2 = g_3 = g_4 = 1\ {\rm V}^{-1}$, $R_1 = R_2 = 10\ {\rm k\Omega}$, $R_3 = 5\ {\rm k\Omega}$, $C_1 = 10\ {\rm nF}$, $R_{\rm M} = 1.5\ {\rm k\Omega}$, and $E_{\rm M} = 0.5\ {\rm V}$.

Figure 1(a) displays the circuit schematic of the meminductive emulator, which comprises a floating module composed of C-FOAs U_2 to U_4, two inverting integrators implemented by op-amps $U_{\rm A}$ and $U_{\rm B}$, and two analog multipliers M_5 and M_6. The floating module allows the meminductor to

be connected in series without ground limitation. The flux-controlled meminductor includes two integration capacitors C_2 and C_3. The across voltage $v_{\varphi L}$ of C_2 represents the internal flux of the meminductor, while the across voltage v_γ of C_3 stands for its internal state variable. The circuit state equation of the meminductor can be written as

$$\begin{cases} i_{\rm L} = \dfrac{g_6(g_5 v_\gamma^2 - E_{\rm L})v_{\varphi L}}{R_{\rm L}}, \\ C_2 \dfrac{{\rm d}v_\gamma}{{\rm d}t} = \dfrac{v_{\varphi L}}{R_4} - \dfrac{v_\gamma}{R_5}, \\ C_3 \dfrac{{\rm d}v_{\varphi L}}{{\rm d}t} = \dfrac{v_{\rm L}}{R_6}. \end{cases} \tag{2}$$

Here, $v_{\rm L}$ and $i_{\rm L}$ are the across voltage and input current of the meminductor. g_5 and g_6 are the voltage gains of multipliers M_5 and M_6, respectively. The meminductive function is given by $L_{\rm M} = g_6(g_5 v_\gamma^2 - E_{\rm L})/R_{\rm L}$. Typical parameters of the flux-controlled meminductive emulator are $g_5 = g_6 = 1\ {\rm V}^{-1}$, $R_4 = R_5 = R_6 = 10\ {\rm k\Omega}$, $C_2 = C_3 = 10$ nF, $R_{\rm L} = 1.5\ {\rm k\Omega}$, and $E_{\rm L} = 0.5$ V.

Denote $i_{\rm M}$ and $v_{\rm M}$ as $I_{\rm M}$ and $V_{\rm M}$, and substitute them into Eq. (1), the DC V–I curve of the S-type memristor is obtained by numerical simulation, as shown in Fig. 2(a). The DC V–I curve shows an S-shape and possesses a negative slope in segments ab and cd, which indicates that the memristor is current-controlled and locally active with negative differential conductance (NDC).[47,48] Segment ab corresponds to the negative differential conductance region for $-0.328\ {\rm V} \le V_{\rm M} \le 0.056\ {\rm V}$ and $0.656\ {\rm mA} \ge I_{\rm M} \ge -0.112\ {\rm mA}$, and segment cd corresponds to the negative differential conductance region for $0.328\ {\rm V} \ge V_{\rm M} \ge -0.056\ {\rm V}$ and $-0.656\ {\rm mA} \le I_{\rm M} \le 0.112\ {\rm mA}$. This means that the S-type memristor can be operated in its locally active domain when supplied with a DC voltage within these ranges.[49] Note that the memristor can operate in its locally active domain without a DC bias, since both segments pass through the origin. Then, $i_{\rm M} = i_{\rm MAX}\sin(2\pi F t)$ is applied with $F = 1$ kHz, 2 kHz, and 3 kHz, and $i_{\rm MAX} = 0.5$ mA to the input terminal of the memristor. The frequency-dependent pinched hysteresis loops are numerically acquired, as shown in Fig. 2(b). The frequency-dependent pinched hysteresis loops pass through the origin and shrink with increasing frequency, which meets the definition of a memristor.[50] Figure 2(c) shows the frequency-dependent pinched hysteresis loops of

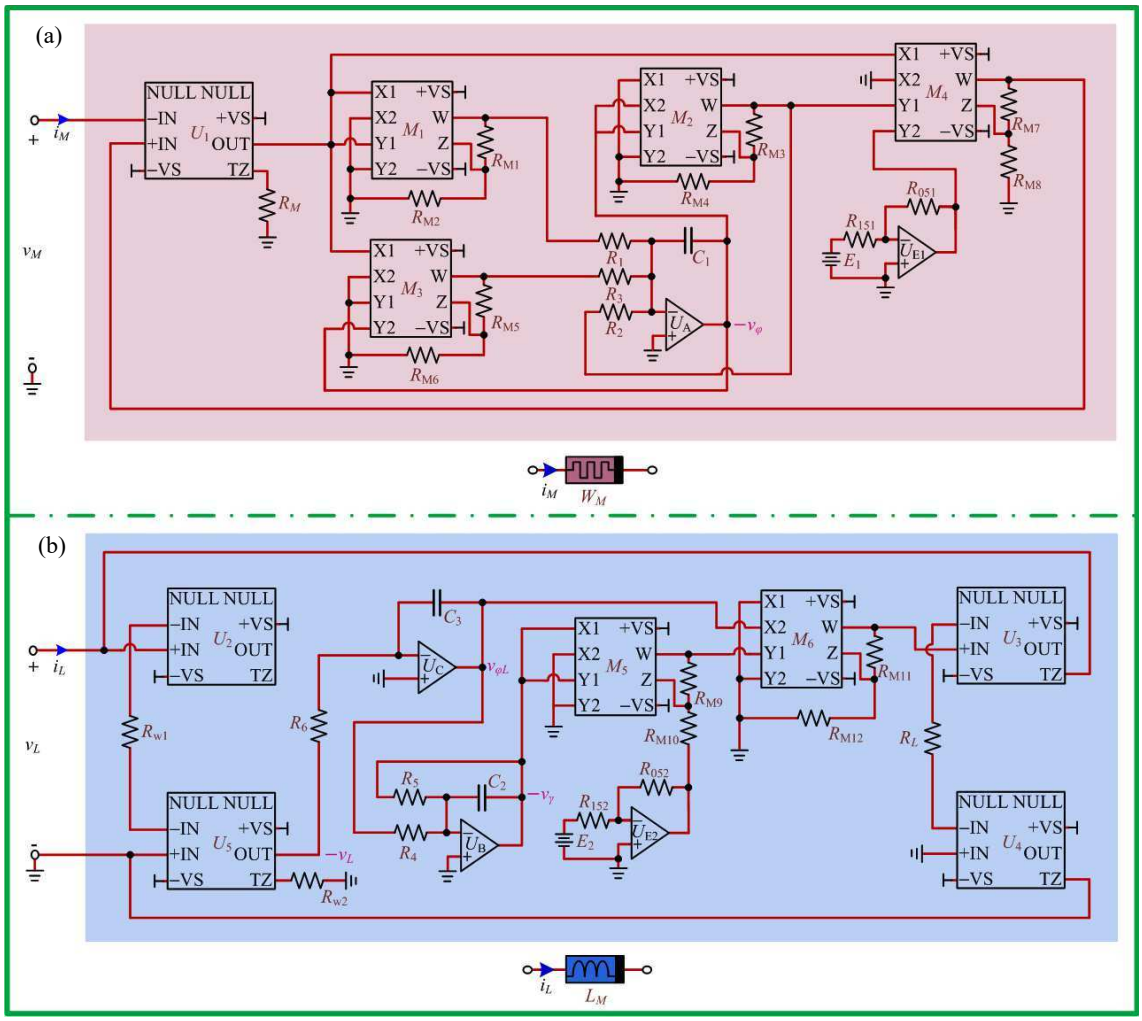


Fig. 1. Memristive and meminductive emulators: (a) S-type memristor emulator; (b) flux-controlled meminductor emulator.

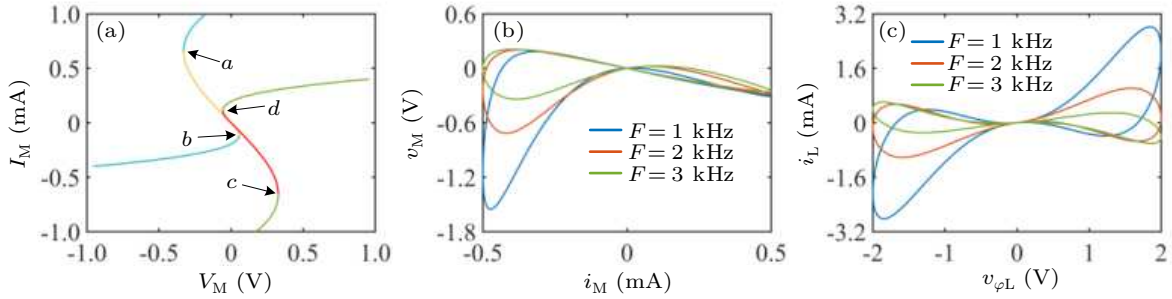


Fig. 2. Properties of the emulators: (a) DC V–I curve of the S-type memristor, where segment ab corresponds to the negative differential conductance (NDC) region for $-0.328\ \text{V} \le V_\text{M} \le 0.056\ \text{V}$ and $0.656\ \text{mA} \ge I_\text{M} \ge -0.112\ \text{mA}$, and segment cd corresponds to the NDC region for $0.328\ \text{V} \ge V_\text{M} \ge -0.056\ \text{V}$ and $-0.656\ \text{mA} \le I_\text{M} \le 0.112\ \text{mA}$; (b) frequency-dependent pinched hysteresis loops of the S-type memristor; (c) frequency-dependent pinched hysteresis loops of the flux-controlled meminductor.

the meminductor for $v_\text{M} = v_\text{MAX}\sin(2\pi F t)$ with $F = 1$ kHz, 2 kHz, and 3 kHz. The frequency-dependent pinched hysteresis loops pass through the origin, and the area of each lobe decreases with increasing frequency, which satisfies the definition of a meminductor.[36]

2.2. Circuit modeling

In the left panel of Fig. 3, the schematic of the microstructure of a biological neuron is shown. The main structure contains ion channels and a lipid bilayer membrane. Potassium and sodium ions move inward and outward, leading to the generation of ion channel currents. The biological neuron is in a resting state without external stimulus. In this state, a small number of potassium and sodium ions pass through ion channels to maintain a dynamic balance. A large number of potassium ions move outward and sodium ions move inward; thus, an action potential is triggered when an external stimulus is applied and exceeds the threshold of an excitable neuron. During the formation of an action potential, potassium and sodium ions in their channels are uniformly transported, resulting in uniformly varying ionic currents. In this process, the conductance of ion channels is under dynamic self-regulation, and complex electromagnetic induction is triggered in the ion channels. Some bionic circuits have been proposed to generate spiking activities of biological neurons, although it is impossible to fully reproduce the spiking activities of biological neurons. The bionic circuit provides a hardware foundation for artificial intelligence applications.

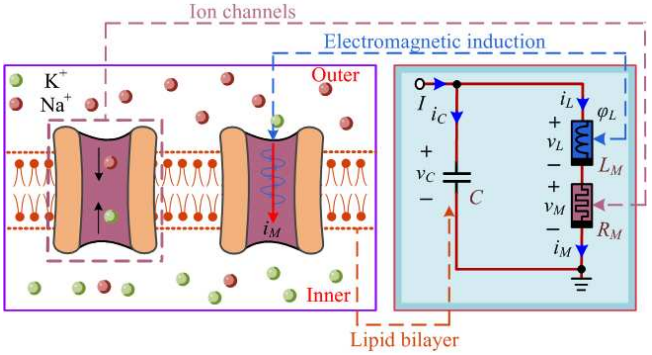


Fig. 3. Schematic of the meminductive and memristive emulator-based bionic circuit.

In the literature, numerous bionic circuits have been built by referring to the microstructure of a biological neuron, within which capacitors and time-varying resistors are frequently deployed to characterize the lipid bilayer membrane and ion channels, respectively. In recent years, memcapacitors and LAMs have been employed to build bionic circuits. Electromagnetic induction induced by varying ionic currents is not considered in these bionic circuits. The meminductor restricts the constitutive relationship between flux and current, which can be deployed to characterize the electromagnetic induction effect between flux and ionic currents. From the viewpoint of circuit modeling, we utilize an S-type memristor and a flux-controlled meminductor connected in series to characterize the electrophysiological properties of ion channels and their internal electromagnetic induction, as shown in the right panel of Fig. 3. Here, we employ a capacitor to characterize the lipid bilayer membrane to simplify the bionic circuit model. The capacitor and the branch composed of the memristor and meminductor are connected in parallel, since ion channels are embedded within the lipid bilayer membrane. The bionic circuit is driven by a DC current source. By introducing the memristive and meminductive emulators into the circuit schematic, the mathematical state equations of the bionic circuit shown in Fig. 3 can be formulated as

$$\begin{cases} C_1\dfrac{\mathrm{d}v_\sigma}{\mathrm{d}t} = \dfrac{g_1 i_\text{M}^2 R_\text{M}^2}{R_1} - \dfrac{g_2 v_\sigma^2}{R_2} - \dfrac{g_3 v_\sigma i_\text{M} R_\text{M}}{R_3}, \\ C_2\dfrac{\mathrm{d}v_\gamma}{\mathrm{d}t} = \dfrac{v_{\varphi L}}{R_4} - \dfrac{v_\gamma}{R_5}, \\ C_3\dfrac{\mathrm{d}v_{\varphi L}}{\mathrm{d}t} = \dfrac{v_\text{C} - g_4(v_\alpha^2 - E_\text{M})i_\text{M} R_\text{M}}{R_6}, \\ C\dfrac{\mathrm{d}v_\text{C}}{\mathrm{d}t} = I - \dfrac{g_6(g_5 v_\gamma^2 - E_\text{L})v_{\varphi L}}{R_\text{L}}. \end{cases} \tag{3}$$

The typical parameters are set as $C = 100$ nF, $I = 0.38$ mA, $R_\text{M} = 1.5\ \text{k}\Omega$, $E_\text{M} = 0.5$ V, $R_\text{L} = 1.5\ \text{k}\Omega$, and $E_\text{L} = 0.5$ V.

3. Dynamical behavior exploration

In this subsection, we explore the dynamical behavior of the memristive and meminductive emulator-based bionic cir-

cuit using double-parameter and single-parameter bifurcation diagrams, double-parameter and single-parameter Lyapunov exponents (LEs), and time-domain waveforms for external stimulus and ion channel-related parameters, e.g., I, $R_{\rm M}$, $E_{\rm M}$, $R_{\rm L}$, and $E_{\rm L}$. The bifurcation diagrams are simulated using the MATLAB ODE45 solver with a time step of 10^{-6} s and a total simulation time of 0.1 s. The LEs are computed using a Jacobi-matrix-based Wolf's method with a time step of 10^{-4} s and a final simulation time of 0.1 s. The initial states are set to $[v_\sigma(0), v_\gamma(0), v_{\varphi L}(0), v_{\rm C}(0)] = [0\ {\rm V}, 0\ {\rm V}, 0\ {\rm V}, 0\ {\rm V}]$; that is, the effect of initial conditions is not considered.

A single-parameter bifurcation diagram for I is plotted to explore the dynamical behavior under external stimuli, as shown in Fig. 4. The bionic circuit undergoes forward and reverse period-doubling bifurcation routes as I increases from 0.25 mA to 0.85 mA. In detail, the bionic circuit begins with period-1 at 0.25 mA, then evolves into chaos via a forward period-doubling bifurcation route. Afterward, a period-3 window appears due to a tangent bifurcation, and then chaos emerges via a chaos crisis. Subsequently, multiple reverse period-doubling bifurcation routes and chaos-crisis scenarios occur. Finally, the bionic circuit returns to period-1 behavior. This demonstrates that the bionic circuit can generate abundant periodic and chaotic firing behaviors. Here, we only present the first two LEs. $\rm LE_1 > 0$ and $\rm LE_2 = 0$ correspond to chaotic firing behavior, $\rm LE_1 = 0$ and $\rm LE_2 < 0$ correspond to periodic firing behavior, and $\rm LE_1 < 0$ and $\rm LE_2 < 0$ correspond to a stable state. One can see that the dynamical behaviors revealed by the single-parameter bifurcation diagram and LEs are consistent.

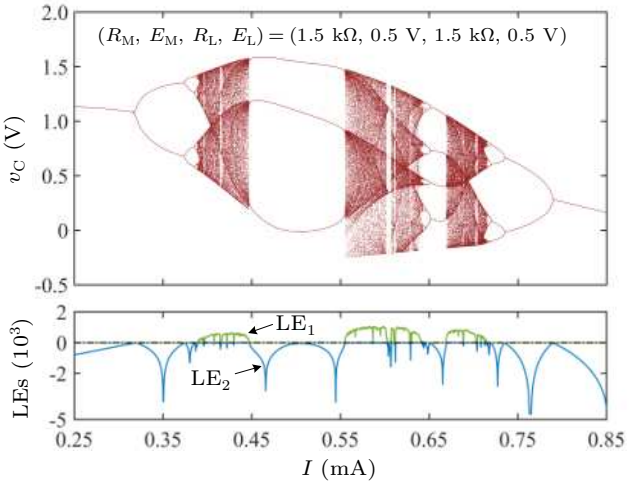


Fig. 4. Single-parameter bifurcation diagram (top) and Lyapunov exponents (bottom) with respect to I.

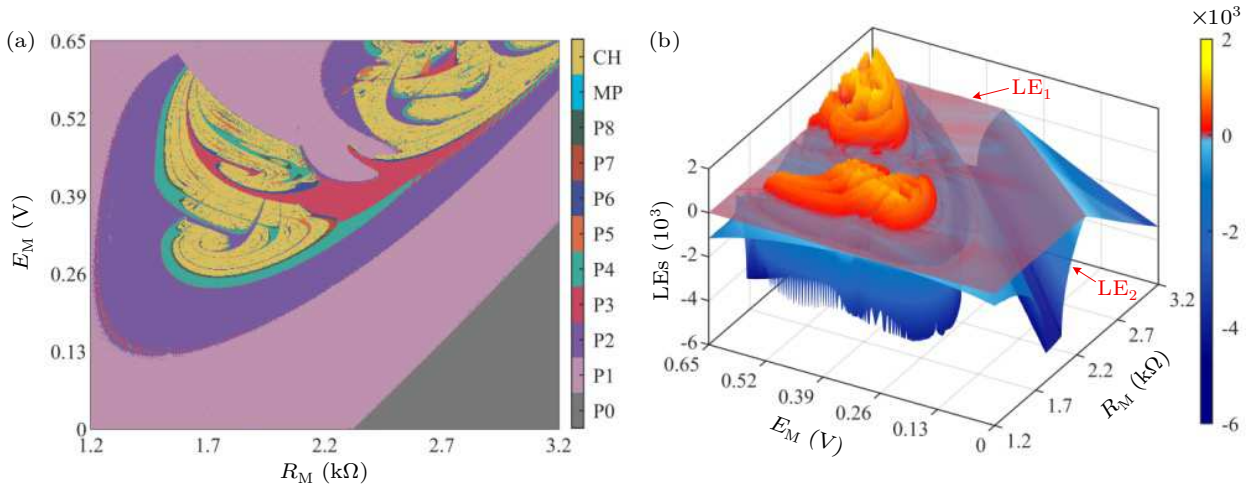


Fig. 5. Dynamical distribution on the $R_{\rm M}$–$E_{\rm M}$ parameter plane: (a) double-parameter bifurcation diagram; (b) double-parameter LE map in a 3D view.

Figure 5 displays the double-parameter bifurcation diagram and the corresponding LE map on the $R_{\rm M}$–$E_{\rm M}$ parameter plane, where $R_{\rm M}$ and $E_{\rm M}$ vary within the ranges [1.2 kΩ, 3.2 kΩ] and [0 V, 0.65 V], respectively. By examining the periodicity of $v_{\rm C}$, the dynamical behaviors in the double-parameter bifurcation diagram are classified. Chaotic behavior (CH) is indicated in dark yellow, multi-periodic behavior (MP) in light yellow, unbounded behavior (P0) in gray, and periodic behaviors of period-1 to period-8 (P1–P8) in other colors, as shown in Fig. 5(a). Figure 5(b) provides a three-dimensional (3D) view of the first two LEs for better visualization of the dynamical distribution. A color gradient is employed to distinguish different dynamical regimes, where yellow-to-red corresponds to positive LE and light-blue-to-dark-blue corresponds to negative LE. Note that only the first two LEs are shown in Fig. 5(b). The double-parameter LE plot exhibits dynamical features that are consistent with those observed in the double-parameter bifurcation diagram. Moreover, the double-parameter bifurcation diagram displays a banded structure with transitions among P1–P2–P4–P8. This reflects the emergence of forward and reverse period-doubling bifurcation routes, which govern the abundant firing behaviors of the bionic circuit.

Single-parameter bifurcation diagrams and LE plots of $R_{\rm M}$ and $E_{\rm M}$ are simulated to reveal the bifurcation behaviors of the bionic circuit, as shown in Fig. 6. The single-parameter

bifurcation diagram in Fig. 6(a) shows that the firing behavior of the bionic circuit begins with forward period-doubling into chaos and eventually transitions into a P1 state via multiple forward period-doubling bifurcation routes and reverse period-doubling as R_{M} increases. During this process, several transitions occur in the bionic circuit via tangent bifurcations and chaos crisis scenarios. These dynamical behaviors and their transitions are well validated by the LEs. Figure 6(b) shows that as E_{M} increases, the firing behavior evolves from forward period-doubling to period-4, and subsequently returns to a P1 state through reverse period-doubling. Note that the single-parameter bifurcation structure with respect to E_{M} appears relatively simple under typical parameter settings. The double-parameter bifurcation diagram in Fig. 5(a) indicates that single-parameter bifurcation diagrams can also exhibit abundant dynamical behaviors for E_{M} under other values of R_{M}.

Subsequently, we investigate the dynamical distribution and bifurcation behavior associated with R_{L} and E_{L}. Figure 7 depicts the double-parameter bifurcation diagram and the corresponding double-parameter LE map on the R_{L}–E_{L} parameter plane for 0.5 kΩ $\leq R_{\mathrm{L}} \leq$ 3.5 kΩ and 0 V $\leq E_{\mathrm{L}} \leq$ 1.0 V. The colorbar settings are consistent with those used in Fig. 5. One can see that R_{L} and E_{L} can trigger abundant dynamical transitions, including the P1–P2–P4–P8–CH sequence within certain local parameter regions, and vice versa. These dynamical transitions reflect the emergence of forward and reverse period-doubling bifurcation routes. Figure 7(b) further provides a 3D view of the first two LEs, which corroborates the dynamical distribution and its associated transitions.

Figure 8 shows the single-parameter bifurcation diagrams and the corresponding LE plots for R_{L} and E_{L}. As R_{L} increases from 0.5 kΩ to 3.5 kΩ, the bionic circuit evolves from P1 into chaos via a crisis, then undergoes multiple reverse period-doubling routes and chaos-crisis scenarios, and subsequently returns to P1. When E_{L} increases from 0 V to 1.0 V, the single-parameter bifurcation diagram exhibits dynamical behavior opposite to that of R_{L}; for example, the bionic circuit enters chaos through a forward period-doubling route and transitions from chaos to periodic behavior via a tangent bifurcation. The corresponding LE plots validate these dynamical transitions.

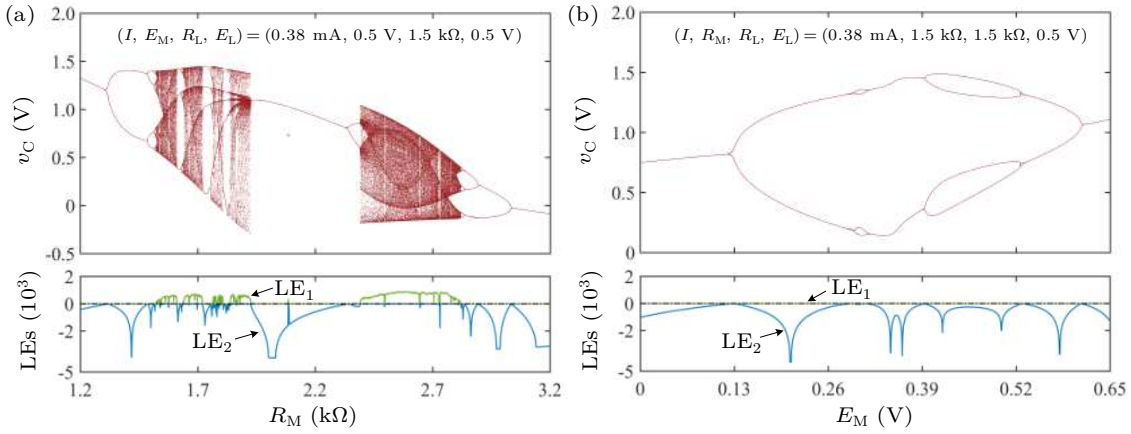


Fig. 6. Single-parameter bifurcation diagrams (top) and LEs (bottom): (a) with respect to R_{M}; (b) with respect to E_{M}.

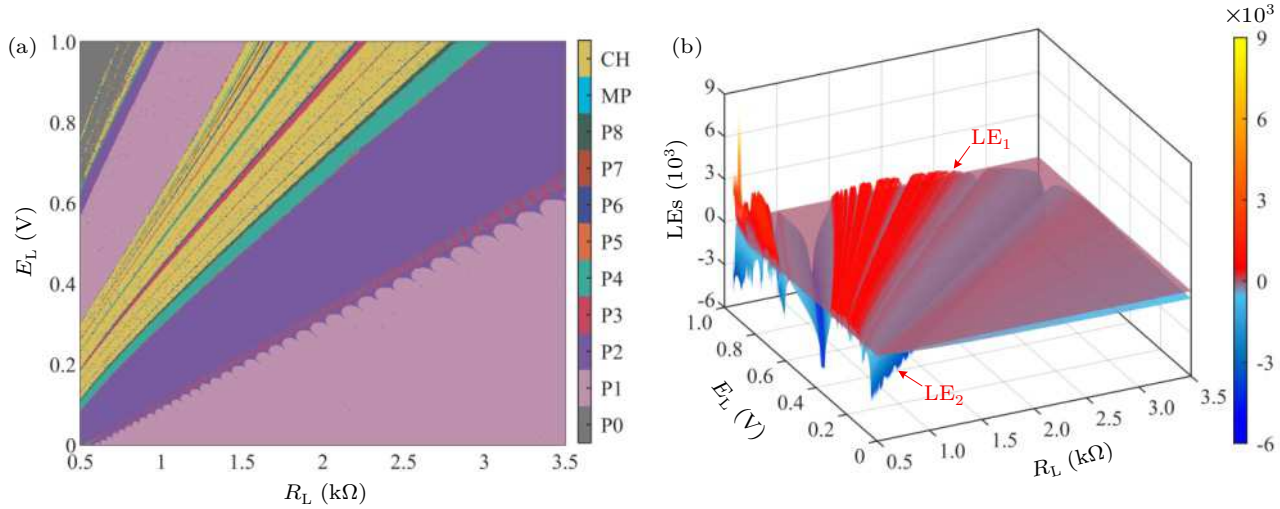


Fig. 7. Dynamical distribution on the R_{L}–E_{L} parameter plane: (a) double-parameter bifurcation diagram; (b) double-parameter LE map in a 3D view.

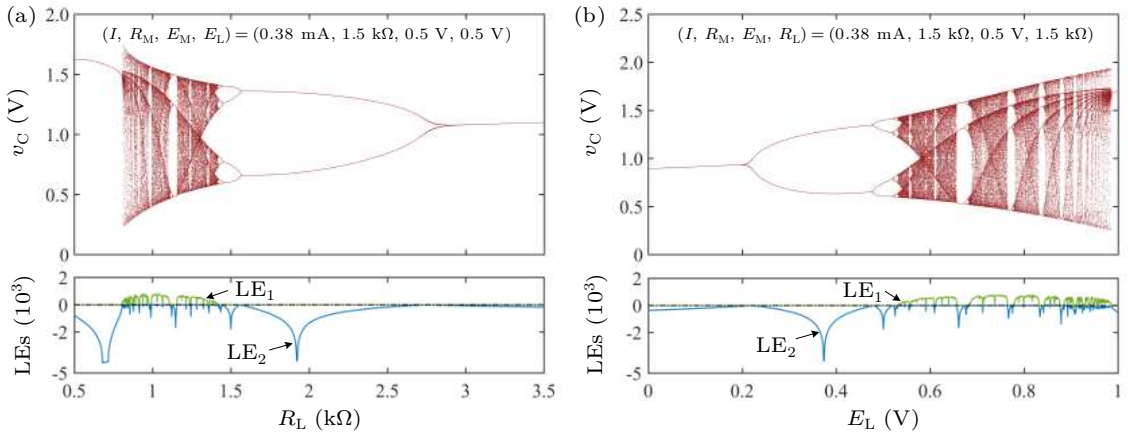


Fig. 8. Single-parameter bifurcation diagrams (top) and LEs (bottom): (a) with respect to R_L; (b) with respect to E_L.

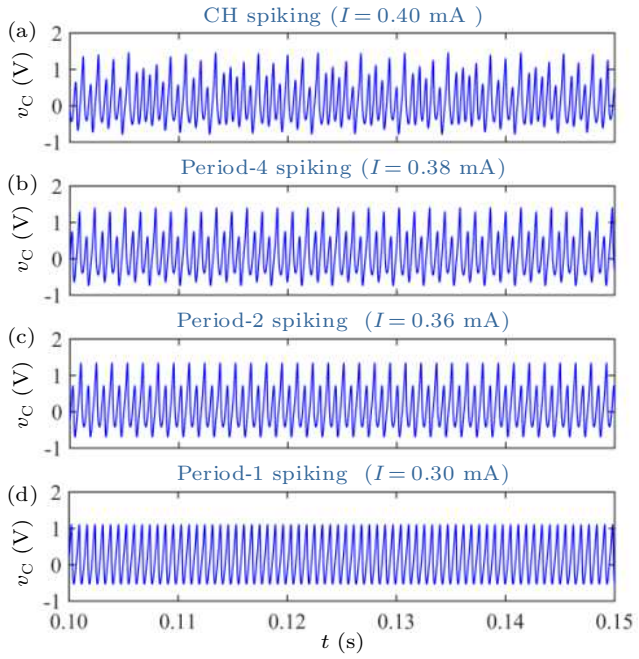


Fig. 9. Time-domain waveforms of v_C for different I: (a) CH spiking activity for $I = 0.40$ mA; (b) period-4 spiking activity for $I = 0.38$ mA; (c) period-2 spiking activity for $I = 0.36$ mA; (d) period-1 spiking activity for $I = 0.30$ mA.

Some discrete values of I are selected to demonstrate the firing behaviors in the bionic circuit, as shown in Fig. 9. Numerical simulations of the time-domain waveforms for $I =$ 0.30 mA, 0.36 mA, 0.38 mA, and 0.40 mA reveal that the P1, P2, P4, and CH spiking activities correspond to the dynamical behaviors shown in Fig. 4. These transitions of spiking activity also reflect the emergence of a reverse period-doubling bifurcation route. It should be emphasized that the objective of this paper is not to replicate the spiking activity of specific biological neurons; instead, it aims to reveal diverse neuronal firing behaviors generated by the bionic circuit.

Numerical simulations of the meminductive and memristive emulator-based bionic circuit demonstrate that the proposed circuit is feasible for generating chaotic and periodic spiking activities. In addition, the numerical simulations further indicate that the DC current stimulus and the parameters of the memristor and meminductor can strongly regulate these spiking activities,[51] reflecting the interplay between external stimulus and the electrophysiological properties of ion channels. Moreover, spiking activities with different periods may provide a promising pathway for energy-efficient implementations of spike-based bionic hardware in spiking neural networks.[52,53]

4. Hardware circuit and experiment

Referring to Figs. 1 and 3, the analog hardware circuit is manually fabricated, as shown in the left panel of Fig. 10. In the hardware implementation, the C-FOAs are AD844AN, the operational amplifiers are AD711JN, and the analog multipliers are AD633JN, while the capacitors are monolithic. Note that several additional chip resistors and potentiometers are deployed in the hardware circuit. Resistors R_{M1}–R_{M12} are used to adjust the gains of multipliers M_1–M_6, where $R_{M1} = R_{M3} = R_{M5} = R_{M7} = R_{M9} = R_{M11} = 1$ kΩ, and $R_{M2} = R_{M4} = R_{M6} = R_{M8} = R_{M10} = R_{M12} = 9$ kΩ. In addition, operational amplifier U_{E1} together with R_{051} and R_{151} is used to adjust the Y_2 input voltage of multiplier M_4 to realize Eq. (1). R_{051} is a potentiometer and R_{151} is a 15 kΩ chip resistor. The bias voltage E_M in the memristive function R_M can be tuned by adjusting the resistance of R_{051}. Similarly, operational amplifier U_{E2} together with R_{052} and R_{152} is used to adjust the bias voltage of multiplier M_5 to realize Eq. (2). R_{052} is a potentiometer and R_{152} is a 15 kΩ chip resistor. Adjusting R_{052} enables tuning of the bias voltage E_L in the inverse meminductive function L_M^{-1}. U_{ext} is a C-FOA (AD844AN) that converts the external DC voltage V_{ext} to an external DC current I through $I = V_{ext}/R_{ext}$. Here, R_{ext} is fixed to 10 kΩ, and V_{ext} is adjusted to obtain the desired DC current I. The analog hardware circuit is powered by VEE $= -15$ V and VCC $= +15$ V.

Here, we assess the deviation of circuit parameters between hardware experiment and numerical simulation by the mean absolute percentage error (MAPE),[54] which is defined

as

$$\mathrm{MAPE} = \frac{1}{N}\sum_{k=1}^{N}\frac{\left|P_{\mathrm{desired,k}} - P_{\mathrm{measured,k}}\right|}{P_{\mathrm{desired,k}}} \times 100\%, \qquad (4)$$

where $P_{\mathrm{desired,k}}$ denotes the circuit parameters in numerical simulation and $P_{\mathrm{measured,k}}$ denotes the corresponding parameters in the hardware experiment. N is the number of finely adjusted circuit parameters.

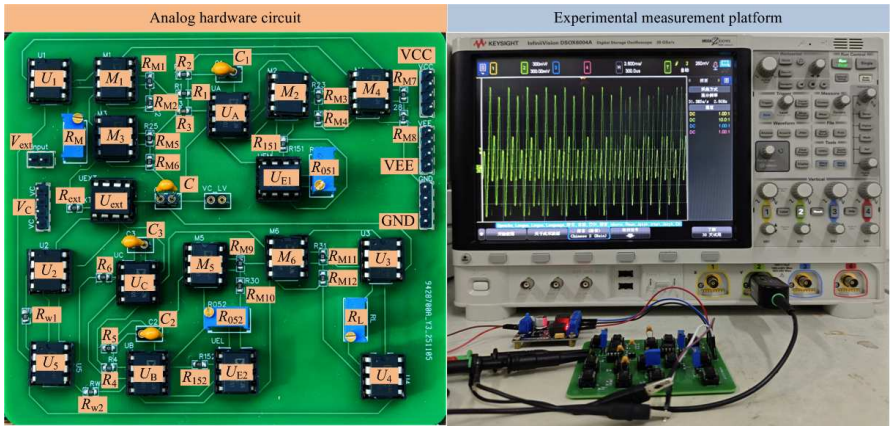


Fig. 10. Analog hardware circuit (left) and experimental measurement setup (right).

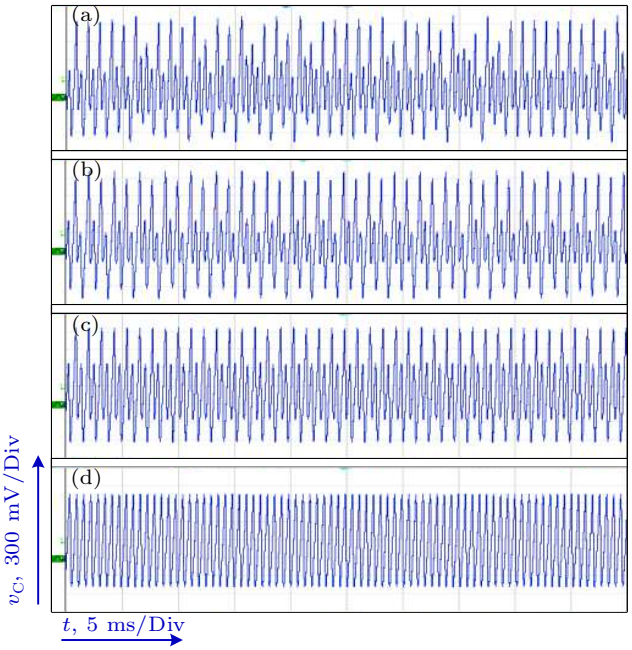


Fig. 11. Hardware-measured time-domain waveforms of v_C for different I: (a) CH spiking activity for $I = 0.40$ mA; (b) period-4 spiking activity for $I = 0.38$ mA; (c) period-2 spiking activity for $I = 0.36$ mA; (d) period-1 spiking activity for $I = 0.30$ mA.

The experimental measurement setup is illustrated in the right panel of Fig. 10, which involves a power supply module, a digital oscilloscope, and the analog hardware circuit. The power supply module provides ±15 V DC voltage. Due to non-ideal characteristics of discrete circuit components and temperature variations, discrepancies inevitably exist between the circuit parameters used in hardware experiments and those used in numerical simulations. During the experimental measurements, four circuit parameters, i.e., R_{M}, E_{M}, R_{L}, and E_{L}, are finely adjusted to maintain the external DC current I as in Fig. 9. Note that all other circuit parameters are kept identical to those used in numerical simulations. The experimentally captured time-domain waveforms are post-processed using Adobe Photoshop to adjust color schemes and rescale the figures for better visualization, as shown in Fig. 11. The green marker on the left side of the figure indicates the zero-voltage reference line of the digital oscilloscope. The circuit parameters in hardware experiments and MAPEs for different spiking activities are listed in Table 1. The MAPEs are all below 10%, which is acceptable for analog circuit experiments.

Table 1. Circuit parameters in hardware experiments and MAPEs for spiking activities.

Spiking	Measured parameters ($I, R_{\mathrm{M}}, E_{\mathrm{M}}, R_{\mathrm{L}}, E_{\mathrm{L}}$)	MAPE
CH spiking	(0.40 mA, 1.551 kΩ, 0.559 V, 1.524 kΩ, 0.587 V)	8.6%
Period-4 spiking	(0.38 mA, 1.553 kΩ, 0.537V, 1.561 kΩ, 0.485 V)	4.5%
Period-2 spiking	(0.36 mA, 1.416 kΩ, 0.486 V, 1.520 kΩ, 0.586 V)	6.8%
Period-1 spiking	(0.30 mA, 1.401 kΩ, 0.558 V, 1.447 kΩ, 0.549 V)	7.9%

5. Conclusion

This paper proposes a simple framework for a bionic circuit, which comprises only a capacitor, an S-type memristor, a flux-controlled meminductor, and an external DC current source. Numerical simulations and hardware experiments are performed to verify the effectiveness of the proposed circuit in generating abundant dynamical behaviors and spiking activities. These dynamical behaviors include forward and reverse period-doubling bifurcation routes, chaotic-crisis scenarios, and tangent bifurcations, which induce abundant chaotic and periodic spiking activities. Note that the bionic circuit generates spiking activity primarily through the appearance of forward and reverse period-doubling bifurcation routes. This is different from the period-adding bifurcation route typically associated with bursting activity. These results confirm that the memristor and meminductor are potential candidates for characterizing ion channels and their internal electromagnetic in-

duction in bionic circuit modeling. The proposed bionic circuit is applicable to spike-based neural networks[2] and low-power brain-inspired chips.[25]

The proposed framework can be used to construct bionic circuits for generating spiking activities in academic research. However, mem-element emulator-based bionic circuits are still limited in integration and exhibit relatively high energy consumption. To address this issue, CMOS-based technology and advanced physical mem-device implementations provide feasible approaches for realizing the proposed framework. The objective of this work is not to replicate the spiking activities of specific biological neurons, but to generate neuron-like spiking behaviors from an application-oriented perspective. This can improve energy efficiency and broaden spike-based applications. In addition, the use of physical memory devices can further simplify the hardware implementation of bionic circuits. However, real memory devices inevitably introduce non-ideal effects, such as threshold behavior, parasitic capacitances, and leakage flux, which may influence the dynamics and spiking activities of the circuit. Under biologically realistic conditions, noise perturbations may also significantly affect the circuit dynamics. These issues warrant further investigation.

Acknowledgments

Project supported by the National Natural Science Foundation of China (Grant Nos. 12572066 and 12172066), the 333 Project of Jiangsu Province, the Research and Innovation Project of the Compound Semiconductor Innovation Consortium (Grant No. RIPCSIC202502), and the College Students' Innovation and Entrepreneurship Training Program of Changzhou University (Grant No. S202510292080).

References

[1] Ma J 2025 *Nonlinear Dyn.* **113** 25365
[2] Yang S M and Chen B D 2025 *IEEE Trans. Neural Netw. Learning Syst.* **36** 1734
[3] Yu Z H, Zhu K L, Wang Y and Yang F F 2025 *Chaos Soliton Fractals* **194** 116233
[4] Cao H L, Cao Y H, Qin L and Mou J 2025 *Chaos Soliton Fractals* **191** 115857
[5] Wu J Y, Li Z J and Lan Y H 2025 *Nonlinear Dyn.* **113** 13715
[6] Xu Q, Ding X C, Chen B, Parastech F, Iu H H C and Ning W 2024 *IEEE Trans. Circuits Syst. I* **71** 4120
[7] Zhang Y T and Zeng Z G 2023 *IEEE Trans. Circuits Syst. I Reg. Pap.* **70** 1868
[8] Chen H G, Hong Q H, Wang Z R, Wang C H, Zeng X X and Zhang J L 2025 *IEEE Trans. Neural Netw. Learning Syst.* **36** 1734
[9] Sung S H, Kim T J, Shin H, Im T H and Lee K J 2022 *Nat. Commun.* **13** 2811
[10] Wang Z R, Rao M Y, Han J W, Zhang J M, Lin P, Li Y N, Li C, Song W H, Asapu S and Midya R 2018 *Nat. Commun.* **9** 3208
[11] Deepthi M, Shashidhara H Lopes S R and Masoller C 2021 *Neurocomputing* **441** 44
[12] Kumar P, Ranjan R K and Kang S M 2024 *IEEE Trans. Circuits Syst. I* **71** 1757
[13] Singh A, Kim D, Lee H and Lee B G 2025 *IEEE Trans. Circuits Syst. I* **72** 1056
[14] Haghiri S, Naderi A, Ghanbari B and Ahmadi A 2020 *IEEE Trans. Circuits Syst. I* **68** 275
[15] Lai Q, Lai C, Zhang H and Li C B 2022 *Chaos Soliton Fractals* **158** 112017
[16] Zhang Y X, Fang Z L and Yan X B 2022 *Appl. Phys. Lett.* **120** 213502
[17] Ren K, Zhang K J, Qin X Z, Ren H X, Zhu S H, Yang F, Sun B, Zhao Y and Zhang Y 2021 *Acta Phys. Sin.* **70** 078701 (in Chinese)
[18] Zhang X M, Zhuo Y, Luo Q, Wu Z H, Midya R, Wang Z R, Song W H, Wang R, Upadhyay N K and Fang Y L 2020 *Nat. Commun.* **11** 51
[19] Zhao R Y, Wang T, Moon T, Xu Y C, Zhao J, Sud P, Kim S J, Liao H T, Zhuo Y and Midya R 2025 *Nat. Electron.* **8** 1211
[20] Pei Y F, Yang B, Zhang X M, He H, Sun Y, Zhao J H, Chne P, Wang Z F, Sun N F and Liang S X 2025 *Nat. Commun.* **16** 48
[21] Shan Y X, Liu Z Y, Tao Y, Dong Y J, Wang Z Q, Bian J Y, Zhao X N, Lin Y, Xu H Y and Liu Y C 2024 *IEEE Electron Dev. Lett.* **45** 1815
[22] Lizzit D, Segatto M and Esseni D 2022 *IEEE Trans. Electron. Dev.* **72** 1083
[23] Wang X P, Ye S, Cui B Y, Li Y C, Wei Y, Xiao Y, Liu J H, Huang Z Y, Wu Y S and Wen Y C 2025 *Nano Energy.* **140** 111011
[24] Khan M U, Hassan B, Alazzam A, Eissa S and Mohammad B 2025 *Microsyst. Nanoeng.* **11** 37
[25] Ishisaki Y, Oshio R, Kuwahara T, Shintani M, Tokumitsu E, Matsuda T, Kawanishi H, Nakashima Y and Kimura M 2024 *IEEE Trans. Electron. Dev.* **71** 4626
[26] Dinavahi A and Harris H R 2025 *Sci. Rep.* **15** 40627
[27] Wang Y F, Tao K F, Zhao L H and Sun J W 2025 *IEEE Trans. Circuits Syst. I* **72** 7940
[28] Mou J, Ma T, Banerjee S and Zhang Y S 2024 *IEEE Trans. Circuits Syst. I* **71** 1771
[29] Ding X C, Fan W W, Wang N, Su Y H, Chen M, Lin Y and Xu Q 2025 *Chaos Soliton Fractals* **199** 116658
[30] Xu Q, Zhang C Y, Wu H G, Chen M, Bao H, Iu H H C and Wang N 2025 *IEEE Trans. Circuits Syst. I*
[31] Liang Y, Zhu Q, Wang G Y, Nath S K, Iu H H C, Nandi S K and Elliman R G 2021 *IEEE Trans. Circuits Syst. I* **69** 1278
[32] Xu Q, Fang Y J, Feng C T, Parastesh F, Chen M and Wang N 2024 *Nonlinear Dyn.* **112** 13451
[33] Xu Q, Wang K, Feng C T, Fan W W and Wang N 2024 *Chaos Soliton Fractals* **189** 115646
[34] Mou J, Cao H L, Zhou N R and Cao Y H 2024 *IEEE Trans. Cybernetics* **54** 7333
[35] Dong Y J, Guo R R, Liang Y, Yang J Q, Wang G Y 2024 *Chaos* **34** 083121
[36] Di Ventra M, Pershin Y V and Chua L O 2009 *Proc. IEEE* **97** 1717
[37] Goel A, Rai S K and Aggarwal B 2023 *Wirel. Pers. Commun.* **131** 2501
[38] Gupta R K, Saxena V and Choudhry M S 2025 *Circuits Syst. Signal Process.* **44** 1
[39] Korkmaz M O, Babacan Y and Yesil A 2023 *AEU-Int. J. Electron. Commun.* **158** 154450
[40] Sharma P K, Ranjan R K, Kang S 2024 *IEEE Circuits Syst. Mag.* **24** 8
[41] Petrović P B 2026 *Circuits Syst. Signal Proc.*
[42] Ma J 2023 *J. Zhejiang Univ.-Sci. A* **24** 109
[43] Xu Q, Wang K, Shan Y F, Wu H G, Chen M and Wang N 2024 *Cogn. Neurodyn.* **18** 645
[44] Xu Q, Ju Z T, Ding S K, Feng C T, Chen M and Bao B C 2022 *Cogn. Neurodyn.* **16** 1221
[45] Qi G Y, Wu Y and Hu J B 2021 *Int. J. Bifurc. Chaos* **31** 2150170
[46] Bao H, Li K X, Ma J, Hua Z Y, Xu Q and Bao B C 2023 *Sci. China Technol. Sci.* **66** 3153
[47] Chua L 2022 *Jpn. J. Appl. Phys.* **61** SM0805
[48] Mannan Z I, Choi H and Kim H 2016 *Int. J. Bifurc. Chaos* **26** 1630009
[49] Jin P P, Wang G Y, Liang Y, Iu H H C and Chua L O 2021 *IEEE Trans. Circuits Syst. I* **68** 4419
[50] Chua L 2019 *Handbook of Memristor Networks* (Springer) pp. 89–157
[51] Lech M, Berry B M, Topcu C, Kremen V, Nejedly P, Lega B, Gross R E, Sperling, M R, Jobst B C and Sheth S A 2021 *IEEE Trans. Biomed. Eng.* **68** 3701
[52] Rao A, Plank P, Wild A and Maass W 2022 *Nat. Mach. Intell.* **4** 467
[53] Zhou P, Choi D U, Lu W D, Kang S M and Eshraghian J K 2022 *IEEE J. Emerg. Sel. Top. Circuits Syst.* **12** 888
[54] De Myttenaere A, Golden B, Le Grand B and Rossi F 2016 *Neurocomputing* **192** 38