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RAPID COMMUNICATION

Design and optimization of area-selective carrier modulation in β-Ga_2O_3 through high temperature oxygen annealing

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Carrier modulation in beta-gallium oxide (β-Ga_2O_3) films through an oxygen annealing method is systematically investigated, including annealing time and annealing cap layer (ACL) design. Capacitance–voltage measurement conducted on vertical SBD structures was used to evaluate the carrier concentration after annealing. The formation of a "surface layer" may suppress the diffusion of oxygen species as the annealing time increases. An 8-hour annealing time resulted in a carrier modulation with an approximately 3-μm-deep low-carrier-concentration layer. The annealing cap layer, consisting of poly-Si and SiO_2, was deposited and patterned to achieve area-selective carrier modulation in β-Ga_2O_3. The effective thickness of poly-Si for blocking oxygen diffusion was confirmed by scanning electron microscopy (SEM) for the first time. A definite thickness of SiO_2 served as both etching stop layer and lift-off layer for poly-Si. According to simulation results, the non-ideal surface caused extra high peak electric field in the β-Ga_2O_3 device. A combination of an optimized dry etching method and low-compressive-stress deposition technology was employed to eliminate the bird's beak-like shape structure that appeared at the edges of the patterns and bulges on the β-Ga_2O_3 surface after annealing. The feasibility of the carrier modulation technology enables the diversity of β-Ga_2O_3 devices fabrication.

Keywords: Ga_2O_3, oxygen annealing, carrier modulation, power device

PACS: 71.55.–i, 73.61.–r, 85.30.–z

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1. Introduction

To date, Ga_2O_3 has attracted considerable interest and is seen as highly promising for high voltage power applications due to its ultra-wide bandgap (4.5–4.9 eV), high critical breakdown field (8 MV/cm), and cost-effective large-scale single crystal melt growth.[1,2] In the past few years, several area-selective carrier concentration modulation technologies have been employed to approach the theoretical limit of the trade-off between breakdown voltage (V_{br}) and specific on-resistance ($R_{on,sp}$) in β-Ga_2O_3 power devices and achieve electrical isolation in devices. Deep acceptors (Mg, N) have been exploited via the ion implantation technology for the current blocking layer of β-Ga_2O_3 UMOSFETs and the implanted edge termination of β-Ga_2O_3 SBDs. The area-selective regrowth technology has addressed the ohmic contact issues of the source electrode in UMOSFETs and MESFETs. Area-selective carrier concentration modulation technology is pivotal in power semiconductor device fabrication, providing more possibilities for various device designs.[3–13]

Ion implantation and area-selective regrowth have been the primary technologies used to achieve localized carrier concentration modulation in β-Ga_2O_3 power devices. These methods mainly target the modulation of n-type carrier concentration. However, challenges associated with ion implantation include uncontrollable implantation depth, the introduction of lattice damage and defects, and impurity redistribution caused by post-annealing activation.[7] Area-selective regrowth requires higher interface quality for the supporting substrate, and the regrown film also encounters impurity activation issues. While these two methods enrich the types of β-Ga_2O_3 power devices, the challenges they confront have hindered the fabrication of high-performance β-Ga_2O_3 power devices. Meanwhile, exploring a unique carrier concentration modulation technology, high-temperature oxygen annealing, is also a promising choice.

Numerous studies have demonstrated that high-temperature oxygen annealing can reduce the carrier concentration in β-Ga_2O_3.[14,15] It is considered that the reduction of n-type carrier concentration was related to an increase in Ga vacancy (V_{Ga}) density.[16–19] When β-Ga_2O_3 single crystal substrates were exposed to an oxygen atmosphere at temperatures exceeding 1000 °C, they underwent a transition from semiconductors to semi-insulators or even insulators (depending on the annealing time and the sample thickness),[20] indicating a significant modulation range of carrier concentration and diffusion depth. Moreover, high-temperature oxygen annealing offers a process cost advantage over ion implantation

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by removing the usage of high-energy ions, simplifying the process steps, and increasing the process yield. However, the inability to achieve precise modulation of carrier concentration and diffusion depth limited the application of this technology in β-Ga_2O_3 power devices. In our previous work,[21] high-temperature annealing has been employed to fabricate selective high-resistance terminal β-Ga_2O_3 Schottky barrier diodes (SBDs), demonstrating the feasibility of area-selective carrier concentration modulation technology in structural design and device fabrication on β-Ga_2O_3 power devices. Nevertheless, there is a lack of published literature in the field regarding the design of oxygen barrier layers and their impact on the surface morphology and electrical properties of β-Ga_2O_3. In this work, oxygen barrier layers were optimized in the patterning etching method and CVD SiO_2 film characteristics, which eliminated the surface non-ideal factors and improved the surface morphology and electrical properties of β-Ga_2O_3. These results further exploit the application potential of this technology in β-Ga_2O_3 power devices.

2. The time of oxygen annealing

The original β-Ga_2O_3 wafer used in this work consists of a 10 μm β-Ga_2O_3 epitaxial layer fabricated by halide vapor phase epitaxy (HVPE) with a net carrier concentration ($N_D - N_A$) of 1.7×10^{16} cm^{-3} grown on a high $N_D - N_A$ of 5×10^{18} cm^{-3} β-Ga_2O_3 substrate. The highest temperature of furnace tube was set at 1100 °C, increasing from an initial temperature of 450 °C over a heating time of 2 h and decreasing to reach 500 °C over a cooling time of 2.5 h. The pressure of the furnace tube was set at standard atmospheric pressure, and an O_2 flow rate of 3000 standard cubic centimeters per minute (sccm) was supplied during the entire equipment operation. Three β-Ga_2O_3 wafers were subjected to oxygen annealing process at a maximum setting temperature of 1100 °C for 4 h, 8 h, and 16 h (the highest temperature was held for 4 h, 8 h, and 16 h). Then the backside of the wafers underwent dry etching to maintain a good ohmic contact with cathode metal after oxygen annealing.

The measured structure of *C*–*V* method is illustrated in Fig. 1(a). The wafer was deposited by the Schottky metal (Ni/Au) with 200 μm radius on the frontside and the ohmic contact metal (Ti/Au) on the backside through electron beam evaporation.[22] As shown in Fig. 1(b), the normalized $1/C^2$ value increases significantly with longer annealing time compared to the pre-annealed. A significant increase in the extracted depletion depth is observed, from 0.32 μm at 0 V bias to 0.76 μm, 1.85 μm, and 1.89 μm after oxygen annealing at 1100 °C for 4 h, 8 h, and 16 h, respectively, as shown in Fig. 1(c). A thicker (∼ 3 μm) low-carrier-concentration layer with a carrier concentration below 10^{15} cm^{-3} is formed beneath the surface of the wafer after oxygen annealing for over 8 h. Nevertheless, the extracted $N_D - N_A$ and measured depletion depth at 0 V bias of wafer with oxygen annealing for 8 h were comparable to that of 16 h, indicating that the diffusion of oxygen was significantly suppressed. It is inferred that the effect of oxygen annealing on the β-Ga_2O_3 epitaxial layer reached near saturation over 8 hours due to the formation of a "surface layer".[23] To maximize the effectiveness of oxygen annealing in reducing carrier concentration and diffusion depth while minimizing the time and the cost involved, a duration of 8 h was chosen for the oxygen annealing process in subsequent experiments.

To verify the blocking effect of the "surface layer" formed during the first oxygen annealing for 8 h, a follow-up secondary annealing was performed. After the initial annealing, the SiO_2 cap layer was removed, and the β-Ga_2O_3 surface was selectively etched to three different depths: 0 nm, 300 nm and 600 nm, as illustrated in Fig. 2(a). Subsequently, all samples underwent a second oxygen annealing for 8 h in oxygen atmosphere. After the second annealing, a uniform 600 nm surface etching was applied, followed by the fabrication of SBD devices on all samples. A net carrier concentration extracted from *C*–*V* measurements of the three SBDs is shown in Fig. 2(b). As the surface etching depth after the first annealing increases, the minimum carrier concentration extracted after the second annealing continuously decreases. These results indicate that the "surface layer" formed during the first annealing partially inhibits further oxygen diffusion and limits carrier reduction. By removing this surface layer, the effectiveness of oxygen annealing in reducing carrier concentration can be further enhanced.

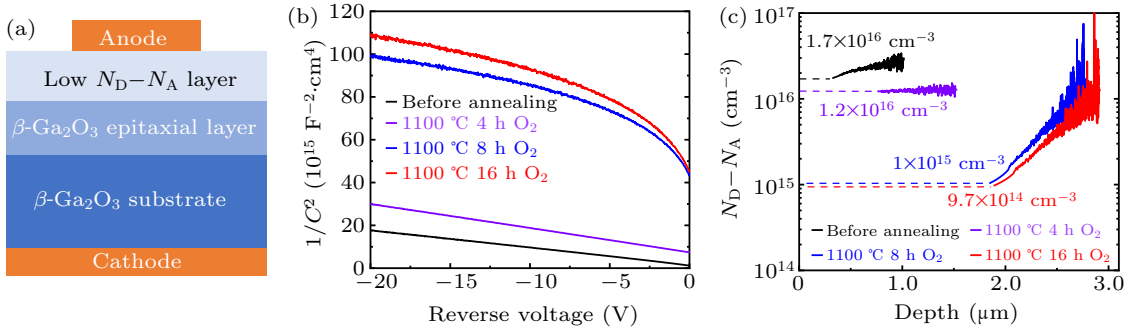


Fig. 1. (a) The measured structure in the *C*–*V* method. (b) Normalized $1/C^2$–*V* curves and (c) extracted $N_D - N_A$ profile for the original β-Ga_2O_3 wafer and three β-Ga_2O_3 wafers annealing in oxygen atmosphere at 1100 °C for 4 h, 8 h, and 16 h.

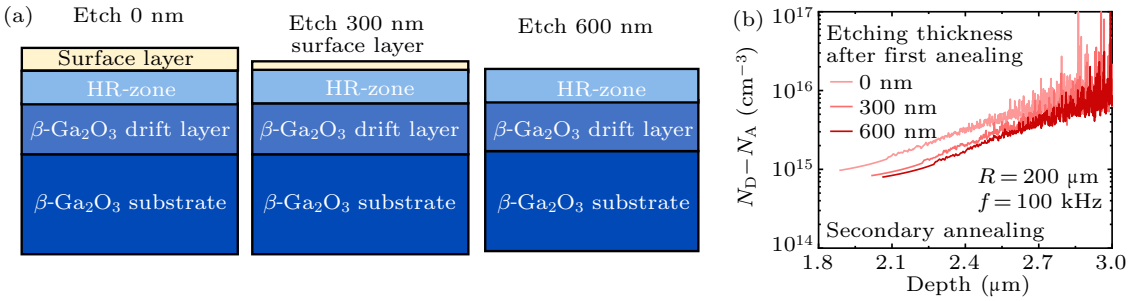


Fig. 2. (a) Samples with three different surface etching thicknesses after the first annealing. (b) Surface net carrier concentration of the samples after secondary annealing processes, extracted by the *C*–*V* method.

3. The thickness of oxygen barrier layers

The original β-Ga_2O_3 wafer was cleaned with organic solvents, piranha solution, deionized water and organic solvents sequentially. Subsequently, CVD SiO_2 and LPCVD poly-Si were deposited on the β-Ga_2O_3 wafer sequentially, as shown in Fig. 3(a). It is worth noting that the backside of the β-Ga_2O_3 wafer was in contact with the carrier wafer and the epitaxial layer was facing upward during SiO_2 deposition. During poly-Si deposition, the β-Ga_2O_3 wafer with SiO_2 layer was placed on a U-shaped quartz boat, with the wafer's edge overlapping on the quartz boat, thereby suspending the backside, resulting in the frontside and backside being deposited with poly-Si simultaneously. Then the β-Ga_2O_3 wafer was placed in a furnace tube for O_2 annealing at 1100 °C for 8 hours. These process flows can also be found in our previous work.[21]

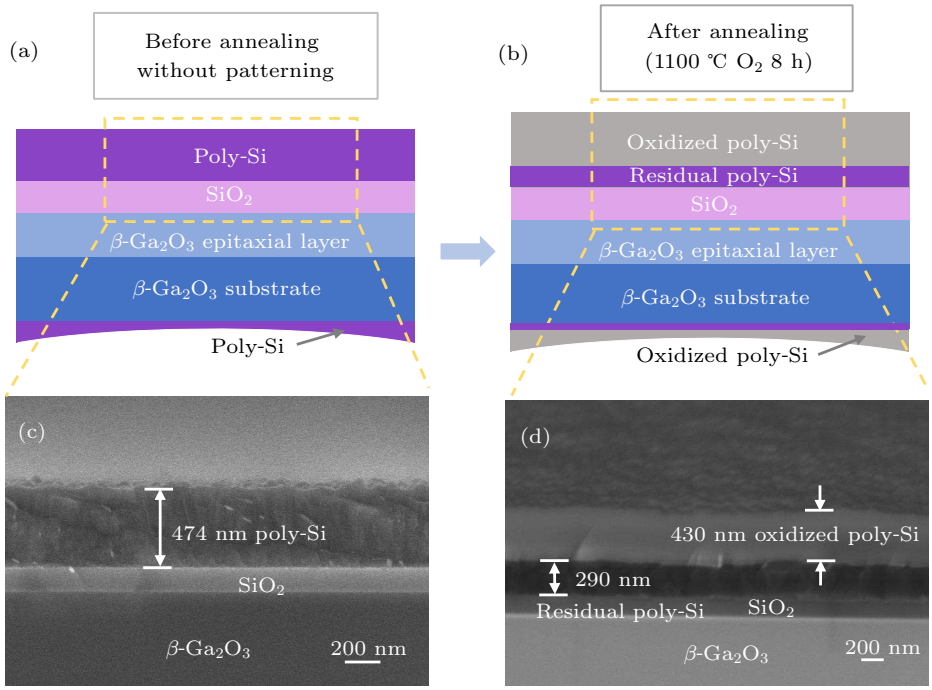


Fig. 3. The cross-section and the scanning electron microscope (SEM) images show the β-Ga_2O_3 wafer with PECVD SiO_2 and LPCVD poly-Si (a), (c) before and (b), (d) after oxygen annealing at 1100 °C for 8 h.

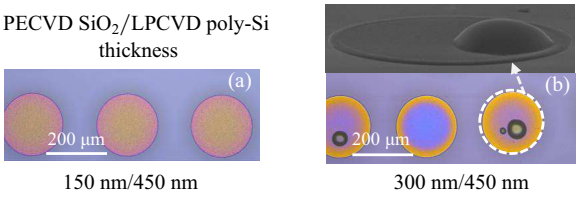


Fig. 4. The microscope images show the morphology of oxygen barrier layers with different SiO_2 thicknesses of (a) 150 nm, (b) 300 nm, after O_2 annealing for 8 h at 1100 °C.

The absorption of oxygen by poly-Si guarantees that the carrier concentration of β-Ga_2O_3 beneath remains unaffected. The thickness of LPCVD poly-Si oxidized was limited after 8-hour annealing in an oxygen atmosphere, with an estimated thickness of 184 nm according to the residual poly-Si, as shown in Figs. 3(c) and 3(d). The formation of dense oxide layer from oxidized poly-Si served as a barrier layer for oxygen, preventing the bottom Si from further oxidation. Under the annealing conditions mentioned above, the thickness of the poly-Si layer on the front side should be at least 184 nm to effectively block oxygen. Whereas, considering the non-uniformity of the thin film deposited in the wafer, the thickness of the poly-Si in the following experiment was set at 450 nm.

Area-selective carrier concentration modulation relies on

the patterning of oxygen barrier layers for oxygen annealing method. There may be uneven distribution of poly-Si thickness in larger size wafers. PECVD SiO_2 layer acts as an etching stop layer and a lift-off layer. A thicker SiO_2 layer underneath can enhance the fault tolerance of etching poly-Si. However, it does not mean that thicker SiO_2 is always better. Two samples with different thicknesses of SiO_2 and the same thickness of poly-Si were implemented to patterning and oxygen annealing, as illustrated in Figs. 4(a) and 4(b). For the 300 nm SiO_2 sample, a color difference was observed between the edge and central regions of the circular patterns. During high-temperature annealing, the oxidation-induced expansion and densification-induced contraction of the poly-Si and SiO_2 progress at different rates across the region, resulting in a non-uniform optical thickness distribution and the observed ring-like color non-uniformity. Although the circular contours were preserved, most of the originally flat areas of the patterns exhibited "bulging." According to our previous work, increasing the thickness of the SiO_2 will cause the originally intact patterns to fracture, which is due to the severe thermal expansion and residual stress present in the SiO_2 film.[24] When the SiO_2 thickness was reduced to 150 nm, the colors in the preserved patterns were more uniform compared to patterns of the same area in the 300 nm case. A thinner SiO_2 thickness and smaller patterned area can alleviate the thermal expansion issues during oxygen annealing. However, the thinner thickness of SiO_2 reduces the tolerance of area-selective patterning etch. The thickness of SiO_2 needs to be precisely designed. In the following experiment, it is recommended that the thickness of PECVD SiO_2 does not exceed 150 nm.

4. Optimization process of area-selective patterning

4.1. The bird's beak-like shape structure formation and irregular bulges on the β-Ga_2O_3 wafer

In the patterning process, dry etching along with wet etching was performed to remove LPCVD poly-Si (450 nm) and PECVD SiO_2 (150 nm) beyond the protection region on β-Ga_2O_3 wafers with patterned photoresist (PR). Dry etching was performed in RIE system with SF_6/CHF_3 gases flow of 15/50 sccm, RIE power of 200 W, and chamber pressure of 20 mTorr. The calibrated etching rate for LPCVD poly-Si was 100 nm/min, and for PECVD SiO_2, it was 48 nm/min. The residual SiO_2 beyond the poly-Si mask region after dry etching was removed by wet etching in a buffered oxide etching (BOE) solution for 5 min, as shown in Fig. 5(a). After soaking the wafer in acetone solvent to remove the PR, it was placed in the furnace tube for oxygen annealing, as shown in Fig. 5(b).

As illustrated in Fig. 5(c), an irregular bulge appeared on the β-Ga_2O_3 wafer surface below the edge of the mask after oxygen annealing. It is speculated that the SiO_2 beneath the mask underwent lateral etching by the BOE solution after dry etching, exposing and suspending a part of poly-Si, which was thoroughly oxidized, the interface between the poly-Si and SiO_2 at the mask edges was oxidized inevitably. The connected oxidation regions from these two parts collectively form a bird's beak-like shape structure,[25–27] which strained the residual poly-Si and exerted pressure on the underlying β-Ga_2O_3 wafer, resulting in the deformation and the formation of bulges on the β-Ga_2O_3 wafer.

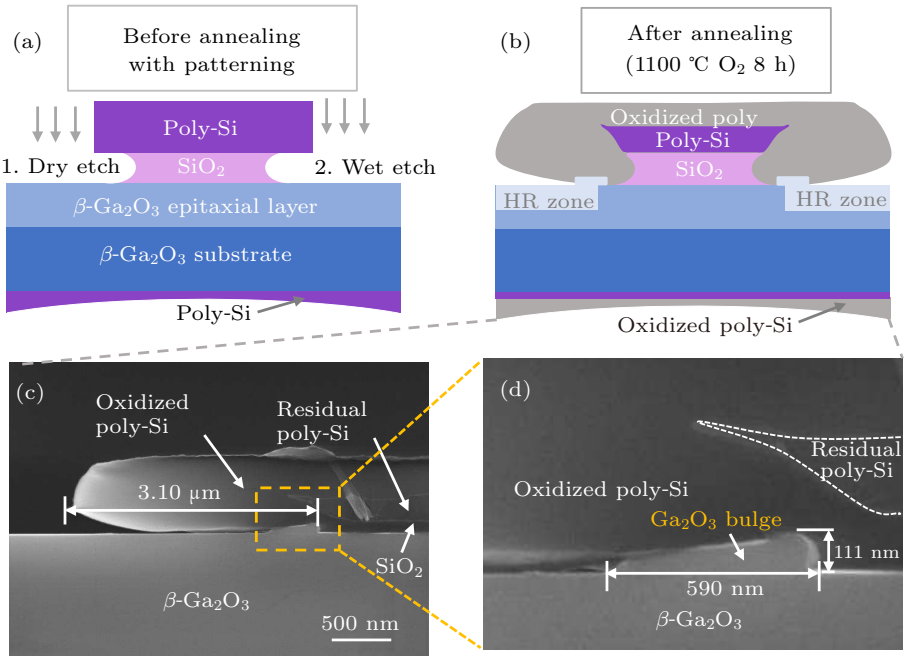


Fig. 5. The cross-section of the patterned β-Ga_2O_3 wafers deposited with PECVD SiO_2/poly-Si oxygen barrier layers (a) before and (b) after 1100 °C 8-h O_2 annealing. (c) A bird's beak-like shape structure was formed after oxygen annealing with a length of 3.1 μm. (d) The SEM image shows the local details of (c). There is an irregular bulge with a width of 590 nm and a height of 111 nm on the β-Ga_2O_3 wafer surface at the edge of the annealing mask, which may be caused by the expanded oxide of oxidized poly-Si.

After removing the annealing mask, the area-selective carrier concentration modulation wafer was deposited with Schottky contact metal on the frontside. As shown in Figs. 6(a)–6(d), four types SBDs were used to illustrate the impact of the bulges region on electrical characteristic using TCAD simulations in Silvaco Atlas. Device 1 is a reference SBD with a $N_D - N_A$ of $\sim 2 \times 10^{16}$ cm^{-3} of epitaxial layer. Device 2 is a high-resistance (HR) terminal SBD. Devices 3 and 4 are SBD with irregular bulges inside and outside the HR zone, respectively. Four types of devices were applied with a reverse bias of −1800 V on the anode electrode, the extracted electric field along the lateral direction near the wafer surface is illustrated in Fig. 6(e). Compared with device 1, the surface electric field and the peak electric field were reduced effectively due to the employment of the HR terminal on device 2. However, the irregular bulge induced two peak electric fields on the surface of devices 3 and 4, which even exceeded the effect of reducing the surface electric field by the HR terminal. As a result, the reverse leakage current of these devices increased, contributing to device instability. Therefore, it is necessary to avoid the generation of surface bulges during the oxygen annealing.

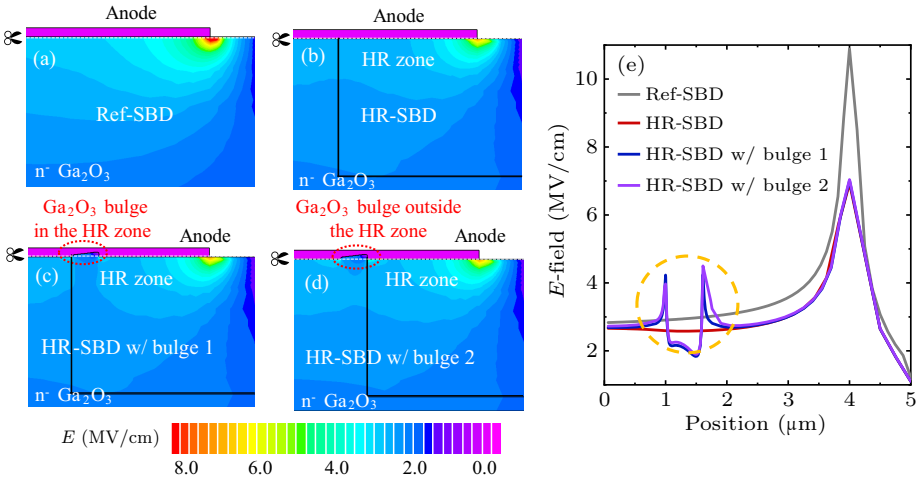


Fig. 6. (a)–(d) Simulation electric field distribution of four types of SBDs (Ref-SBD, HR-SBD, HR-SBD w/ bulge 1, HR-SBD w/ bulge 2) under a reverse bias of −1800 V. (e) Extracted electric field profile of the four types of devices along the lateral direction near β-Ga_2O_3 wafers surface.

4.2. Optimization of the etching process and the SiO_2 film characteristics

As shown in Fig. 7(a), the optimized process eliminated the wet etching process, adopting a multi-cycle dry etching process. Close manual monitoring was conducted during the etching of poly-Si to ensure complete removal of the surface poly-Si without etching into the surface of β-Ga_2O_3 wafer. It is worth noting that, based on our experimental experience, a quick and effective method to determine whether the poly-Si outside the masked area has been etched clean was to visually observe whether the masked pattern appears to "float" on the β-Ga_2O_3 wafer (the mask is opaque, while the β-Ga_2O_3 wafer is semi-transparent). According to Fig. 5, it is speculated that the exposed poly-Si due to the lateral etching of the BOE solution at the edge of the annealing mask created a pathway for oxygen to enter the interface between poly-Si and SiO_2. This optimized etching process avoided the lateral corrosion of SiO_2 and the exposure of the bottom surface of poly-Si at the edge region of mask. Meanwhile, the remaining SiO_2 layer outside the masked area also served as a stress buffer layer for the interface-thickened oxide. In addition, it has been proven that the CVD SiO_2 has a weak ability to block oxygen for the β-Ga_2O_3 epitaxial layer in high temperatures.[21] After annealing, the optimized patterned structure significantly improved the formation of bird's beak-like structures, although there are no bulges on the β-Ga_2O_3 surface, deformation still occurred, as shown in Fig. 7(c).

Based on the optimized etching process, we further refined the film characteristics of SiO_2 beneath the poly-Si. The parameters of two CVD deposition methods and films properties are summarized in Table 1. Stoney's formula was used to extract the thin film residual stress via SiO_2 thin film from stress induced bowing of the Si substrate.[28] The measured SiO_2 was deposition on 2 in. (100)-oriented Si wafer with 400 μm thickness. The compressive stress of inductively coupled plasma PECVD (ICP-PECVD) SiO_2 was lower than that of PECVD SiO_2 by 25%. As shown in Fig. 7(d), the surface of the β-Ga_2O_3 wafer after oxygen annealing with the mask is almost very smooth, indicating that the reduced compressive stress presented in ICP-PECVD SiO_2 effectively avoided deformation of the β-Ga_2O_3 wafer. Post-deposition stress-relief treatments, as well as advanced deposition techniques that provide improved uniformity and film density, may further facilitate the formation of low-stress films, thereby ensuring flatter edge morphology.

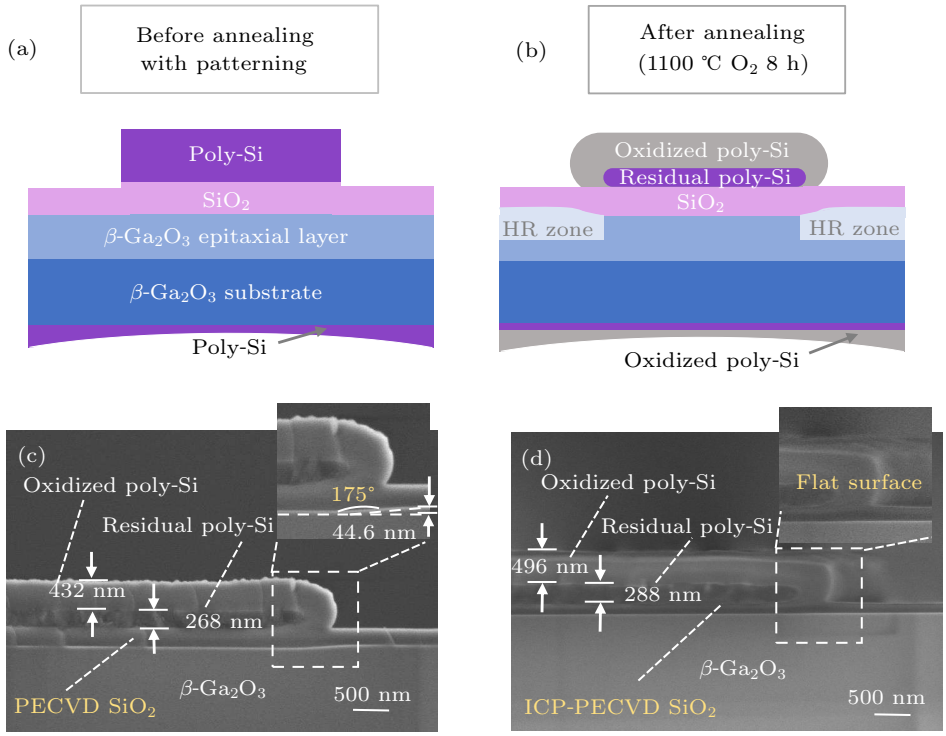


Fig. 7. The cross-section of the patterned β-Ga_2O_3 wafers deposited with ACL (a) before and (b) after 1100 °C 8-h O_2 annealing. The two SEM images show β-Ga_2O_3 wafers deposited with different SiO_2 by (c) PECVD and (d) ICP-PECVD after 1100 °C 8-h O_2 annealing. (c) Deformation of β-Ga_2O_3 wafer occurred beneath the edge of ACL, with an angle of 175°. (d) The surface of β-Ga_2O_3 wafer remained flat and smooth after oxygen annealing.

Table 1. CVD SiO_2 deposition parameters and measured films properties.

SiO_2 deposition method	RF power (W)	ICP power (W)	Pressure (mTorr)	Gases flow rate (sccm)	Deposition rate (nm/min)	Deposition temperature (°C)	Compressive stress (MPa)
PECVD	200	–	850	SiH_4/O_2 (130.5/13)	58	300	269.3
ICP-PECVD	–	500	7.5	SiH_4/N_2O (150/710)	20	130	209.7

5. Conclusion and perspectives

We have developed an optimized area-selective carrier concentration modulation technology based on high-temperature oxygen annealing method for β-Ga_2O_3 power devices. The 8-hour annealing time was a compromise choice that optimized the annealing process cost and the reduction in carrier concentration in the epitaxial layer of β-Ga_2O_3 wafer. According to SEM images, the thickness of poly-Si annealing cap layer was advised to be at least 185 nm. As for SiO_2, the etching stop layer and lift-off layer were advised to reduce to below 150 nm, which avoided the fracture of the mask on the β-Ga_2O_3 wafer after oxygen annealing. The optimizing etching process prevented the exposure of poly-Si and reduced the oxidized region at the edge of the mask, contributing to the disappearance of the bird's beak-like shape structure and bulges on the surface of the β-Ga_2O_3 wafer. Improving the film characteristics of SiO_2 beneath poly-Si further promoted the flatness of the β-Ga_2O_3 wafer after oxygen annealing. These results promote the cost-effective application of the β-Ga_2O_3 power devices.

Acknowledgements

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