Effect of heavy ion radiation on TDDB properties and lifetime prediction of high-*k* dielectric layers

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This study investigates the effect of heavy ion radiation on the time-dependent dielectric breakdown (TDDB) behavior of high-*k* dielectric layers. By testing and comparing parameters such as breakdown voltage, breakdown time, charge quantity, and dielectric layer lifetime before and after irradiation, and analyzing the underlying micromechanisms, the effect of heavy ion radiation on dielectric layer reliability is revealed. The results show that heavy ion radiation can induce defects in the dielectric layer. These defects play an important role in TDDB evolution, promote the formation of conductive paths, accelerate charge transport and defect accumulation, and ultimately degrade the breakdown time, charge quantity, and lifetime. Additionally, larger dielectric layer areas facilitate the formation of conductive paths, further exacerbating reliability degradation. This study provides a theoretical basis for optimizing device reliability in radiation environments.

Keywords: heavy-ion radiation, high-*k* dielectric layers, TDDB, lifetime prediction

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1. Introduction

With the advancement of Moore's law to the 3 nm and below process nodes, the thickness of gate dielectric layers has been reduced to 1–3 nm, approaching physical and quantum limits.[1,2] Traditional SiO_2 struggles to meet the requirements of advanced manufacturing processes due to its high tunneling current and insufficient breakdown field strength.[3] Meanwhile, the stringent reliability requirements for chips in fields such as artificial intelligence further highlight the urgency of optimizing gate dielectric reliability. High-*k* materials (such as hafnium oxide) can reduce leakage current and suppress short-channel effects while maintaining a relatively thick oxide layer. However, reliability concerns remain under long-term electrical stress.[4–6] Time-dependent dielectric breakdown (TDDB) is a key indicator for evaluating the long-term reliability of devices,[7] and its evolution may be affected by heavy ion radiation.[8–10] With the increasingly widespread application of 28 nm process devices in the aerospace field, these devices must operate over extended periods in harsh space radiation environments. Therefore, investigating the correlation between the TDDB characteristics of 28 nm-process ultrathin dielectric layers and heavy ion radiation has become an important topic in semiconductor reliability research.

In the space radiation environment, galactic cosmic rays (GCRs) are one of the major threats. GCRs are high-energy particles originating from outside the solar system within the Milky Way and consist of protons, alpha particles, and heavy ions. Their energy spectrum peaks in the range of hundreds of MeV to GeV. Due to their high linear energy transfer (LET) values, they can significantly affect microelectronic devices. Extensive research has been conducted on the effects of heavy ion radiation on dielectric layers and the TDDB characteristics of high-*k* dielectric layers. Heavy ion radiation adversely affects high-*k* dielectric layers. Li confirmed that Ta ion irradiation induces oxygen vacancy defects in high-*k* dielectrics using high-resolution transmission electron microscopy (HRTEM) and x-ray diffraction (XRD).[11] Radiation not only introduces additional defects and alters charge transport, leading to reliability degradation, but can also exacerbate this degradation. Moreover, the higher the radiation fluence, the more pronounced the degradation of gate dielectric layers, and relevant studies have further confirmed the adverse effects of radiation on gate dielectric reliability.[12–15] Regarding the TDDB characteristics of high-*k* dielectric layers, the defect generation mechanisms in high-*k* dielectrics differ significantly from those in silicon dioxide dielectrics, particularly in the more complex behavior of oxygen vacancies. Additionally, multi-stress conditions can alter the elec-

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tron and hole trapping and detrapping processes, thereby affecting the TDDB characteristics of hafnium silicon oxynitride dielectrics.[16,17]

Existing studies have yielded substantial results on the effects of heavy ion radiation on dielectric layers and the TDDB characteristics of high-k dielectric layers. However, the correlation between these two areas remains insufficiently explored. Specifically, most TDDB studies do not account for radiation effects, limiting the reliable assessment of device reliability under specialized operating conditions. Given that p-channel metal–oxide–semiconductor (PMOS) capacitors with high-k gate dielectric structures are fundamental components of 28 nm-process devices, this study selects such capacitors as the research objects and systematically investigates the effects of heavy ion radiation on the TDDB characteristics of high-k dielectric layers. It also elucidates the radiation-induced mechanisms and the influence of dielectric layer area on radiation-induced degradation. This work aims to improve the theoretical understanding of the reliability of high-k dielectric layers under heavy ion radiation and provide technical support for the radiation-hardened design and lifetime prediction of integrated circuits operating in extreme environments.

2. Experimental devices and conditions

The samples used in this experiment are PMOS capacitors fabricated using the 28 nm process by the Beijing Microelectronics Technology Institute. The equivalent physical thickness of the high-k gate dielectric layer is 6.19 nm. The capacitors have two different areas, corresponding to dimensions of 2 μm × 2 μm and 20 μm × 20 μm, respectively. The experimental samples were divided into two groups: one group was subjected directly to TDDB testing, while the other underwent TDDB testing after irradiation. A high-precision semiconductor parameter analyzer (Keysight B1500A) was used to apply gate stress to both groups of MOS capacitors and measure their breakdown characteristics.

The samples were subjected to heavy ion irradiation at the Institute of Modern Physics, Chinese Academy of Sciences, in Lanzhou. The Heavy Ion Research Facility in Lanzhou (HIRFL) was used as the radiation source, providing $^{181}Ta^{35+}$ ions. These ions were used for the heavy-ion irradiation experiments. The irradiation was performed at room temperature. The ion energy at the sample surface was 2560 MeV, corresponding to a linear energy transfer (LET) of 70.06 MeV/(mg/cm^2). The fluence rate was 1×10^5 ions/(s·cm^2), and the total fluence was set to 7×10^6 ions/cm^2.

3. Experimental results and analysis

To determine the withstand voltage range of the PMOS capacitors, a voltage-ramp (V-ramp) test was first conducted to determine their breakdown voltages. This test provided a key basis for selecting the stress voltage in the subsequent TDDB tests.

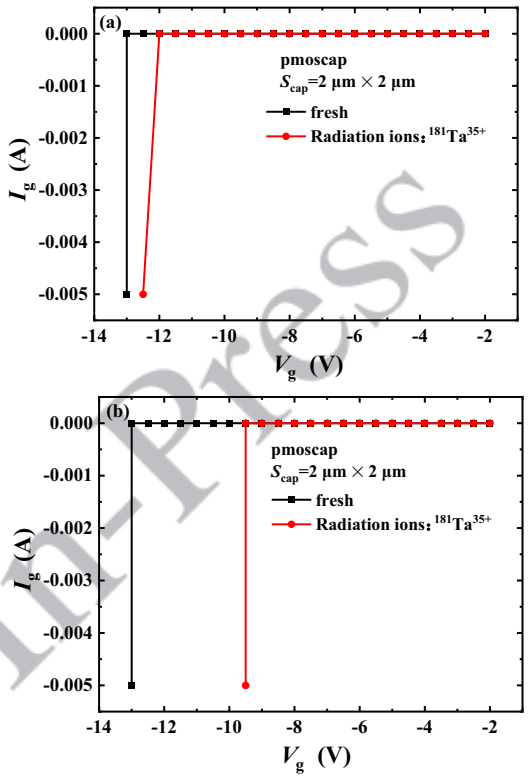


Fig. 1. Breakdown voltages of PMOS capacitors of different sizes before and after irradiation. (a) $S_{cap} = 2\ \mu m \times 2\ \mu m$. (b) $S_{cap} = 20\ \mu m \times 20\ \mu m$.

Figure 1 presents the breakdown voltage test results of PMOS capacitors before and after irradiation. A comparison of the test data shows that, before irradiation, the breakdown voltages of PMOS capacitors with different areas are approximately −13 V. After irradiation, the breakdown voltage of small-area PMOS capacitors decreases to −12.5 V, while that of large-area PMOS capacitors decreases to −9.5 V. These results indicate that radiation reduces the breakdown voltage of PMOS capacitors, with the extent of degradation depending on the capacitor area.

Figure 2 shows the gate current (I_g) characteristics of small-area PMOS capacitors under different gate voltage stresses before and after irradiation, plotted on log-log coordinates. Before irradiation, the gate current transport in the device follows the Fowler–Nordheim tunneling mechanism.[18] As the absolute value of the negative gate voltage increases, the electric field in the gate dielectric strengthens, increasing the carrier tunneling probability and shortening the breakdown time. Specific observations can be made from the figure. For example, the breakdown time is approximately 350 s at $V_g = -11$ V and increases to approximately 600 s when the absolute value of the negative gate voltage decreases to $V_g = -10.5$ V. After irradiation, at the same gate voltage of $V_g = -10.5$ V, the breakdown time decreases to approxi-

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mately 20 s. These results demonstrate that radiation accelerates breakdown, leading to rapid failure even at relatively low gate voltages.

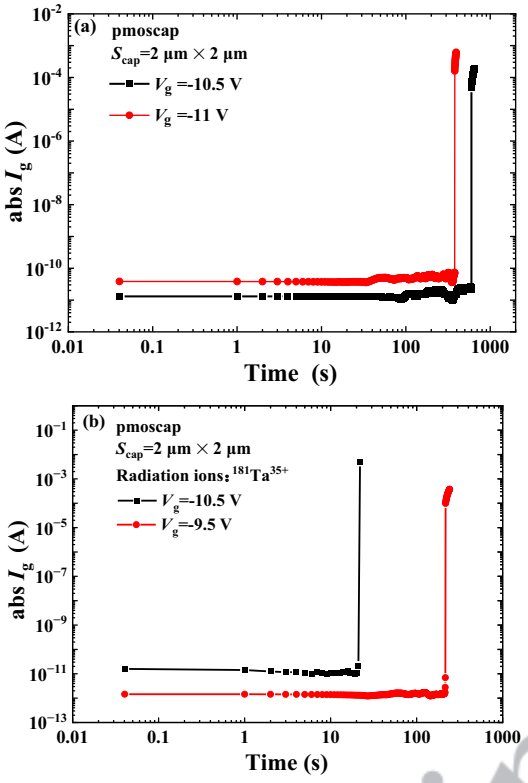


Fig. 2. Relationship between gate current (I_g) and time (T) of small-area PMOS capacitors under different gate voltages in log–log coordinates. (a) Before irradiation. (b) After irradiation.

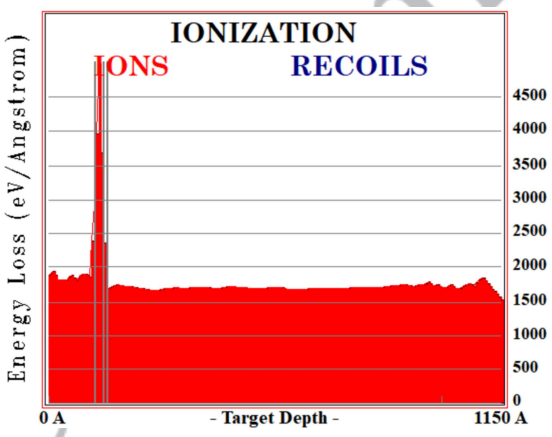


Fig. 3. Distribution map of ion energy loss.

Figure 3 presents the distribution of ion energy loss under heavy ion irradiation. In the dielectric layer, the incident ions collide intensely with electrons, resulting in significant energy loss and making the layer more susceptible to radiation-induced damage.

The defect-dominated breakdown process is fundamentally consistent with the conductive filament formation mechanism in memristive systems. In memristive systems, the failure mechanism stems from the accumulation of dielectric defects (predominantly oxygen vacancies) driven by an electric field, forming conductive filaments and ultimately triggering device breakdown.[19,20] In this study, the distribution of defects in the dielectric layer before and after irradiation is schematically illustrated in Fig. 4. Radiation induces defects in the gate dielectric.[21] When electrical stress is applied, additional defects are generated. These defects contribute to the formation of conductive paths (similar to the conductive filaments in memristive systems), significantly accelerating charge transport and energy dissipation in the gate dielectric during the TDDB process.

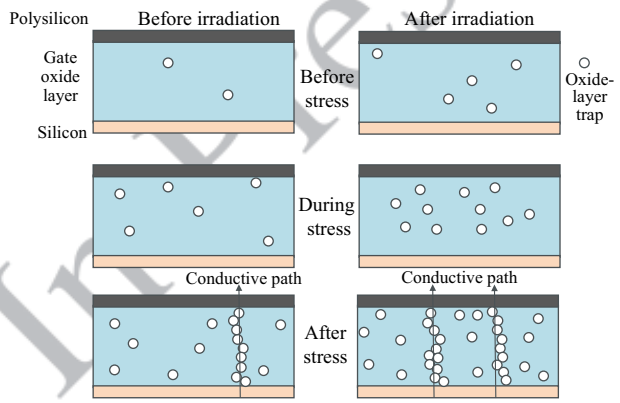


Fig. 4. Schematic illustration of the defect distribution in the dielectric layer before and after irradiation.

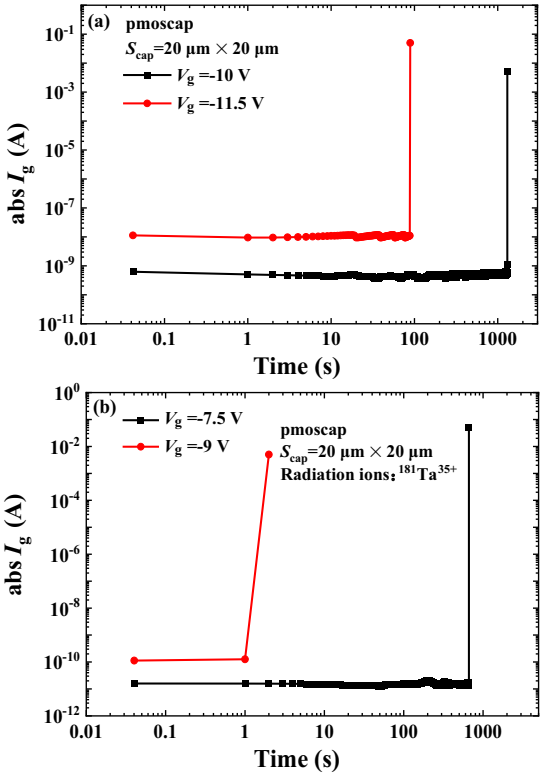


Fig. 5. Relationship between gate current (I_g) and time (T) of large-area PMOS capacitors under different gate voltages in log–log coordinates. (a) Before irradiation. (b) After irradiation.

Figure 5 shows the gate current (I_g) characteristics of large-area PMOS capacitors under different gate voltage

stresses before and after irradiation, plotted on log–log coordinates. Comparative analysis indicates that large-area PMOS capacitors exhibit the same trend as small-area devices, with breakdown time decreasing as the absolute value of the negative gate voltage increases. After heavy-ion irradiation, the breakdown time of large-area PMOS capacitors also decreases markedly. The data show that the post-irradiation lifetime under the lower gate stress ($V_g = -7.5$ V) is already shorter than the pre-irradiation lifetime under the higher stress ($V_g = -10$ V), further confirming that radiation degrades the gate dielectric breakdown characteristics.

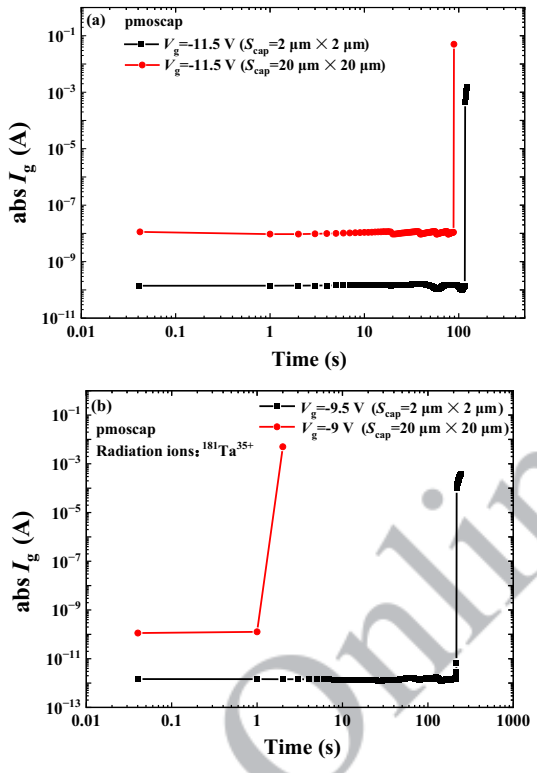


Fig. 6. Relationship between gate current (I_g) and time (T) for PMOS capacitors with different areas before and after irradiation, plotted on log–log coordinates. (a) Before irradiation. (b) After irradiation.

Figure 6(a) shows the gate current characteristics of PMOS capacitors with different areas before irradiation, plotted on log–log coordinates. Under the same gate voltage stress, the breakdown time of large-area devices is slightly shorter than that of small-area devices, although the difference is small. Before irradiation, the dielectric layer contains no additional radiation-induced defects. Therefore, the capacitor area has a relatively small impact on the formation of conductive paths and the breakdown time. Figure 6(b) presents the gate current (I_g) characteristics of devices with different areas after irradiation. After heavy ion irradiation, the breakdown voltages of large- and small-area devices differ, measuring -9.5 V and -12.5 V, respectively. Therefore, the large-area capacitor is subjected to a gate voltage of $V_g = -9$ V, while the small-area capacitor is subjected to $V_g = -9.5$ V, precluding a direct comparison under the same voltage conditions. The figure shows that even under a lower gate voltage stress, the breakdown time of large-area devices is shorter than that of small-area devices, indicating that radiation-induced defects have a more pronounced impact on the breakdown characteristics of large-area devices.

A comparison between Figs. 6(a) and 6(b) reveals that radiation markedly degrades the dielectric breakdown strength, with more pronounced degradation in larger-area devices. As shown in Fig. 7, heavy ion irradiation induces defects in the high-k dielectric layers. During the TDDB process, additional defects are also generated in the dielectric layers. The combined effects of radiation-induced and stress-induced defects make the dielectric layers more susceptible to conductive path formation after irradiation, thereby accelerating breakdown. Larger dielectric layers can accommodate more conductive paths, and the formation of any one conductive path can cause dielectric breakdown.[22] Therefore, larger-area devices exhibit more severe TDDB degradation than smaller-area devices.

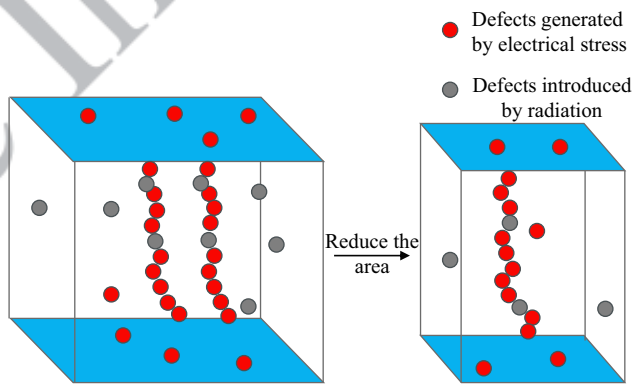


Fig. 7. Defect distribution in dielectric layers of different areas after irradiation.

Figure 8 shows the breakdown charge of PMOS capacitors with different areas before and after irradiation. "abs Q" denotes the absolute value of the accumulated charge before dielectric breakdown, obtained by integrating the gate current (I_g) with respect to time. As shown in Fig. 8(a), before irradiation, the areas of the PMOS capacitors differ by two orders of magnitude, and their breakdown charges also differ by two orders of magnitude. Therefore, the breakdown charge densities of dielectric layers with different areas are approximately the same. However, as shown in Fig. 8(b), the device characteristics change significantly after irradiation. Although the total breakdown charge of large-area PMOS capacitors remains higher than that of small-area devices, the reduction in their charge density is much greater, and the changes in charge density differ substantially between the two device sizes. This phenomenon further indicates that radiation induces defects in the dielectric layer, which can connect with those subsequently induced by electrical stress. After irradiation, large-area devices have a higher probability of forming conductive paths

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than small-area devices because of their larger area, leading to earlier dielectric breakdown and thereby reducing their effective charge-carrying capacity.[22]

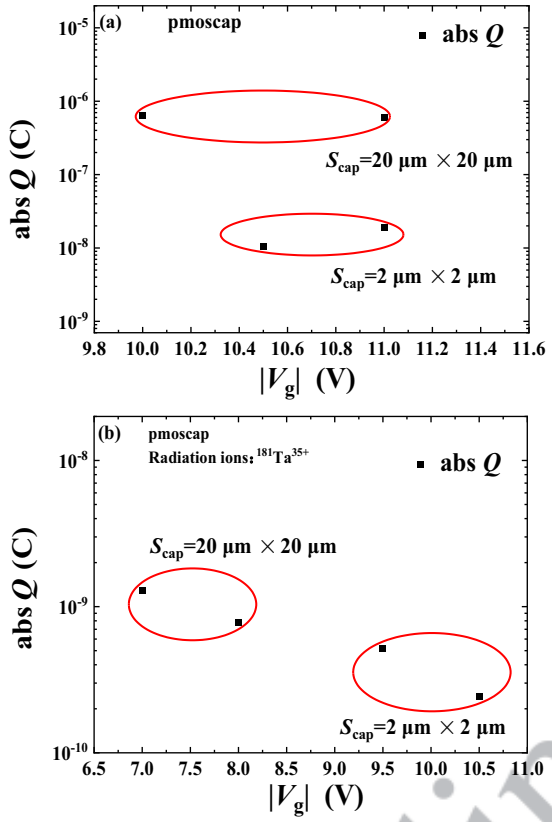


Fig. 8. Relationship between breakdown charge (abs Q) and gate voltage (V_g) for PMOS capacitors with different areas before and after irradiation. (a) Before irradiation. (b) After irradiation.

After accurately determining t_{BD} in TDDB tests under different gate stresses, we used different models to predict the TDDB lifetime of the dielectric layers, as shown in Fig. 9.

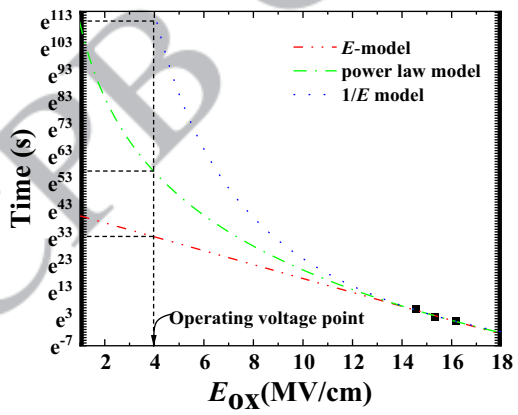


Fig. 9. Comparison of three lifetime extrapolation models.

Figure 9 presents the performance of the E-model, $1/E$ model, and power-law model in extrapolating the TDDB lifetime of MOS capacitors. At an operating voltage of 2.5 V, the predictions of the $1/E$ and power-law models differ from that of the E-model by dozens of orders of magnitude, whereas the E-model provides predictions that are highly consistent with the actual lifetime. In TDDB studies of high-k dielectrics, the physical basis of the E-model is the field-driven evolution of defects, which dominates dielectric breakdown. The E-model is applicable under both high and low electric-field conditions.[23,24] Compared with the other models, the E-model offers greater adaptability and advantages. The $1/E$ model is based on electron tunneling in dielectrics and is suitable for lifetime prediction under high electric-field conditions. However, under low electric-field conditions, the lifetime predicted by the $1/E$ model is often higher than the actual lifetime.[25] The power-law model is based on reactions involving protons and is suitable for devices with dielectric layers thinner than 2 nm.[26] Considering the actual characteristics of the devices, the E-model is the most suitable for predicting their lifetime.

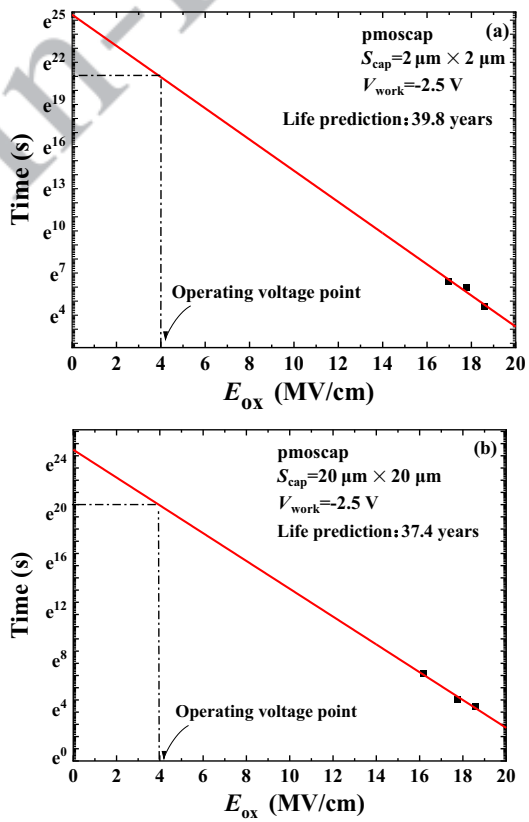


Fig. 10. Lifetime prediction for PMOS capacitors with different areas before irradiation, plotted on log–log coordinates. (a) S_{cap} = 2 μm × 2 μm. (b) S_{cap} = 20 μm × 20 μm.

Figures 10 and 11 show the fitting curves of electric field intensity versus breakdown time for PMOS capacitors with different areas before and after irradiation, plotted on log–log coordinates. By substituting the operating voltage of 2.5 V into the extrapolation, the lifetimes of the samples under the operating voltage were estimated. As shown in the figures, the lifetimes of all capacitors decrease after irradiation, but the lifetime degradation of large-area devices is more severe than that of small-area devices. This indicates that large-area

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devices are more significantly affected by radiation, consistent with the conclusions presented earlier. Radiation induces defects in the dielectric layer, and the defects introduced by radiation and electrical stress can connect to form conductive paths. The larger the device area, the more likely conductive paths are to form within the dielectric layer. The formation of these coupled defects and conductive paths ultimately reduces the dielectric layer's lifetime, with larger dielectric layers exhibiting a more pronounced reduction in device lifetime.

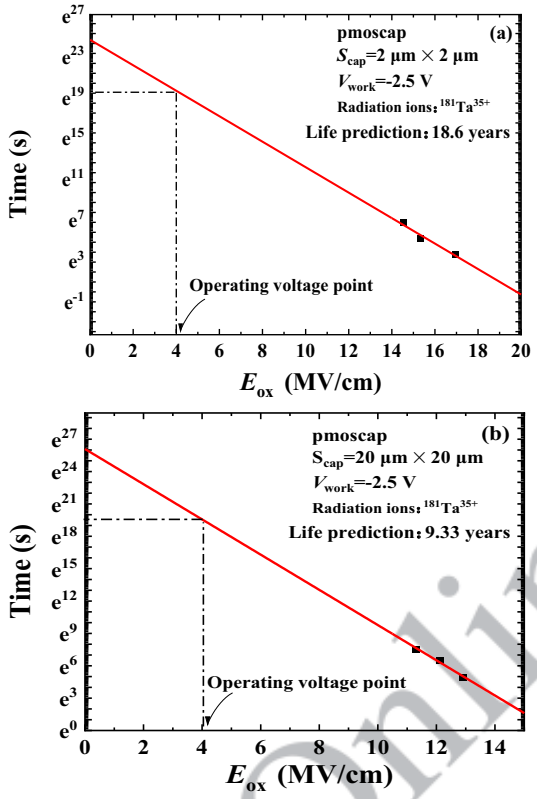


Fig. 11. Lifetime prediction for PMOS capacitors with different areas after irradiation, plotted on log–log coordinates. (a) $S_{cap} = 2\ \mu m \times 2\ \mu m$. (b) $S_{cap} = 20\ \mu m \times 20\ \mu m$.

4. Conclusion

This study investigates the effects of Ta heavy ion irradiation on the TDDB characteristics of high-*k* dielectric layers in 28 nm-process PMOS capacitors with different areas. The results show that heavy ion irradiation induces defects in the dielectric layer, significantly degrading the breakdown characteristics of the capacitors. After irradiation, the breakdown voltage, breakdown time, dielectric layer charge density, and device lifetime all decrease significantly. Moreover, the larger the dielectric layer area, the more severe the radiation-induced degradation. This is manifested in a shorter breakdown time, a greater reduction in charge density, a larger decrease in lifetime, and an increased likelihood of conductive path formation through the connection of defects introduced by radiation and electrical stress, thereby accelerating dielectric breakdown. These findings provide a theoretical reference for radiation-hardened design and lifetime prediction of integrated circuits fabricated using the 28 nm process.

Acknowledgments

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