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Influences of trapping on the operating characteristics and high-power microwave damage effect of AlGaAs/InGaAs pHEMT devices

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High-power microwaves (HPM) coupled into a low-noise amplifier (LNA) through antennas pose a significant threat to the reliability of pseudomorphic high electron mobility transistor (pHEMT). In this paper, the effects of introducing donor and acceptor traps into GaAs/InGaAs pHEMT devices on their operating characteristics and HPM damage effect are systematically studied. Simulation results show that introducing donor traps with a concentration of 1×10^{18} cm^{-3} and an energy level of $E_c - 0.6$ eV in the substrate layer, and acceptor traps with a concentration of 1×10^{18} cm^{-3} and an energy level of $E_v + 0.6$ eV in the isolation layer, can reduce the internal peak temperature of the device by 756 K and 658 K, respectively, under HPM exposure. The physical mechanism of trapping influencing the HPM effect is mainly due to ionized traps forming positive and negative charge centers, which generate an internal electric field opposing the external field. This weakens the electric field in the barrier layer, reducing carrier accumulation from avalanche breakdown during the positive half-cycle of the HPM pulse. These results are valuable for enhancing the reliability of LNA in complex electromagnetic environments.

Keywords: AlGaAs/InGaAs pHEMT, high-power microwave (HPM), trapping, low-noise amplifiers (LNA), reliability

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1. Introduction

GaAs pseudomorphic high electron mobility transistors (pHEMTs), due to their high electron mobility, excellent thermal stability, and low noise figure, are widely used in low-noise amplifiers (LNAs) for RF front-end applications.[1,2] LNAs play a crucial role in amplifying signals and ensuring the proper functioning of RF circuits. As the external electromagnetic environment becomes more complex, strong electromagnetic signals, such as high-power microwaves (HPM), can couple with antennas and enter the system. The LNA, being part of the RF front-end, is one of the first components to be affected. Under HPM exposure, the LNA may experience functional degradation or even failure, leading to the malfunction of the entire RF receiver circuit.[3,4] As the core component of the LNA circuit, GaAs HEMTs are the most vulnerable to HPM exposure. Therefore, studying the HPM damage mechanisms and protection techniques for GaAs HEMT devices is critical for improving the reliability of LNAs in complex electromagnetic environments.

Existing studies on HPM damage effects in LNA mainly use circuit-level injection experiments to observe changes in key parameters like gain, noise figure, and operating current, helping to determine the damage threshold.[5] In contrast, device simulations are often employed to analyze the HPM damage mechanism, injecting HPM at the device port and assessing changes in critical physical parameters such as electric field, current density, and temperature.[6–12] Wang *et al.* confirmed through pulse injection experiments and simulations that the failure mechanism of GaN HEMT devices during pulse injection is localized avalanche breakdown. The formation of thermal–electrical positive feedback results in continuous heat accumulation, ultimately causing thermal failure.[13] Li *et al.* found that, for certain pulse widths, the device failure is caused by the coupling of thermoelectric multiphysics fields.[14] Both the pulse voltage injection experiment on LNAs and devices lead to the conclusion that the main failure mechanism of GaAs HEMTs is localized avalanche breakdown below the gate, ultimately resulting in thermal breakdown.[15–18] Existing studies have shown that the failure of HEMT under HPM exposure is strongly related to the distribution of electric fields and currents. Extensive research has shown that introducing traps in GaN HEMT can alter electric field distributions, effectively adjusting current and on-

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resistance.[19–24] However, similar studies on GaAs HEMT are scarce, and research on the impacts of trap introduction on GaAs HEMT HPM effect is even more limited.

In this work, we developed a typical GaAs HEMT model as described in Ref. [25] and utilized TCAD simulation to systematically investigate the effects of donor and acceptor trap doping positions, concentrations, and energy levels on the output characteristics of GaAs HEMT. Furthermore, we explored the impact of trap introduction on the HPM damage effect. Through comparative analysis, we identified a trapping scheme that can enhance the HPM resistance of the device without causing a significant degradation in output characteristics.

2. Simulation model

Figure 1 shows the schematic structure of the AlGaAs/InGaAs pHEMT. The structure consists of a 10-nm InGaAs channel layer, a 34.5-nm $Al_xGa_{1-x}As$ barrier layer (where $x = 0.3$), a 30-nm GaAs cap layer, and a 50-nm Si_3N_4 sacrificial layer, all built on a GaAs substrate. The source and drain are Ohmic contacts, and the gate is a metal electrode, with a Schottky barrier of 0.9 eV. For thermal boundary conditions, the GaAs substrate is set as a heat exchange boundary, while all other interfaces are adiabatic, with the initial temperature of the device set to 300 K. The hydrodynamics model, high-field saturation model, doping-dependence mobility model, Shockley–Read–Hall (SRH), Auger, and avalanche models are considered in this study.

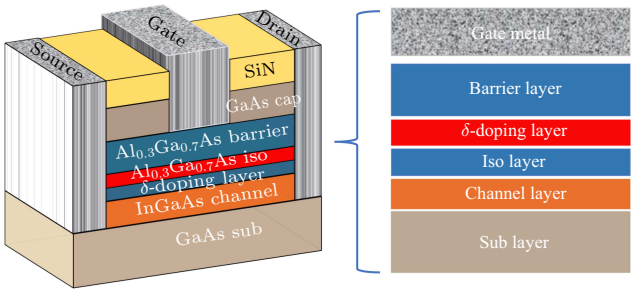

Fig. 1. Schematic diagram of the GaAs pHEMT device structure.

Table 1. Common doping impurities and their energy level distribution in GaAs.

Doping elements	Energy level	Properties	Remarks
Zn	E_v+ 0.021~0.026 eV	shallow acceptor	Su *et al.*[26]
Cd	E_v+ 0.36 eV	shallow acceptor	Huth *et al.*[27]
Si	E_c− 0.0058 eV	shallow donor	
	E_v+ 0.035 eV	shallow acceptor	
C	E_v+ 0.026 eV	shallow acceptor	Sze and Ng[28]
Fe	E_v+ 0.52 eV	deep acceptor	
Cr	E_v+ 0.63 eV	deep acceptor	
O	E_c− 0.67 eV	deep donor	

Table 1 presents the experimentally determined doping impurities and their energy levels in GaAs.[26–28] Based on the measured impurity and energy level distribution in GaAs, in this study, the trap concentrations are set within the range of 1×10^{15} cm^{-3} to 1×10^{18} cm^{-3}, the energy levels of acceptor trap and donor trap are set within the range of E_v+ 0 eV to E_v+ 0.6 eV and E_c− 0 eV to E_c− 0.6 eV, respectively, ensuring that these trap conditions can be achieved through doping in practical engineering. According to the test results in Refs. [29,30], the capture cross-section for both donor and acceptor traps in this paper is set to 2.5×10^{-16} cm^2.

Figure 2 shows the schematic diagram of the HPM waveform and bias conditions in this study. The GaAs pHEMT device is injected with the voltage pulse with a rising time of 1 ns and an amplitude of 10 V on the gate. Here, 2 V is applied to the drain and the source is grounded.

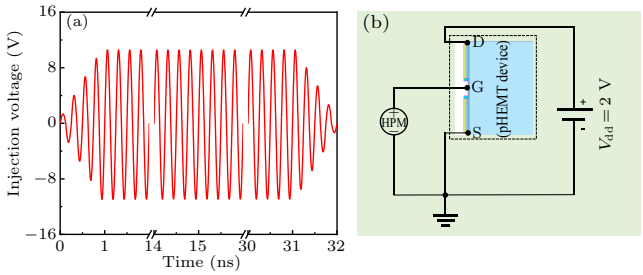

Fig. 2. (a) Schematic diagram of the HPM waveform and (b) bias conditions in the HPM injection simulation experiment.

3. Results and discussion

3.1. Influences of trapping on operating characteristics

Figure 3 shows the transfer characteristic curves with varying concentrations and energy levels of traps introduced in different layers. The impact of traps on key operating parameters, such as threshold voltage, off-state current, and saturation output current, can be determined from the changes in the transfer characteristic curves.

Figures 3(a)–3(c) show that introducing deep donor traps with an energy level of E_c− 0.6 eV in different layers results in a minimal effect on the off-state current and maximum output current. As the trap concentration increases, a slightly negative shift in the threshold voltage was observed; this is because when donor traps ionize, they increase the channel electron concentration and cause the device to turn on earlier. For deep donor traps, the ionization energy is high, and only a small portion of the traps undergo ionization, leading to a relatively small impact of trap concentration on the threshold voltage.

Figures 3(d)–3(f) show the transfer characteristic curves under donor trapping with different energy levels. It is evident that the trap energy level variation in the isolation and barrier layers has little effect on the off-state current and threshold voltage. This is primarily because the isolation and barrier layers are thin, resulting in a limited number of ionized electrons. In contrast, the thicker substrate layer generates a sig-

nificant number of ionized electrons, which affects the channel electron concentration. As shown in Fig. 3(d), the threshold voltage shifts significantly in the negative direction as the donor trap energy level decreases, while the off-state current increases notably. Shallow donor traps have lower ionization energies, so as the energy level decreases, the ionization degree of the traps increases.

Figures 3(a)–3(c) show that introducing deep donor traps with an energy level of $E_c - 0.6$ eV in different layers results in a minimal effect on the off-state current and maximum output current. As the trap concentration increases, a slightly negative shift in the threshold voltage was observed; this is because when donor traps ionize, they increase the channel electron concentration and cause the device to turn on earlier. For deep donor traps, the ionization energy is high, and only a small portion of the traps undergo ionization, leading to a relatively small impact of trap concentration on the threshold voltage.

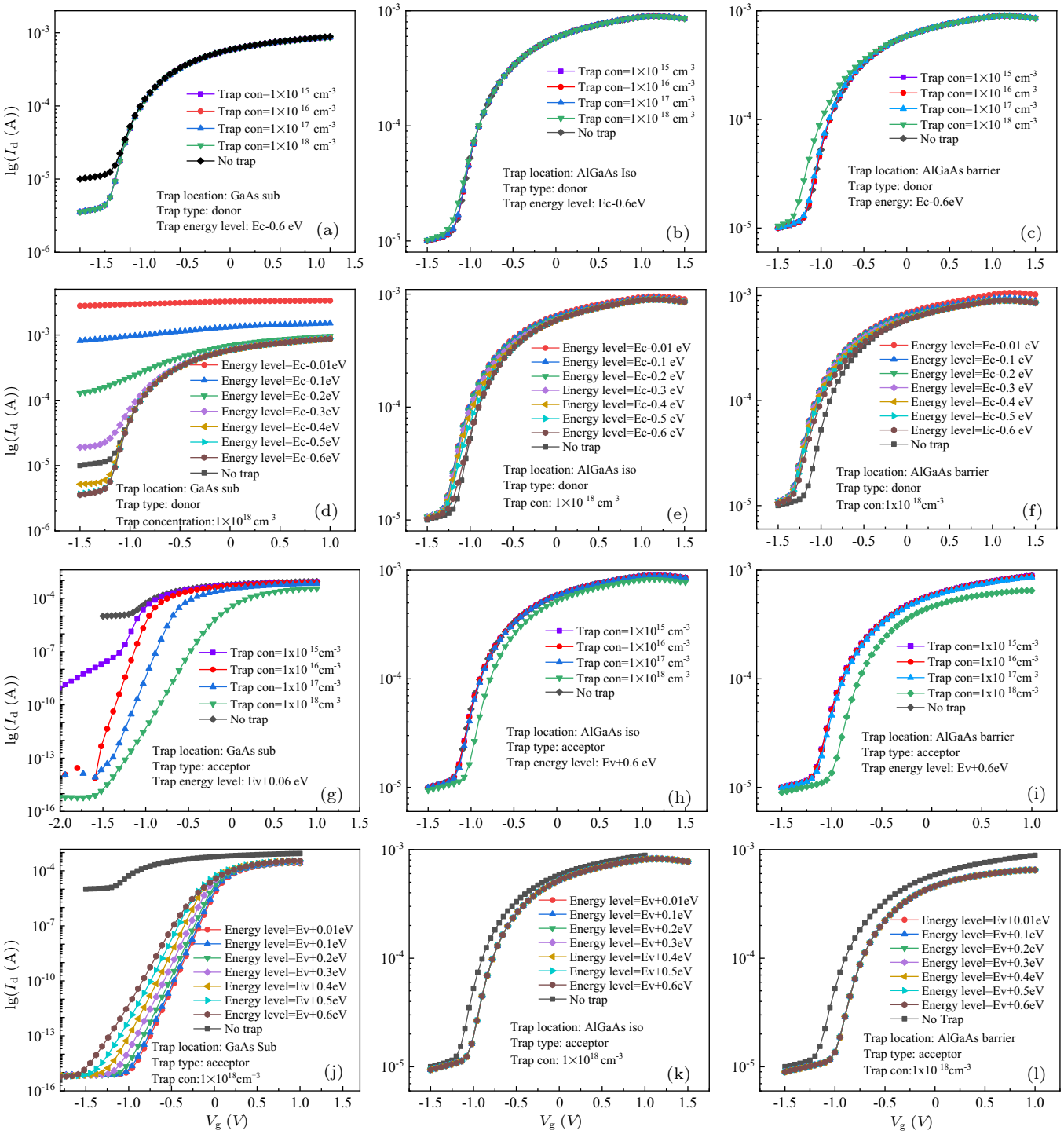

Fig. 3. Transfer characteristic curves of GaAs pHEMT under different trap doping locations, energy levels, and concentrations.

As shown in Fig. 3(g), introducing acceptor traps in the substrate leads to a significant reduction in off-state current as the trap concentration increases. This is because the acceptor traps capture free electrons, reducing the substrate leakage current. However, this also lowers the channel electron concentration, which decreases the maximum output current. Similarly, Figs. 3(h) and 3(i) show that as the acceptor trap concentration increases in the isolation and barrier layers, the maximum output current decreases significantly. This is mainly because deep acceptor traps in the barrier and isolation layers are more likely to remain in their ionized state, forming negative charge centers, which depletes the channel electrons and reduces the maximum output current.

Figures 3(j)–3(l) show the impact of acceptor trap energy level on transfer characteristics. Adding acceptor traps to different layers results in a positive shift in the threshold voltage and a reduction in the maximum output current. The degree of change in threshold voltage and maximum output current increases as the trap energy level decreases. A lower trap energy level increases the ionization of traps, meaning more free electrons are captured, reducing the channel electron concentration, which in turn causes the threshold voltage to shift positively and the maximum output current to decrease.

Figures 4(b) and 4(c) illustrate the electron release process after donor trapping in the barrier and substrate layers, respectively. The electric field strength in the barrier layer is higher than that in the substrate under HPM injection, making it easier for deep donor traps in the barrier layer to ionize, forming positive charge centers. In contrast, deep traps in the substrate are less likely to ionize, leading to a smaller impact of deep donor trap concentration on off-state current and saturation output current (as shown in Fig. 3(a)). Figures 4(d) and 4(e) depict the electron capture process after acceptor trapping in the barrier and substrate layers, respectively.

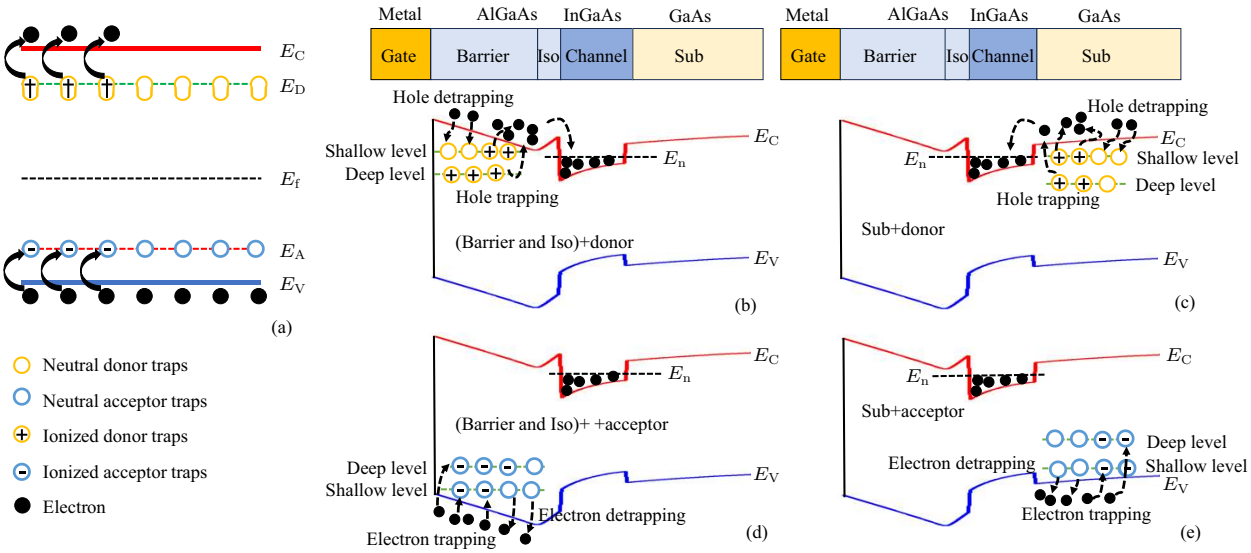

Fig. 4. The electron capture and release processes in the substrate and barrier layer of GaAs pHEMT.

In this study, the Fermi level is located within the forbidden band, and $(E_d - E_F) \gg kT$ holds. For donor traps, the distribution function of electrons occupying the donor energy level is given by

$$n_d = 2N_d \exp\left[\frac{-(E_d - E_F)}{kT}\right], \tag{1}$$

where n_d represents the electron occupancy density at the donor trap energy level, N_d is the donor atom concentration, E_d is the donor trap energy level, E_F is the Fermi level, k is the Boltzmann constant, and T is the temperature.

Additionally, the Boltzmann approximation holds for conduction band electrons, and the thermal equilibrium concentration of conduction band electrons is given by

$$n_0 = N_c \exp\left[\frac{-(E_c - E_F)}{kT}\right], \tag{2}$$

where n_0 and N_c represent the thermal equilibrium concentration of conduction band electrons and the effective density of states in the conduction band, respectively.

The ratio of electrons in the donor energy level to the total number of electrons (including electrons in the donor energy level and conduction bands) determines the degree of ionization.

$$\frac{n_d}{n_d + n_0} = \frac{1}{1 + \frac{N_c}{2N_d}\exp\left[\frac{-(E_c - E_d)}{kT}\right]}. \tag{3}$$

From Eq. (3), it is evident that as N_d increases, the ionization degree decreases, which also explains the increase in donor trap concentration in Figs. 3(a)–3(c), with minimal changes in the device transfer characteristics. Furthermore, as E_d decreases, the ionization degree of donor traps increases, which is consistent with the results shown in Figs. 3(d)–3(f),

where a decrease in the donor energy level leads to an increase in off-state current and a larger negative shift in the threshold voltage.

Similarly, for acceptor traps, the distribution function for hole occupancy in the acceptor energy level is given by

$$p_{\mathrm{a}} = 4N_{\mathrm{a}} \exp\left[\frac{-(E_{\mathrm{F}} - E_{\mathrm{a}})}{kT}\right], \tag{4}$$

where p_{a}, N_{a}, and E_{a} represent the hole occupancy density in the acceptor energy level, the acceptor atom concentration, and the acceptor energy level, respectively.

$$p_0 = N_{\mathrm{V}} \exp\left[\frac{-(E_{\mathrm{F}} - E_{\mathrm{V}})}{kT}\right], \tag{5}$$

$$\frac{p_{\mathrm{a}}}{p_{\mathrm{a}} + p_0} = \frac{1}{1 + \dfrac{N_{\mathrm{V}}}{4N_{\mathrm{a}}} \exp\left[\dfrac{-(E_{\mathrm{a}} - E_{\mathrm{V}})}{kT}\right]}, \tag{6}$$

where p_0 and N_{V} represent the thermal equilibrium concentration of valence band holes and the effective density of states in the valence band, respectively.

From Eq. (6), it can be seen that as N_{a} increases, the proportion of holes occupying the acceptor energy level relative to the total hole concentration increases, indicating a reduction in the ionization degree of acceptor traps with higher concentration. Although the ionization degree of acceptor traps decreases with concentration, the total number of ionized acceptor traps still rose, especially in the substrate layer. This explains the significant decrease in the off-state current with increasing concentration, as shown in Fig. 3(g). Furthermore, as E_{a} decreases, the ionization degree of acceptor traps increases, resulting in more captured electrons. This leads to a larger positive shift in the threshold voltage and a greater reduction in maximum output current, as shown in Figs. 3(j)–3(l).

3.2. Influences of trapping on HPM effect

Based on the above discussion, it can be concluded that introducing traps with different energy levels and concentrations at various locations in a GaAs pHEMT results in releasing or capturing electrons, thereby affecting the current density. Additionally, ionized deep traps form positive and negative charge centers, creating an internal electric field that influences the local electric field distribution. Under HPM exposure, electromagnetic field energy couples into the device, leading to thermal melting and eventual device failure. The formula for heat generation within the device is as follows:

$$Q = |J \cdot E|, \tag{7}$$

where Q represents the Joule heat, J is the current density, and E is the electric field strength.

From Eq. (7), it can be seen that the heat generation power of the device in a strong electromagnetic environment is primarily determined by the current density and electric field strength. Traps can influence the current density by capturing and releasing electrons, while also creating positive and negative charge centers that affect the local electric field strength. Therefore, in this study, we will further analyze the impacts of trap introduction on the HPM-induced thermal damage effects.

Figure 5 shows the peak temperature curves within the device for different concentrations and energy levels of traps introduced. Under HPM conditions, the primary failure mode is thermal failure, where the local temperature exceeds the melting point of GaAs (1511 K). By comparing the temperature rise curves of defect-free devices with those of devices with introduced defects, the impact of trap introduction on the HPM-induced damage can be assessed.

From the temperature rise curves in Figs. 5(a)–5(f), it can be seen that the introduction of donor traps in the isolation and barrier layers does not significantly suppress the temperature rise under HPM injection. Furthermore, as shown in Figs. 5(d)–5(f), compared to the original devices, the addition of shallow donor traps causes the device to reach the melting point of GaAs sooner. The temperature in the original device exceeds 1511 K within the third HPM injection cycle. However, when a deep donor trap with a concentration of 1×10^{18} cm^{-3} and an energy level of $E_{\mathrm{c}} - 0.6$ eV is added to the substrate, the highest temperature within the device remains below 1000 K at the failure moment of the original device, showing a reduction of 762 K.

Figures 5(g)–5(l) show the temperature rise curves within the device after introducing acceptor traps in the different layers. It can be observed that the introduction of acceptor traps effectively reduces the temperature rise rate under HPM exposure. Specifically, when an acceptor trap with an energy level of $E_{\mathrm{v}} + 0.6$ eV and a concentration of 1×10^{18} cm^{-3} is added to the substrate, the highest temperature in the device remains below 500 K at the moment the temperature of the original device exceeds 1511 K, resulting in a reduction of 1233 K. Similarly, the introduction of acceptor traps with an energy level of $E_{\mathrm{v}} + 0.6$ eV and a concentration of 1×10^{18} cm^{-3} in the isolation and barrier layers reduces the temperature in the device by 658 K and 730 K, respectively, compared to the original device.

When introducing traps to mitigate the HPM damage effect, the impact on the operating characteristics of the device needs to be considered. Figure 6 shows the variation in the saturated output current and peak temperature of the device during the third cycle of HPM injection.

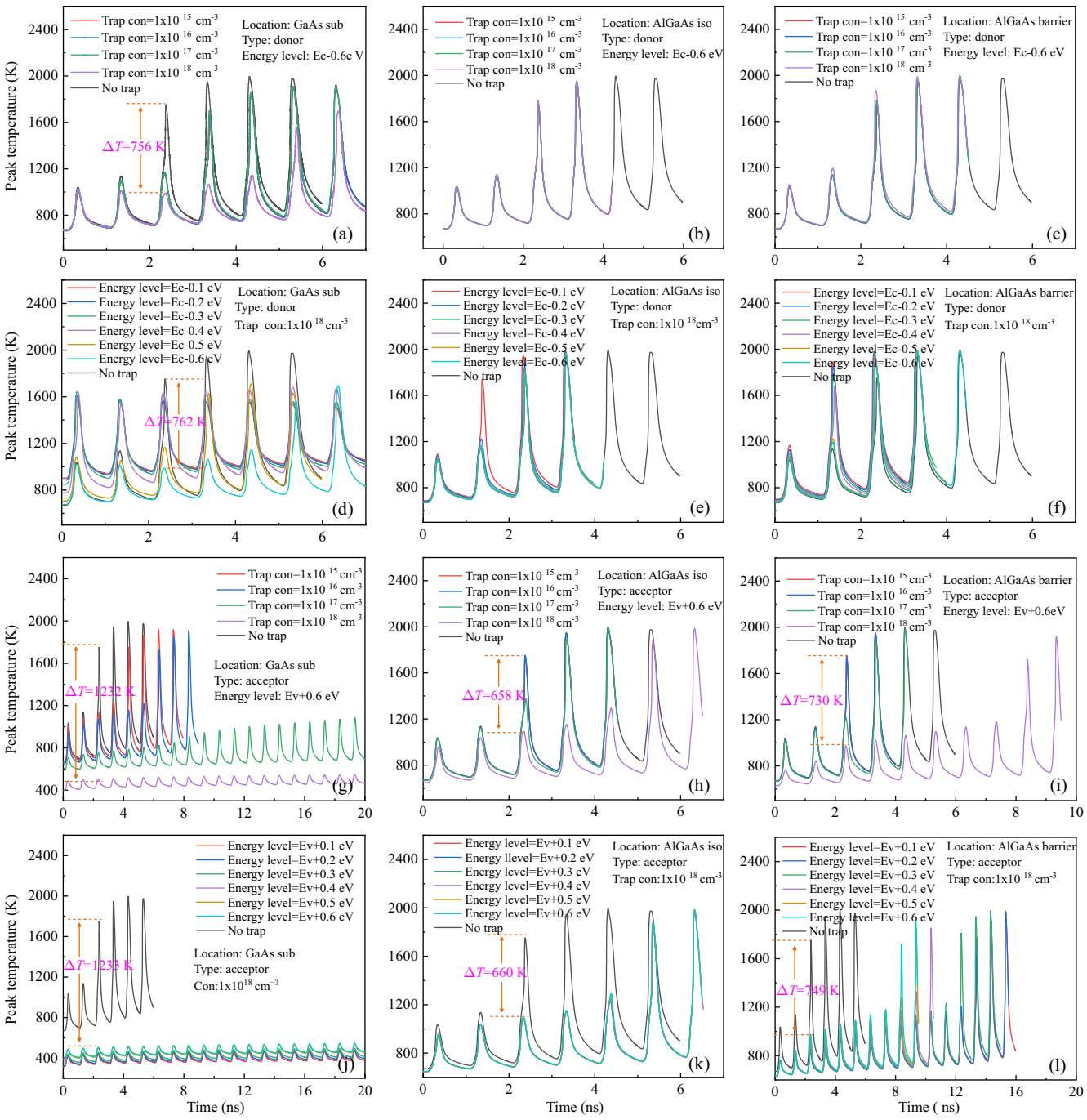

Fig. 5. The temperature rise curves of GaAs pHEMT devices with trapped locations, energy levels, and concentrations under HPM exposure (with a 1-GHz, 10-V sine wave pulse signal injected at the gate port).

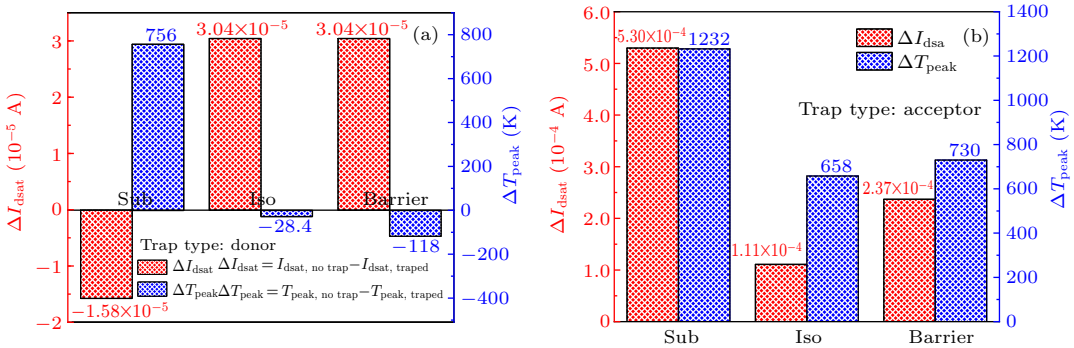

Fig. 6. Statistical data on the effects of traps with a concentration of 1×10^{18} cm^{-3}: (a) donor traps with an energy level of $E_c - 0.6$ eV and (b) acceptor traps with an energy level of $E_v + 0.6$ eV, on the output current and temperature (at 2.5 ns) under HPM exposure.

As shown in Fig. 6(a), adding donor traps with a concentration of 1×10^{18} cm^{-3} and an energy level of $E_c - 0.6$ eV in the substrate effectively reduces the temperature rise, with minimal impact on the output current compared to donor trapping in other layers. The saturated output current increases by only 1.58×10^{-5} A (the saturated output current of the original device is 8.8×10^{-4} A). Figure 6(b) shows that although introducing acceptor traps with a concentration of 1×10^{18} cm^{-3} and an energy level of $E_v + 0.6$ eV in the substrate effectively reduces the temperature rise rate, it significantly affects the operating characteristics of the device, resulting in a decrease of 5.30×10^{-4} A in the saturated output current. Conversely, introducing the same concentration and energy level of acceptor traps in the isolation layer reduces the output current decrease to 1.1×10^{-4} A while effectively lowering the temperature by 658 K.

Additionally, as shown in Fig. 7, the effects of two doping schemes on other characteristics of GaAs pHEMT devices were investigated, including donor traps with a concentration of 1×10^{18} cm^{-3} and energy level $E_c - 0.6$ eV in the substrate, and acceptor traps with a concentration of 1×10^{18} cm^{-3} and energy level $E_v + 0.6$ eV in the isolation layer. It can be observed that the two doping schemes have minimal impact on important device parameters such as threshold voltage, transconductance, cutoff frequency, and gain when compared to the original undoped trap-free device.

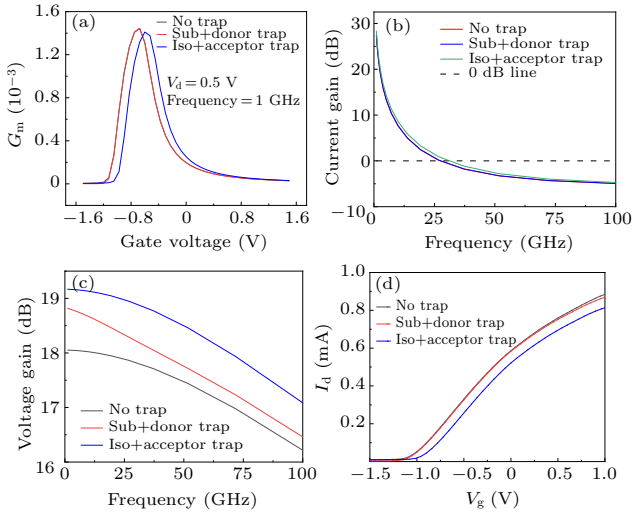

Fig. 7. Device characteristics under different trap doping conditions: (a) transconductance, (b) cutoff frequency, (c) gain, (d) transfer characteristic curve.

3.3. Physical mechanism that trapping improve the HPM resistance of HEMT

Figures 8(a) and 8(b) show the electric field intensity and electron density distribution for these different trap doping devices under HPM (frequency and amplitude are 1 GHz and 10 V respectively) injection from gate. The maximum electric field and electron density for all three devices occur beneath the gate near the source. According to Eq. (7), the electric field intensity and electron density together determine the heat generation, which explains why the temperature at the location near the source beneath the gate reaches the melting point of the material first. Additionally, it is observed that the devices with added traps have significantly lower electric field intensity and electron density at this location compared to the original device, reducing the heat generation power under HPM exposure.

Figure 8(c) shows the electric field intensity distribution at the position near the source beneath the gate, as marked in Fig. 8(a). It can be seen that after trapping, the electric field intensity in the barrier layer beneath the gate decreases, especially in the region close to the bottom of the gate. This is the area where avalanche breakdown, leading to excessive heating, occurs under HPM exposure. As shown in Fig. 8(d), deep donor traps in the substrate undergo ionization under the HPM voltage pulse injection, forming positive charge centers, while acceptor traps in the isolation layer ionize to form negative charge centers. These ionized deep traps generate charged ions that create an internal electric field opposite to the direction of the external electric field, thereby reducing the electric field intensity in the barrier layer. Therefore, the decrease in electric field intensity near the source beneath the gate due to trap addition can reduce carrier accumulation caused by avalanche breakdown, lowering the heat generation of the device and ensuring its reliability under HPM exposure.

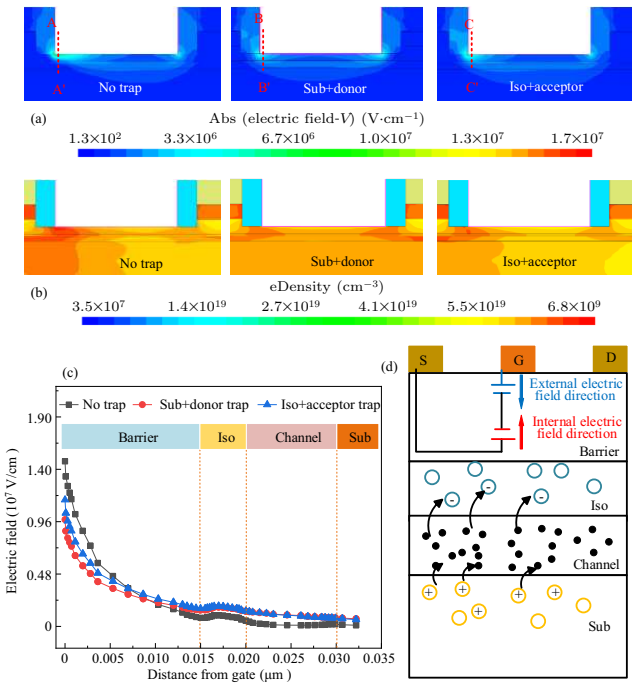

Fig. 8. The internal electric field intensity and electron density distribution at 2.5 ns for trap-free devices, devices with donor traps (concentration of 1×10^{18} cm^{-3} and energy level of $E_c - 0.6$ eV) added to the substrate, and devices with acceptor traps (concentration of 1×10^{18} cm^{-3} and energy level of $E_v + 0.6$ eV) added to the isolation layer.

4. Conclusions

In summary, the effects of introducing donor and acceptor traps into different layers of typical GaAs/InGaAs pHEMTs on their operating characteristics and HPM damage effect are systematically studied. Considering both the impact of traps on device characteristics and the improvement in damage effects under HPM, adding high-concentration, deep-level donor traps (concentration of 1×10^{18} cm^{-3} and energy level of $E_c-0.6$ eV) in the substrate layer, and adding acceptor traps (concentration of 1×10^{18} cm^{-3} and energy level of $E_v+0.6$ eV) in the isolation layer are two effective strategies to suppress the temperature rise rate under HPM exposure, while having minimal impact on the DC operating characteristics of the device. The main reason for the reduced temperature rise rate in the device under HPM exposure is that ionized traps form positive and negative charge centers, which generate an internal electric field opposite to the direction of the external field. This weakens the electric field strength in the barrier layer, leading to reduced carrier accumulation caused by avalanche breakdown during the positive half-cycle of the HPM pulse. The findings of this study provide valuable insights for enhancing the reliability of GaAs pHEMTs under HPM exposure.

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References

[1] Chen C N, Lin Y H, Hung L C, Tang T C, Chao W P, Chen C Y, Chuang P H, Lin G Y, Liao W J, Kuo T Y, Lin K Y, Huang T W, Lin Y C, Lu H C, Tsai T H and Wang H 2021 *IEEE Trans. Microwave Theory Techn.* **69** 980
[2] Lv Z H, Xu Z W, Dang R R, Song C Y and Yu X P 2021 *IEEE Microwave and Wireless Components Letters* **32** 399
[3] Mao Q D, Huang L Y, Xiang Z W and Meng J 2023 *IEEE Transactions on Plasma Science* **51** 3469
[4] Li F X, Chai C C, Wu H, Wang L, Liang Q S, An Q and Yang Y T 2022 *Microelectronics Reliability* **128** 114427
[5] Zhang C B, Wang H G, Zhang J D and Du G X 2015 *IEEE Transactions on Electromagnetic Compatibility* **57** 1132
[6] Wang L, Chai C C, Li F X, Qin Y S and Yang Y T 2022 *Microelectronics Reliability* **136** 114665
[7] Qin Y S, Chai C C, Li F X, Liang Q S, Wu H and Yang Y T 2022 *Micromachines* **13** 106
[8] Yan T, Zhang Y H, Li P and Zhang S 2018 *Microelectronics Reliability* **82** 228
[9] Zhou L, San Z W, Hua Y J, Liang L, Zhang S, Zhao Z G, Zhou H J and Yin W Y 2017 *IEEE Transactions on Electromagnetic Compatibility* **59** 902
[10] Xi X W, Chai C C, Liu Y, Yang Y T, Fan Q Y and Shi C L 2016 *Chin. Phys. B* **25** 048504
[11] Xi X W, Chai C C, Zhao G, Yang Y T, Yu X H and Liu Y 2016 *Chin. Phys. B* **25** 048503
[12] Singh S K, Tripathi A K and Saini G 2020 *Superlattices and Microstructures* **146** 106684
[13] Wang L, Chai C C, Zhao T L, Wei F, Liu W S, Wang Y T, Li Z, Xu L, Li F X and Yang Y T 2023 *IEEE Transactions on Power Electronics* **39** 1492
[14] Li X D, Yuan J H, Wang H Y, Cai Z Q, Shao W H, Chen Y Q, Zheng X F, Zhang J C and Hao Y 2023 *IEEE Transactions on Electron Devices* **70** 5619
[15] Yi S P and Du Z W 2019 *IEEE Transactions on Plasma Science* **47** 4620
[16] Liu Y Q, Chai C C, Wu H, Zhang Y H, Shi C L and Yang Y T 2020 *IEEE Journal of the Electron Devices Society* **8** 731
[17] Yu X H, Chai C C, Liu L, Yang Y T and Xi X W 2015 *Chin. Phys. B* **24** 048502
[18] Yu X H, Ma Z Y, Chai C C, Shi C L and Wang P 2019 *IEEE Transactions on Electromagnetic Compatibility* **62** 101
[19] Su X, Yang L, Zhang M, Zhu Q, Gao W Z, Zhao W, Yu Q, Chang Q Y, Lu H and Shi C Z 2024 *Appl. Phys. Lett.* **125** 102105
[20] Jia F C, Ma X H, Yang L, Hou B, Zhang M, Zhu Q, Wu M, Mi M H, Zhu J J and Liu S Y 2021 *IEEE Transactions on Electron Devices* **68** 6069
[21] Chaudhuri R R, Joshi V, Gupta S D and Shrivastava M 2021 *IEEE Transactions on Electron Devices* **68** 4869
[22] Joshi V, Tiwari P and Shrivastava M 2019 *IEEE Transactions on Electron Devices* **66** 570
[23] Pan S J, Feng S W, Li X, Bai K, Lu X Z, Y Li J, Zhang Y M, Zhou L X and Zhang M 2024 *Appl. Phys. Lett.* **125** 102105
[24] Yang S, Huang S, Wei J, Zheng Z Y, Wang Y R, He J B and Chen K J 2020 *IEEE Electron Dev. Lett.* **41** 685
[25] Synopsys 2019 *Sentaurus Technology Template*
[26] Su J L, Nishi Y and Moll J L 1971 *Solid-State Electron.* **14** 262
[27] Huth F 1970 *Phys. Stat. Sol. (a)* **1** K37
[28] Sze S M and Ng K K 2007 *Physics of Semiconductor Devices*, 3rd ed. (Hoboken, NJ: John Wiley & Sons)
[29] Stievenard D, Bourgoin J C and Lannoo M 1984 *J. Appl. Phys.* **55** 1477
[30] Narasimhan K L and Arora B M 1985 *Solid State Commun.* **55** 615