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A 2-kV high-voltage GaN HEMT on sapphire substrate with floating field plate technique and bonding pad over active region

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A 2-kV high-voltage D-mode GaN high electron mobility transistor (HEMT) with floating field plate (FFP) technique and bonding pad over active region is demonstrated in this work. Compared with the conventional GaN HEMTs that utilize gate field plate (GFP) and source field plate (SFP) technologies, the breakdown voltage (BV) of the proposed device is enhanced by integrating GFP, SFP, and FFP together. This combination significantly reduces the electric field in the oxide layer, thereby reducing the breakdown risk of long-term operation. In order to save the chip area, the source and drain bonding pads of the conventional device and the proposed device are prepared on the upper surface of the active region. Meanwhile, the static on resistance ($R_{DS,on}$) of the two devices are both $\sim$ 150 mΩ. At the same gate–drain spacing (L_{GD}) of 30.5 μm, the conventional device features a specific on-resistance ($R_{on,sp}$) of 10 mΩ· cm^2 and a BV close to 1600 V. While the $R_{on,sp}$ of the proposed device based on FFP technology is 10.5 mΩ·cm^2, and the BV is over 2000 V. Under the premise that the $R_{on,sp}$ is roughly the same, the BV of the proposed device is 33 % higher than the conventional one. The proposed FFP GaN HEMT greatly reduces the oxide electric field, obtains excellent breakdown voltage characteristics, and has great potential for application in the field of high-voltage GaN HEMTs.

Keywords: GaN HEMT, breakdown voltage, sapphire, floating field plate

PACS: 85.30.De, 85.30.Tv

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1. Introduction

GaN high-electron-mobility transistors (HEMTs) have broad prospects in the field of power devices,[1] because of their high-current operation capability, low on-resistance, and high electron saturation velocity.[2–5] GaN HEMTs are currently used in scenarios below 650 V, but their application in high-voltage scenarios such as automotive electronics and radar communications is limited. Therefore, the development of high-voltage GaN HEMTs is imminent.

The introduction of the field plate structure is the simplest and most commonly used method to improve the breakdown voltage (BV) of GaN HEMT devices. In Ref. [6], the authors proposed a self-aligned slant-field-plate technology to increase the BV to more than 1 kV. A vertical field plate is proposed in GaN HEMT to increase BV, which extends the vertical drain field plate to the GaN buffer layer.[7] Based on the gate field plate and two-stage source field plate technology, a D-mode GaN-on-sapphire with gate–drain spacing (L_{GD}) of 30-μm highlighting a high BV over 1700 V is fabricated in Ref. [8]. The metal field plate effectively increases the BV of the device, but the common disadvantage of the stepped or multilayer field plate is that it will increase the complexity of the process and increase the manufacturing cost.

The floating field plate (FFP) is different from the traditional metal field plates. It does not directly connect the electrode but adds a floating metal block above the drift region, and there is an interlayer dielectric between the metal block and the semiconductor material, which is in a floating state.[9,10] The modulation of the electric field near the gate by the FFP and the source metal field plate enables the device to effectively reduce the peak electric field near the gate in the blocking state, resulting in a more uniform distribution of the electric field near the channel layer. At the same time, the modulation effect of the two suppresses the gate and drain leakage current in the off state, thus greatly improving the breakdown voltage. On the other hand, for lateral GaN HEMTs, the bonding pad over active region still poses a challenge, and the risk of leakage and breakdown increases with higher voltage ($>$ 1200 V), leading to greater challenges.

In this work, a 2-kV GaN HEMT on the 6-inch (1 inch = 2.54 cm) sapphire substrate using source and gate field plates combined with a single floating field plate is

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demonstrated, and the FFP and the gate field plate are simultaneously formed through the lift-off process during fabrication, simplifying the process preparation. Additionally, the bonding pads of the two devices are both above the active region. In order to ensure the vertical breakdown voltage and reliability of the active region, the SiN passivation layer, with a thickness of 4 μm, was achieved by depositing it in two stages, each with a thickness of 2 μm. Finally, the proposed device with a gate–drain distance (L_{GD}) of 30.5 μm, an $R_{on,sp}$ of 10.5 mΩ·cm^2, and a high blocking voltage exceeding 2000 V was achieved, along with a threshold voltage (V_{th}) of −8 V. In comparison, the conventional devices demonstrated an $R_{on,sp}$ of 10 mΩ·cm^2 and a blocking voltage of close to 1600 V.

2. Device structure and fabrication process

Figures 1(a) and 1(b) show the schematic views of the conventional GaN HEMT and the proposed FFP GaN HEMT, respectively. The L_{GD} of the conventional device and the proposed device is consistent (30.5 μm), and the source field plate (SFP) and the drain field plate (DFP) are 14 μm and 6 μm, respectively. The proposed device introduces an FFP structure, where an SiN insulating dielectric layer separates the FFP from the surface of the AlGaN barrier layer, and the potential of the FFP varies with the variation of drain-to-source voltage. In the blocking state, there is an electric field in the transverse direction between the gate field plate (GFP) and the FFP of the device. With the combination of the gate field plate, the SFP, and the FFP, the metal field plates with different potentials and the SiN dielectric layer form an equivalent flat capacitor, which generates coupling charges at both ends of the metal field plates.[11] The charges at the FFP attract the electric flux lines from the two-dimensional electron gas (2DEG) layer and the GaN channel layer, which alleviates the concentration of the gate electric field and makes the surface electric field of the device more uniform. As shown in Fig. 1(c), the bonding pads are prepared above the active region, which is different from the traditional preparation method of making pads outside the active area,[12,13] which improves the current capacity in the same chip area. Figure 1(d) reveals the photograph of the entire 6-inch GaN HEMT wafer after the completion of all the manufacturing processes.

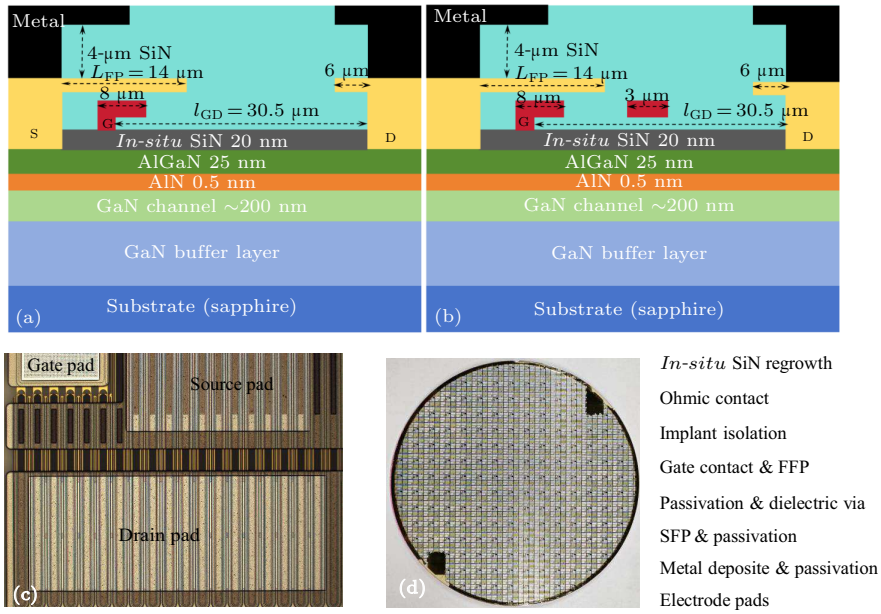


Fig. 1. Schematic diagram of (a) the conventional GaN HEMT, (b) the proposed FFP GaN HEMT with *in-situ* SiN gate dielectric, (c) micrograph of the proposed GaN HEMT fabricated on sapphire substrates, (d) the photograph of the fabricated GaN HEMT wafer.

To save the chip area and comply with advanced packaging techniques, the preparation of bonding pads over the active region of the device offers an effective solution to this issue. In previous works, bonding pads for high-voltage GaN HEMTs were typically positioned outside the active region of the device, thereby eliminating the need for strict control over the quality and thickness of the interlayer dielectric.[14,15] However, achieving a high-voltage GaN HEMT with a bonding pad over the active region is still a challenge, especially in devices with BVs higher than 1200 V, and a significantly high-quality thicker interlayer dielectric is required. Consequently, both the conventional structure and the proposed structure in this paper utilize the sapphire substrate. This choice serves to prevent warping and cracking of the wafers due to the excessive thickness of the interlayer dielectric. Additionally, the sapphire substrate's excellent insulating properties prevent vertical breakdown of the device.

Figures 2(a)–2(f) demonstrate the simplified manufacturing process steps of the FFP GaN HEMT. The 6-inch GaN wafer, consisting of a 2-μm GaN buffer layer, a 200-

nm GaN channel layer, a 0.5-nm AlN spacer, and a 25-nm $Al_{0.25}Ga_{0.75}N$ barrier layer, was grown on a 6-inch sapphire substrate using metal-organic chemical vapor deposition (MOCVD). Then, an about 20-nm *in-situ* SiN is regrown (Fig. 2(a)) as a gate oxide layer to ensure the reliability of the oxide, alleviate the surface state of the device, and improve the threshold voltage stability.[16–19] The manufacture begins with the creation of ohmic contacts, followed by the sequential deposition of Ti/Al/Ni/Au and a rapid thermal annealing at 850 °C in a nitrogen atmosphere for 30 s (Fig. 2(b)). In the next step, through boron (B) ion implantation, the 2DEG is clipped and isolated to form the active region. Then the gate ohmic contact metal of Ni/Au is formed by evaporation, and the gate contact is formed by a lift-off process (Fig. 2(c)). Subsequently, the gate field plate and FFP are formed through etching a 200-nm plasma-enhanced chemical vapor deposition (PECVD) SiN layer, then the source and drain metal is deposited (Fig. 2(d)), so the SFP and DFP are both formed in this step (Fig. 2(e)). Finally, the 4-μm-thick SiN passivation layer is prepared through two times of PECVD with each time 2 μm (Fig. 2(f)).

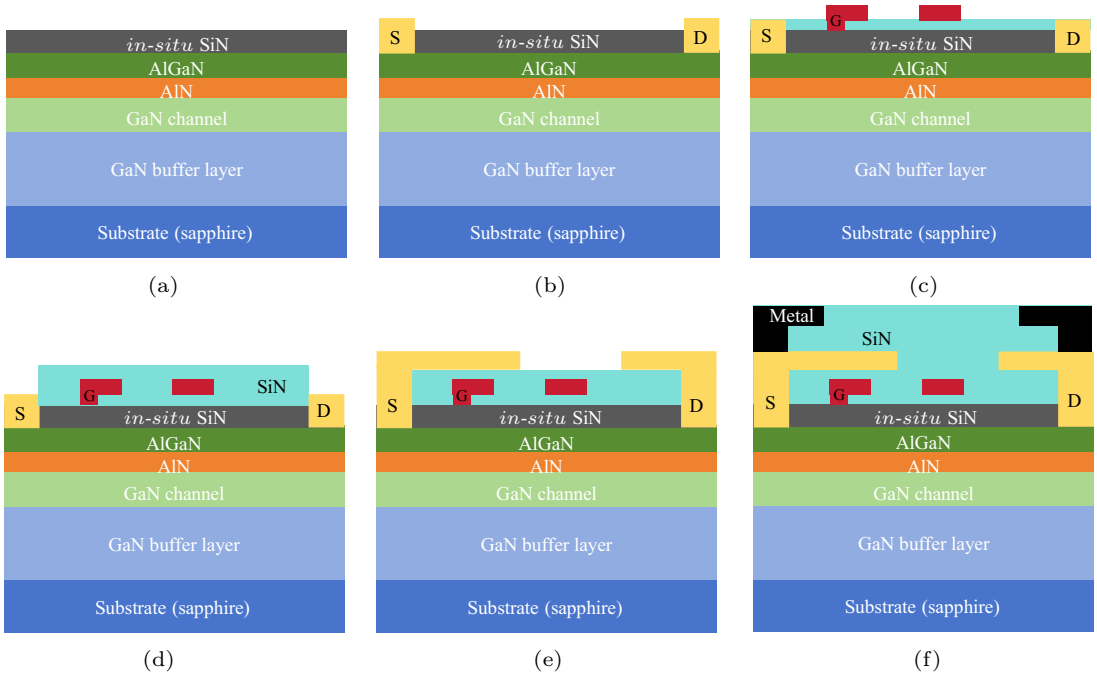


Fig. 2. The fabrication procedures for the proposed device: (a) the formation of multi-epitaxial-layers and *in-situ* SiN regrowth, (b) the formation of ohmic contact and boron ion implantation, (c) the sputtering of gate metal electrode and formation of the FFP, (d) deposition and etching SiN layer to form source and drain windows, (e) preparation of the SFP and DFP, (f) passivation, metal deposition and preparation of bonding pads.

3. Results and discussion

Figure 3(a) shows the transfer characteristic curves of the conventional device and the proposed device. Both devices are D-mode, and the V_{th} of the devices are both about −8 V. At the same time, the gate leakage current of the two devices is very close, and the gate current is only 10^{-3} mA/mm when the device is in the on-state. The transconductance curves of the two devices can be seen in Fig. 3(b). The maximum transconductance of the conventional device is 1310 μS, and the maximum transconductance of the proposed device is 1290 μS. The larger the transconductance is, the stronger the current control of the gate is. Therefore, the *in-situ* SiN layer greatly increases the gate stability, which not only reduces the gate leakage but also enhances the gate control capability.

Figure 4(a) shows the output characteristic curves of the two devices. The output curves are tested under the conditions of $V_{GS} = -3$ V, 0 V, 3 V, respectively. The results reveal that when $V_{DS} = 1$ V, $V_{GS} = 3$ V, the static drain–source on resistance ($R_{DS,on}$) of the conventional device is 150 mΩ, the $R_{DS,on}$ of the proposed device is 158 mΩ; correspondingly, the $R_{on,sp}$ of the conventional device is 10 mΩ·cm^2, and the $R_{on,sp}$ of the proposed device is 10.5 mΩ·cm^2. The $R_{DS,on}$ and $R_{on,sp}$ of the two devices are basically close. Figure 4(b) demonstrates the breakdown characteristic curves of the two devices. Due to the very low leakage current achieved by the manufactured devices, we implement stringent standards and use an I_D of 1 μA as the criterion for assessing device breakdown. At $V_{GS} = -16$ V, the BV of the conventional device is close to 1600 V, and the BV of the proposed device exceeds 2000 V. It can be seen that the introduction of FFP has a great effect on the breakdown voltage characteristics of the device. The forward conduction characteristics of both devices are almost identical, but the BV of the proposed device has been improved by 33%.

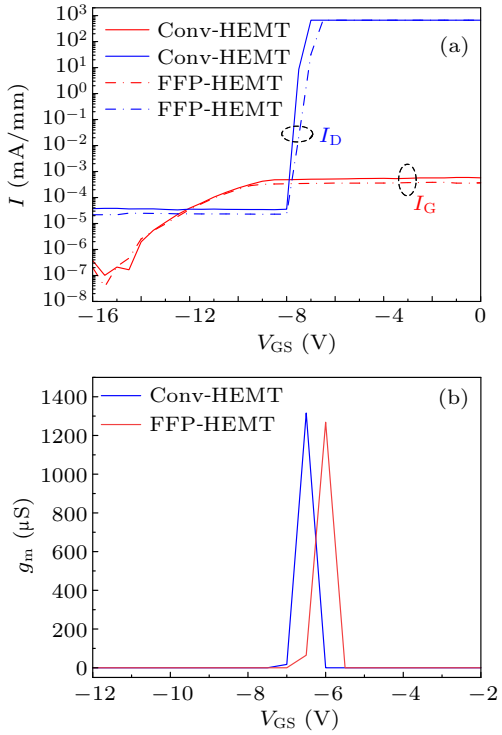


Fig. 3. (a) Transfer characteristic curves of conventional (Conv) GaN HEMT and proposed FFP GaN HEMT, (b) transconductance curves of the two devices.

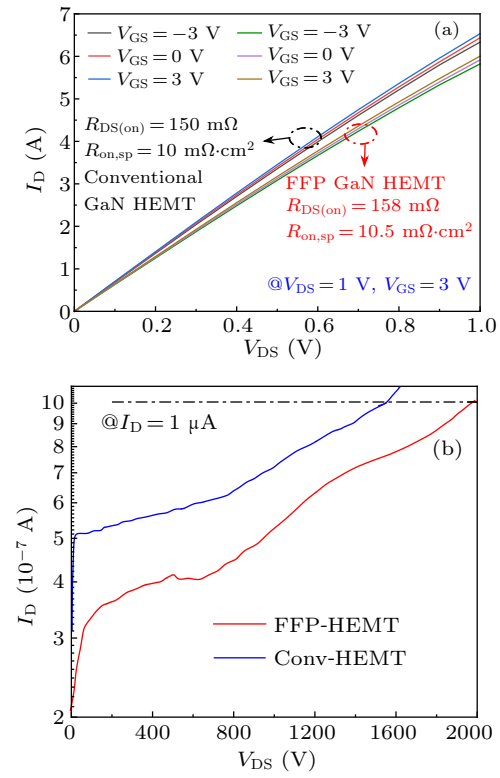


Fig. 4. (a) Output characteristic curves of the conventional HEMT and FFP HEMT, (b) the breakdown characteristic curve of the devices.

Figures 5(a) and 5(b) depict the drain leakage current and the gate leakage current of the proposed FFP GaN HEMT and conventional HEMT, respectively. During the reverse biased state, the V_{DS} from 0 V to 200 V is applied during the gate and drain leakage current testing. As shown in Figs. 5(a) and 5(b), under the condition of $V_{GS} = -16$ V, it can be noted that with the increase of V_{DS}, the I_D and I_G of the proposed FFP GaN HEMT are significantly lower than those of the conventional structure, which indicates that the introduction of floating field plate can greatly reduce leakage current and improve the BV of the device. In fact, when the carrier moves under a high electric field, it will obtain energy from the electric field and accelerate its speed, leading to impact ionization, generating avalanche carriers and increasing the leakage current. When the device is in a higher electric field, the leakage current will rise sharply, and the device will breakdown. Compared with the Conv-HEMT, under the same V_{DS}, the floating field plate introduces an additional electric field, which interacts with the original electric field, not only reducing the peak electric field, but also making the surface electric field more uniform. As a result, the leakage current (I_D and I_G) of the proposed FFP-HEMT is smaller than the conventional one.

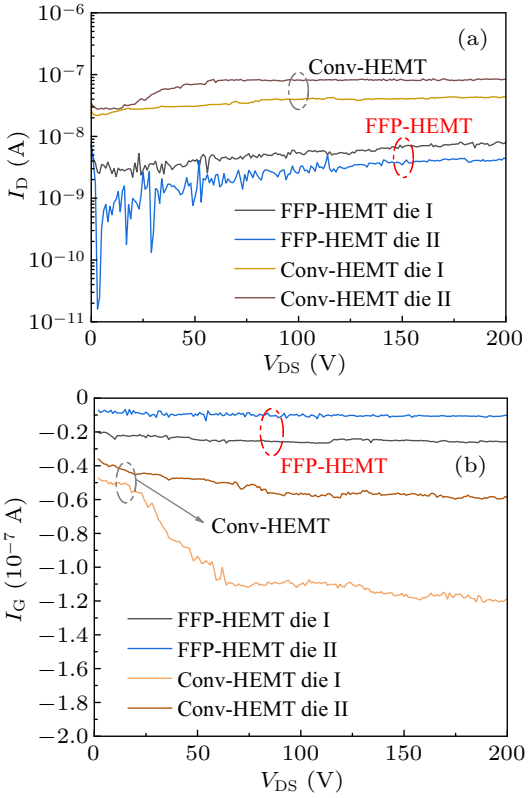


Fig. 5. (a) The drain leakage current (I_D) and (b) the gate leakage current (I_G) of the FFP-HEMT and the Conv-HEMT device in the reverse bias state.

The experimental test results can only represent device characteristics at certain macroscopic levels. To verify the electric field modulation effect of the FFP on the channel layer, TCAD device simulation was conducted. During the epitaxial growth process, the GaN buffer layer will exhibit a shallow N-type semiconductor. At the same time, to prevent the bulk leakage current in the buffer layer, carbon concentration doping of 1×10^{16} cm^{-3} was considered. Therefore, in the simulation, the unintentional doping concentration of the buffer layer is 1×10^{15} cm^{-3}, and the C-doping concentration is 1×10^{16} cm^{-3}.[20,21]

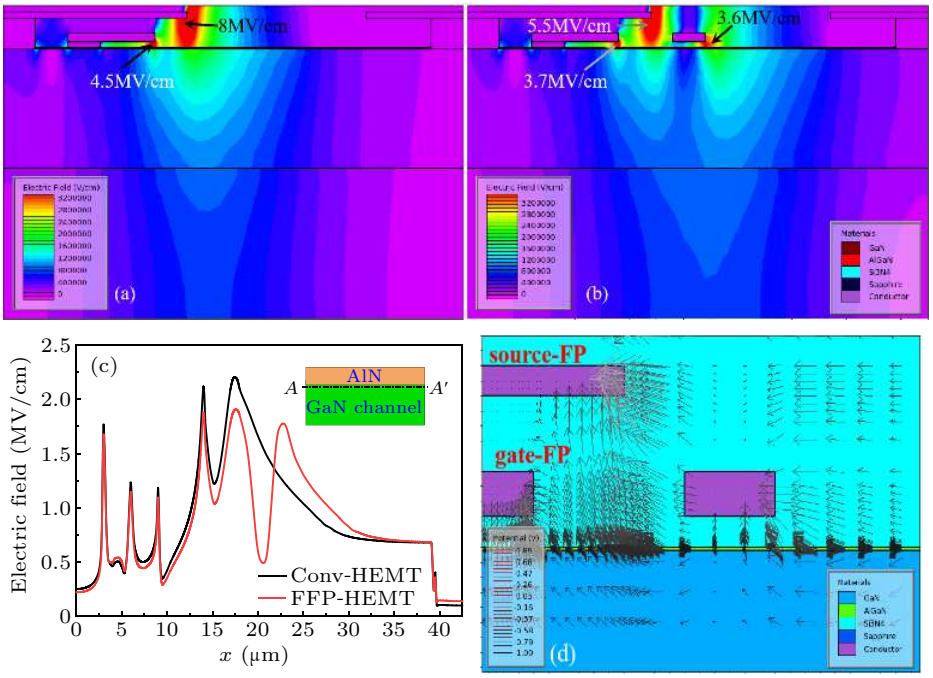


Fig. 6. (a) Electric field distribution of the conventional GaN HEMT at $V_{DS} = 1600$ V, $V_{GS} = -16$ V; (b) the proposed FFP GaN HEMT at $V_{DS} = 2000$ V, $V_{GS} = -16$ V; (c) the electric field distribution at the interface of GaN channnel layer at $V_{DS} = 1600$ V along the dotted line AA'; (d) the electric field vector diagram of FFP GaN HEMT.

The electric field distributions of the conventional device and the proposed device at their respective BV are plotted in Figs. 6(a) and 6(b), respectively. It is evident that the introduction of the floating field plate significantly reduces the electric field in the SiN passivation layer. Specifically, the peak electric field decreases from 8 MV/cm to 5.5 MV/cm, and the peak electric field at the gate field plate's edge is also reduced. The introduction of the floating field plate is beneficial for the improvement of BV and stability of the device. Figure 6(c) illustrates the electric field distribution along the surface of the GaN channel layer for both devices. The proposed device mitigates the electric field peaks caused by the gate and source field plates. Consequently, the maximum electric field throughout the semiconductor region is 2 MV/cm, which is well below the critical breakdown electric field of GaN material. In the simulation, the peak electric field in the GaN material is close to the critical electric field of GaN (3.4 MV/cm), indicating that the device has broken down. Therefore, it can be observed that the BV of the conventional device is about 1600 V, while the BV of the proposed device is higher than 2000 V. This conclusion is consistent with the experimental test results presented in Fig. 4(b). Figure 6(d) presents the electric field vector diagram, showing how the floating field plate, gate field plate, and source field plate form a capacitive structure. Under capacitive coupling, the edge of the floating field plate generates coupling charges, which attract the electric field lines near the gate field plate. This alleviates the surface electric field and the electric field at the gate corner, thereby enhancing the BV and improving the robustness of the passivation layer.

For the stability validation of the proposed FFP GaN HEMT, various bias voltages were applied to the floating field plate in the simulations. When the V_{DS} of 1200 V was applied, Fig. 7(a) presents the three-dimensional electric field distribution of the proposed device at a potential of -300 V, while Fig. 7(b) demonstrates the electric field distribution of the proposed device at a potential of $+300$ V. Under different capacitive coupling potentials of the floating field plate, the channel layer electric field remains relatively low, while the peak electric field consistently appears in the oxide layer. The maximum electric field in the oxide layer is only 5 MV/cm in Fig. 7(a), which is significantly lower than the breakdown electric field of the oxide layer. Moreover, under normal operating conditions, the potential of the FFP is positive, which results in a lower electric field in the oxide layer, as shown in Fig. 7(b). This strongly suggests that the device exhibits excellent voltage sustaining capability. Figure 7(c) illustrates the electric field distribution within the channel layer along the dotted line AA' of the FFP GaN HEMT under different bias conditions at $V_{DS} = 1200$ V. At the normal capacitive coupling floating potential, the electric field intensity of the channel layer is the lowest. However, under conditions of normal floating potential of -300 V and $+300$ V, the channel layer electric field increases, yet there is no abnormally high electric field present in the channel layer on either the left or right side of the FFP. Moreover, under actual blocking state, the potential of the FFP varies with V_{DS}, and it is always positive. As a result, we present the simulation result of the potential

at the FFP under different V_{DS} of the proposed GaN HEMT in Fig. 7(d). The results clearly demonstrate that, as V_{DS} is increased from 0 V to 2 kV, the potential at the FFP rises from 0 V to approximately +800 V. Finally, it can be seen that the introduction of FFP is effective and stable for improving the breakdown voltage of the device.

It is well known that the capacitive characteristics have a direct impact on the dynamic behavior of the devices; therefore, a simulation study was conducted on the capacitances of both devices to roughly evaluate the dynamic performance of the devices. For power devices, the gate-to-drain capacitance (C_{GD}) is an important factor that affects the dynamic characteristics of the device, influencing its switching speed, switching losses, and stability. Figure 8(a) shows the

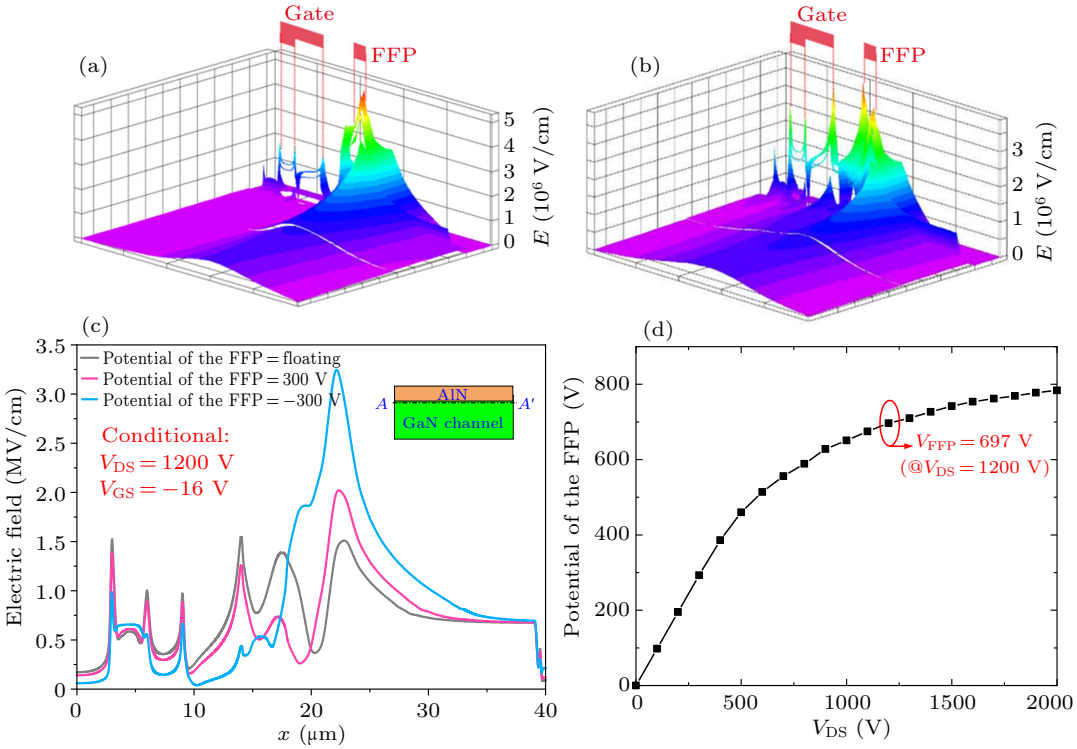


Fig. 7. Three-dimensional electric field distribution of the proposed device (a) at floating potential −300 V and (b) at floating potential +300 V (V_{DS} = 1200 V), (c) the electric field distribution within the channel layer along the dotted line AA' of the FFP GaN HEMT under different FFP bias conditions (V_{DS} = 1200 V), (d) the potential of FFP under different V_{DS} of the proposed GaN HEMT.

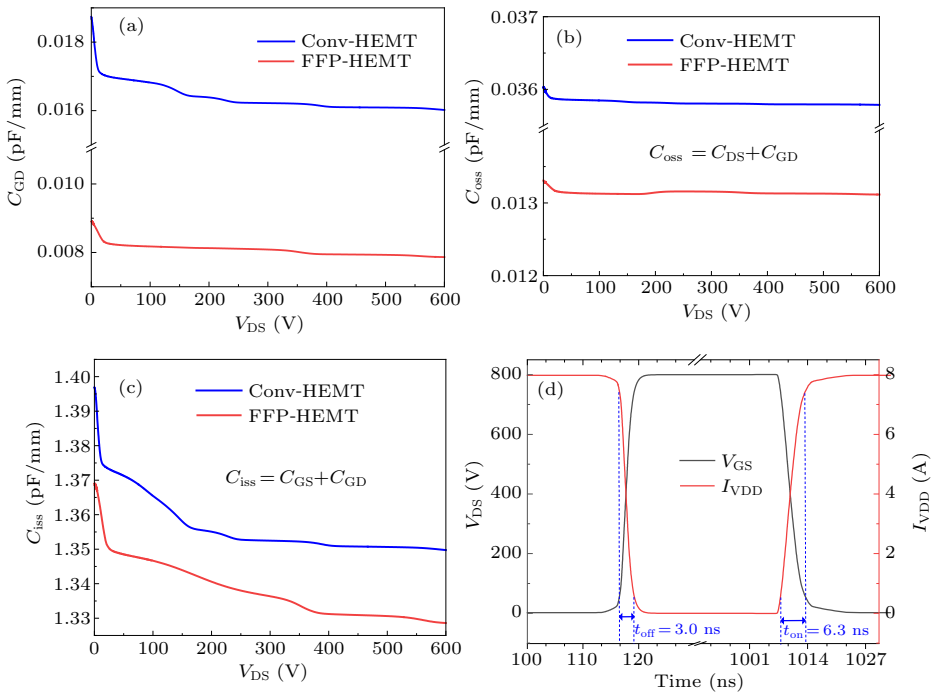


Fig. 8. (a) Gate-to-drain capacitance of the Conv-HEMT and the FFP-HEMT, (b) the output capacitance of the two devices, (c) the input capacitance of the two devices, (d) the turn-on and turn-off processes of FFP GaN HEMT.

comparison of C_{GD} between two types of devices, with the C_{GD} of the FFP being smaller than that of the conventional device. The smaller C_{GD} of the proposed FFP GaN HEMT means that under high-frequency signals, the charging and discharging time of the capacitance is shorter, reducing signal attenuation and distortion. This implies that compared to conventional devices, the proposed FFP GaN HEMT device performs more outstandingly in high-frequency applications. Figures 8(b) and 8(c) show the output capacitances (C_{oss}) and input capacitances (C_{iss}) of the two devices, respectively. The input and output capacitances of the proposed FFP GaN HEMT are both smaller than those of the conventional device. This may be due to the introduction of the floating field plate, which increases the new capacitance coupling effect and shields a part of the gate-to-drain capacitance. The dynamic characteristics of the proposed device have been characterized, and Fig. 8(d) shows the simulation results. As can be seen from the figure, the proposed device has excellent switching characteristics, with a turn-on time (t_{on}) of 6.4 ns and a turn-off time (t_{off}) of 3.0 ns, respectively.

Figure 9 illustrates the relationship between the BV and $R_{on,sp}$ for various previous GaN HEMTs. It is evident that the proposed FFP-HEMT exhibits significant advantages in terms of breakdown voltage.[22–28]

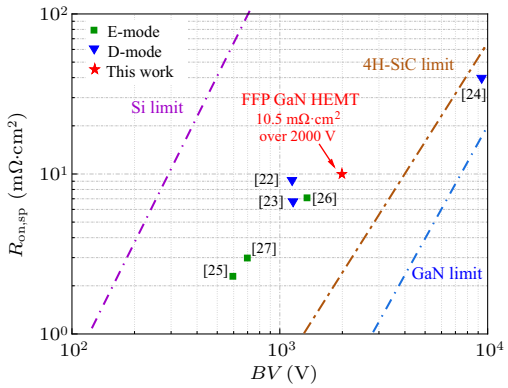


Fig. 9. The relationship between BV and $R_{on,sp}$ of different GaN HEMT devices.

4. Conclusion

In this work, a novel FFP GaN HEMT is proposed and fabricated, achieving a breakdown voltage level exceeding 2000 V due to the combined effects of the FFP and the gate and source field plates. The utilization of *in-situ* grown SiN as the gate oxide layer, along with the introduction of the FFP, optimizes the electric field distribution within the oxide layer and significantly enhances the stability of the device. Additionally, for ultra-high voltage lateral devices, the bonding pads over the active region are still a challenge, and the bonding pads of our proposed GaN FFP HEMT device are successfully positioned directly above the active region, leading to a reduction in chip area and an improvement in current capability. This innovation offers promising commercial potential and is well-suited for high-voltage and high-current applications.

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