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High-quality GaAs/InSb core–shell nanowires grown by molecular-beam epitaxy

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High-quality GaAs/InSb core–shell nanowires have garnered significant research interest owing to the exceptional properties of InSb, including its high electron mobility, strong spin–orbit coupling, and large g-factor, which are pivotal for advanced electronics and quantum technologies. Concurrently, GaAs/InSb core–shell nanowires have been extensively investigated due to their potential in realizing topological insulators and enabling dissipationless edge state transport, characteristics analogous to those sought in InAs/GaSb systems. However, the substantial lattice mismatch ($\sim 14.6\%$) between GaAs and InSb poses considerable challenges in achieving high-quality heteroepitaxial shells. Detailed investigations into the growth, microstructure, and strain distribution within such systems remain limited. Here, we demonstrate the successful growth of high-quality GaAs/InSb core–shell nanowires via molecular-beam epitaxy, utilizing self-catalyzed pure zinc blende GaAs nanowire cores. Through systematic optimization, we identified that an InSb shell growth temperature of 390 °C and an Sb/In beam equivalent pressure ratio of 4.36 are crucial for obtaining smooth, continuous shells with uniform thickness. Advanced transmission electron microscopy analysis confirmed the epitaxial zinc-blende structures of both the core and shell, revealing a dislocation density of approximately 50 μm^{-1} in the InSb shell, notwithstanding the lattice mismatch. Cross-sectional strain mapping, conducted via geometric phase analysis, unveiled a $\sim 15\%$ compressive strain at the GaAs/InSb interface, along with complex residual strain within the shell, attributed to the hexagonal nanowire geometry. Field-effect transistors fabricated with back-gated configurations exhibited n-type conduction, with a room-temperature carrier mobility of 50 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and Ohmic behavior. Our work provides useful insights for the growth and optimization of other highly mismatched core–shell nanowires, thereby facilitating their integration into complex device architectures.

Keywords: GaAs/InSb, nanowires, molecular-beam epitaxy, microstructure and strain analysis, electrical properties

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1. Introduction

The exploration of narrow bandgap III–V semiconductors, particularly InSb, has become increasingly important due to their exceptional properties, including high electron mobility, significant spin–orbit coupling, and large g-factor.[1–7] These attributes make InSb an attractive candidate for various advanced electronic and quantum applications, such as high-speed transistors, spintronic devices, and topological quantum computing, where the creation and manipulation of Majorana bound states are of particular interest.[8–17] One promising strategy to leverage the unique properties of InSb is through the fabrication of core–shell nanowires, where an InSb shell is epitaxially grown around a core material with different electronic and structural characteristics. GaAs, a well-studied III–V semiconductor with mature fabrication techniques, serves as an ideal core material. The GaAs/InSb core–shell nanowire system not only combines the high mobility and strong spin–orbit interaction of InSb with the stability and processability of GaAs but also introduces the possibility of engineering novel band alignments and strain-induced effects due to the significant lattice mismatch ($\sim 14.6\%$) between the two materials.[18,19] Additionally, the unique band structure and strain-induced modifications in these nanowires could enable the realization of topological insulators,[20,21] paving the way for dissipationless edge state transport and novel quantum computing architectures. Despite these promising prospects, research on GaAs/InSb core–shell nanowires remains limited. To date, only one research group has reported on the growth and characterization of these heterostructures.[21,22] This scarcity of studies underscores the urgent need for further investigations into the growth mechanisms, microstructural evolution, and electronic transport behaviors of GaAs/InSb core–shell nanowires. In particular, a detailed understanding of the microstructure and strain distribution within these nanowires is crucial for future optimizing their performance

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in device applications. While theoretical models and preliminary experiments have suggested the presence of strain and its potential effects, a systematic microstructural and strain analysis of the cross-sections of GaAs/InSb core–shell nanowires has yet to be conducted.

In this study, we aim to fill these knowledge gaps by conducting an investigation of the growth, microstructure, and strain distribution in high-quality GaAs/InSb core–shell nanowires grown via molecular beam epitaxy (MBE). We have explored the optimal growth conditions to achieve smooth and continuous InSb shells on pure zinc-blende GaAs cores and employed advanced transmission electron microscopy (TEM) techniques to analyze the resulting microstructures. Furthermore, we have performed a detailed strain analysis on the cross-sections of the nanowires to elucidate the strain relaxation processes and their implications for device performance. By providing a deeper understanding of these fundamental aspects, our research will lay the foundation for the development of high-performance GaAs/InSb core–shell nanowire-based devices for future electronic and quantum technologies.

2. Experiments

2.1. MBE growth of the GaAs nanowires and GaAs/InSb core–shell nanowires

All the GaAs nanowires and GaAs/InSb core–shell nanowires were grown in a solid source MBE system (VG V80H), using commercial p-type Si (111) wafers as substrates. These Si substrates were pretreated by chemical etching before loading into the MBE chamber.[23–26] First, the Si substrates were dipped into an HF solution (5%) for about 30 s to remove the native oxidized layer completely. Then, the substrate was coated with a new oxidized layer by dipping the substrate into the H_2SO_4 (98%) and H_2O_2 (30%) (volume ratio = 4 : 1) solution for about 20 s. For the growth of GaAs/InSb core–shell nanowires, GaAs nanowire cores were grown directly on Si substrates by a self-catalyzed growth manner. The GaAs cores were grown by opening the Ga source shutter for 8 s and then opening the As source shutter. The growth temperature was 650 °C with an As/Ga beam equivalent pressure (BEP) ratio of 4.85 (As and Ga fluxes are 1.6×10^{-6} mbar (1 bar = 10^5 Pa) and 3.3×10^{-7} mbar, respectively). The growth time of GaAs nanowire cores was 30 min. After the growth of GaAs nanowire cores, the Ga shutter was closed, while As flux and the substrate temperature were kept unchanged for 30 s to ensure that the Ga droplet was consumed. Then, the As shutter was closed and the substrate temperature decreased to the InSb shell growth temperature. For InSb shell growth, In flux was fixed at 1.4×10^{-7} mbar, and the Sb/In BEP ratios were decreased from 5.85 to 3.21 by tuning the Sb flux. The growth temperatures of InSb shells were 410 °C to 380 °C. The growth time of InSb shells was 30 min to 90 min.

2.2. Characterizations of the GaAs nanowires and GaAs/InSb core–shell nanowires

The morphology of the GaAs nanowires and GaAs/InSb core–shell nanowires was characterized by scanning electron microscopy (SEM, FEI Nano SEM 650 operated at 15 kV). The crystal structure of the nanowires was investigated by TEM (JEOL 2200 and JEM F200, operated at 200 kV). The element distribution of the nanowires was investigated by the energy dispersive spectrum (EDS) based on the scanning-TEM mode of the JEOL 2200 and JEM F200 TEM systems. For TEM analysis, nanowires were removed from the growth substrate via sonication in ethanol and then drop-cast onto lacey carbon grids. The individual nanowire samples were prepared by dispersing the nanowires in ethanol, using an ultrasonic bath for 10 s, and then placing a drop onto a lacy carbon grid. The cross-sections of the nanowire samples were prepared by first embedding the nanowire samples in epoxy resins and then slicing them with an ultramicrotome (Leica EM UC6). Then the samples were transferred onto the Cu grids for TEM investigations. The strain maps of high-resolution TEM images were determined using Strain++ software.

2.3. Device fabrication of the GaAs/InSb core–shell nanowires

For electrical transport characterizations of GaAs/InSb core–shell nanowires, we fabricated backgated field-effect transistor (FET) devices. Similar to the approach employed in TEM analysis, the GaAs/InSb core–shell nanowires were detached from the growth substrate through sonication in ethanol. To prepare individual nanowire samples, the nanowires were first dispersed in ethanol and subjected to an ultrasonic bath for 10 seconds. Then, a droplet of the dispersion was placed onto a heavily doped p-type Si (111) substrate. In order to expedite the evaporation of ethanol, the Si substrate was placed on a heater and heated at 200 °C for a few seconds. Before depositing metal, a diluted $(NH_4)_2S_x$ solution was used to remove the native oxide layer of nanowires in the contact areas for about 2–7 min. Then, we attached metal electrodes to nanowires using a standard electron beam lithography (EBL) process. A chromium/gold (20 nm/80 nm) film was evaporated and then lifted off in acetone. All electrical measurements of nanowire devices were performed at 6 K and 300 K on a probe station using a semiconductor parameter analyzer.

3. Results and discussion

In this work, we used self-catalyzed high-quality GaAs nanowires as cores for the growth of high-quality InSb shells. Based on our previous work,[26,27] under optimal conditions,

we can grow GaAs nanowires with a pure zinc-blende structure. Epitaxially growing InSb shells on such high-quality GaAs nanowires is expected to prevent the adverse effects of stacking faults and twin defects in the GaAs nanowires on the crystal quality of the InSb shells. Therefore, we initially grew these GaAs nanowires on an Si (111) substrate. To verify the crystal quality of the GaAs nanowires, we conducted detailed microstructural characterizations. Figure 1 presents the typical crystal structure information of the GaAs nanowires. As shown in Fig. 1(a), the GaAs nanowires have a uniform diameter of approximately 50 nm. Selected-area electron diffraction (SAED) and high-resolution TEM images confirm that the GaAs nanowires possess a pure zinc-blende structure without stacking faults or twin defects. It is evident that Ga droplets exist at the top of the GaAs nanowires, providing compelling evidence that these GaAs nanowires grow via a self-catalyzed vapor-liquid-solid mechanism. For GaAs/InSb core–shell nanowires, the Ga droplets on the tops of the GaAs nanowires need to be consumed prior to the growth of the InSb shells.

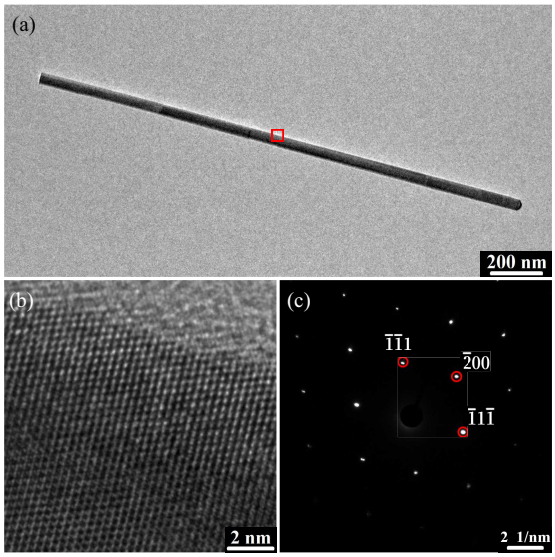


Fig. 1. Crystal structure information of the GaAs nanowires for InSb shell growth. (a) A typical TEM image of the GaAs nanowire. (b) Typical high-resolution TEM image of the GaAs nanowire (recorded from the red box region in panel (a)). (c) Typical SAED pattern of the GaAs nanowire.

To achieve the optimum conditions for growing homogeneous InSb shells on high-quality GaAs nanowire cores, the evolution of nanowire morphology was investigated as a function of the InSb growth temperature. The growth temperatures for InSb shells were systematically decreased from 410 °C to 380 °C while maintaining a constant Sb/In BEP ratio of 5.85 and a fixed growth duration of 60 min. SEM images (25° tilted view and side-view) of these nanowires, presented in Figs. 2(a)–2(p), reveal the surface roughness of the GaAs/InSb core–shell nanowires. The InSb shells grown at 410 °C exhibit significantly rough surfaces, a finding consistent with the observations reported by Rieger *et al.*[21] As the growth temperature is reduced, the quality of the shell surface improves, reaching an optimum at a growth temperature of 390 °C. However, further decreasing the temperature to 380 °C results in a marked increase in surface roughness. A similar phenomenon has been observed in the growth of GaAs/InAs and GaAsSb/InAs core–shell nanowires, although the temperature window for optimal growth in those systems is considerably broader.[25,28] Additionally, it is noted that no shells were formed on the bottom portions of these nanowires. The diameters of nanowires range from approximately 90 nm to 150 nm and the lengths of nanowires are about 1500 nm.

The narrow growth temperature window for InSb shells is likely ascribed to the significant lattice mismatch between GaAs and InSb. Similar to the Stranski–Krastanow growth mode employed for InAs quantum dot materials on GaAs substrates,[29] yet with certain differences, due to this lattice mismatch, InSb shells tend to grow following the Volmer–Weber mode, which is characterized by island formation. According to the formula for nucleus density[30]

$$N_{\mathrm{s}} = AN_0\left(\dot{R}/n\upsilon\right)^p \exp\left(E/k_{\mathrm{B}}T\right),$$

where N_{s} represents the nucleus density, A is a pre-factor, N_0 is the number of available sites for nucleation, $\dot{R}$ is the deposition rate, n is the atomic density of the substrate, υ is the atomic vibration frequency, p is an exponent related to the nucleation mechanism, E is the activation energy for nucleation, k_{B} is the Boltzmann constant, and T is the growth temperature. Based on this formula, the nucleus density N_{s} exhibits a negative correlation with the growth temperature T. This implies that as the substrate temperature decreases, the nucleus density of InSb on the sidewalls of GaAs nanowires increases, which is conducive to the formation of a continuous and smooth InSb shell layer. However, when the substrate temperature is excessively low, insufficient energy is available to facilitate the formation of a smooth InSb shell, resulting in a resurgence of surface roughness.[30]

Subsequently, with the InSb shell growth temperature maintained at 390 °C, we investigated the influence of the Sb/In BEP ratio on the morphology of the nanowire shells. In this series of experiments, the In flux was held constant at 1.4×10^{-7} mbar. The Sb/In BEP ratios were adjusted by varying the Sb flux, ranging from 8.2×10^{-7} mbar to 4.5×10^{-7} mbar, which corresponded to Sb/In BEP ratios from 5.85 to 3.21. All InSb shells were grown for a duration of 60 min. As shown in Figs. 3(a)–3(p), with a decrease in the Sb/In BEP ratio, the GaAs nanowire cores were completely encapsulated by the InSb shells. The surface quality reached its optimum at an Sb/In BEP ratio of 4.36, with an average diameter of approximately 100 nm. However, as the

Sb/In BEP ratio was continuously reduced, the surface roughness deteriorated. Moreover, In droplets formed on the tops of the nanowires due to an excess of In flux. The sensitive influence of the Sb/In BEP ratio on the morphology of the InSb shell can be ascribed to the surfactant effect of Sb.[31–33] Being a relatively heavy atom, Sb has a tendency to accumulate at the surface of the growth layer, thereby exerting a substantial influence on the surface energy. It is crucial to re-emphasize that during the MBE growth of InSb planar epitaxial layers, the Sb/In BEP ratio is approximately 1. Notably, an Sb/In BEP ratio of 20 has been determined as the optimal condition for the MBE growth of InAs/InSb axial heterostructure nanowires.[14,34] For the radial growth of the InSb shell, it is recommended that the Sb/In BEP ratio be set within the range between the values used in the two aforementioned growth modes.

Regarding the phenomenon where no shell forms on the bottom portions of these nanowires, we speculate that it is related to two factors: the supply of In and the growth mode of the InSb shell. As illustrated in Fig. 3, as the Sb/In BEP ratio gradually decreases (in other words, the relative supply of In increases), shells begin to form on the bottom portions of these nanowires. However, when the Sb/In BEP ratio becomes excessively small (that is, the relative supply of In is too abundant), indium droplets start to accumulate at the top of the nanowires. This suggests that the absence of shells on the bottom portions of these nanowires occurs only when the relative supply of In is insufficient, and during the growth process of the InSb shell, the supply of In primarily advances from the top to the bottom of the nanowires. When the supply of In is insufficient, the InSb shells formed by combining with Sb on the top portions have already completely consumed the In atoms. Consequently, there are not enough In atoms on the bottom portions to facilitate InSb formation, leaving the GaAs core exposed. Conversely, when the supply of In is excessive, the surplus In atoms are unable to descend to the sidewalls of the nanowires and instead gather at the top, forming indium droplets. This speculation can also explain the phenomenon depicted in Fig. 2. When the temperature is too high, a complete InSb shell fails to form on the nanowire sidewalls (resulting only in InSb islands on the GaAs sidewalls), and the In atoms are not fully consumed. As a result, some In atoms will sink to lower positions (as shown in Figs. 2(a)–2(d)). When a complete InSb shell is formed, all In atoms are consumed, preventing the formation of InSb shells on the bottom portions of the nanowires.

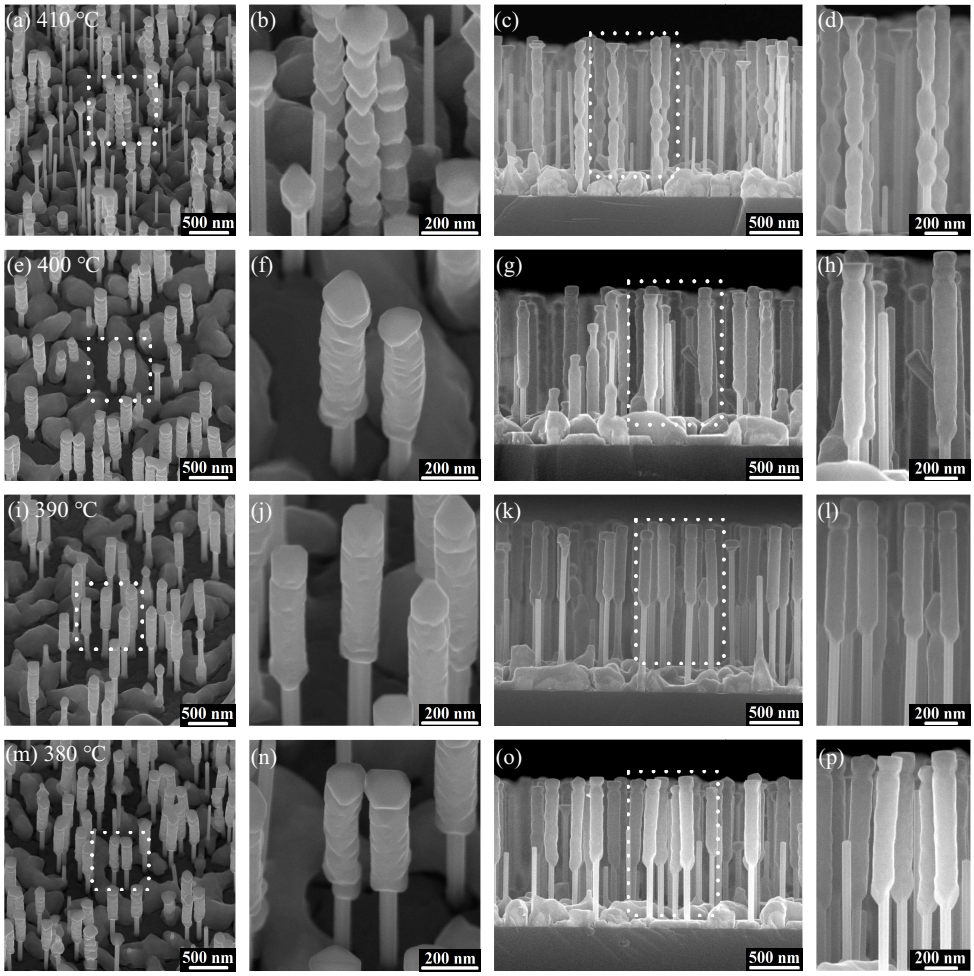


Fig. 2. 25° tilted and side-view SEM images of GaAs/InSb core–shell nanowires grown at different InSb shell temperatures: (a)–(d) 410 °C, (e)–(h) 400 °C, (i)–(l) 390 °C, and (m)–(p) 380 °C.

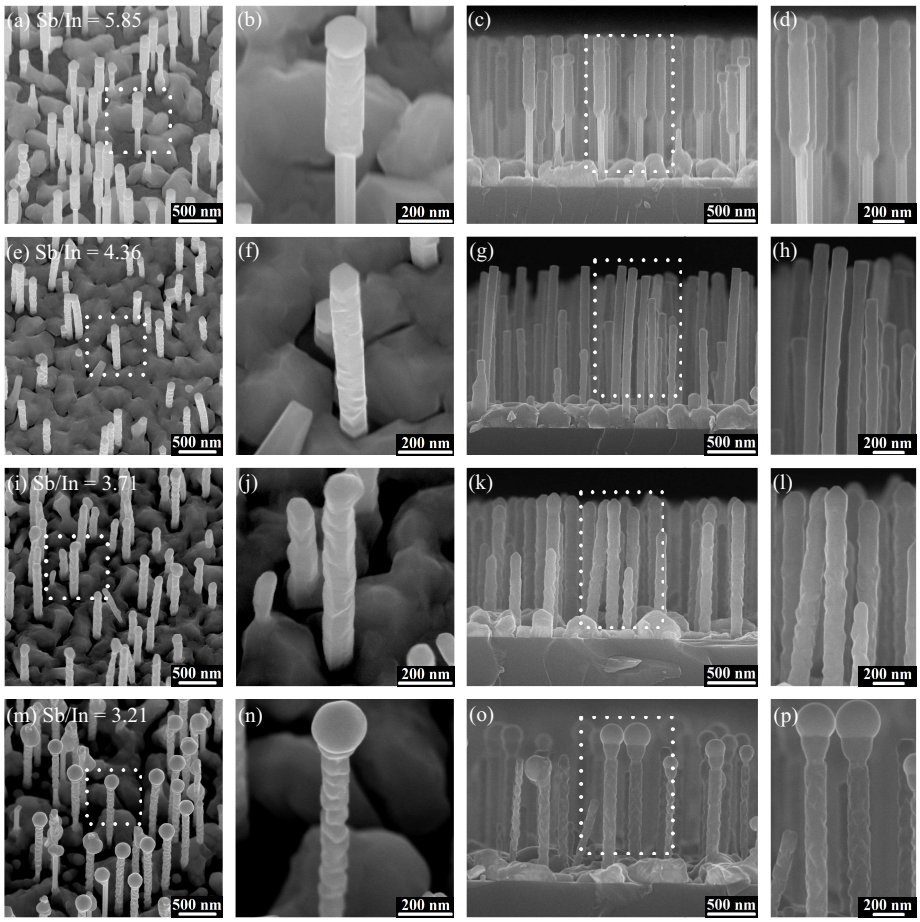


Fig. 3. 25° tilted and side-view SEM images of GaAs/InSb core–shell nanowires grown at different Sb/In BEP ratios: (a)–(d) 5.85, (e)–(h) 4.36, (i)–(l) 3.71, and (m)–(p) 3.21.

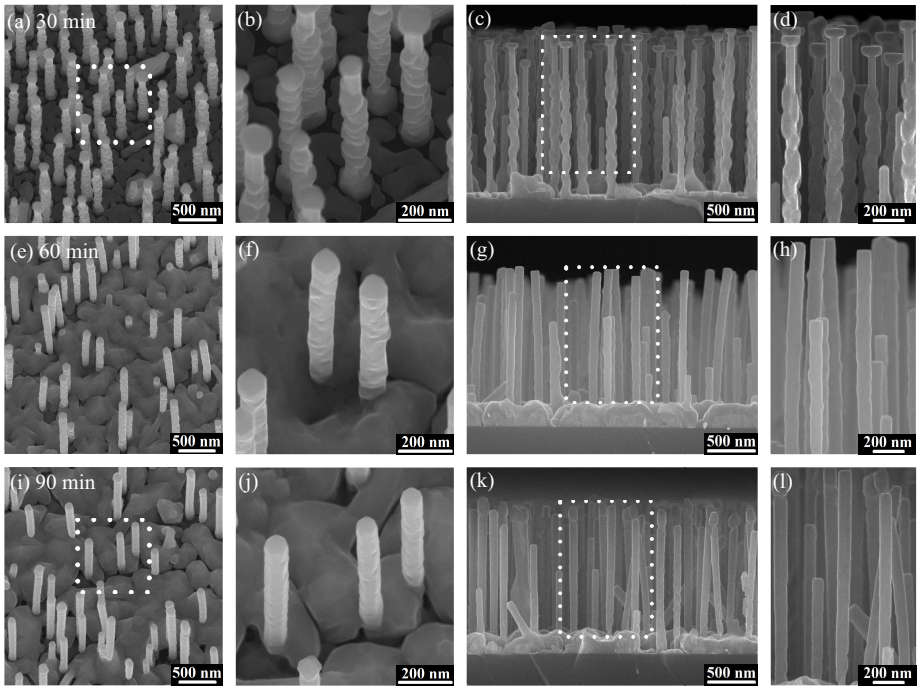


Fig. 4. 25° tilted and side-view SEM images of the GaAs/InSb core–shell nanowires grown with different InSb shell growth time: (a)–(d) 30 min, (e)–(h) 60 min, and (i)–(l) 90 min.

After confirming the optimal parameters for growth temperature and the Sb/In BEP ratio, we proceeded to investigate the influence of growth time on the quality of InSb shells. The experiments were conducted by growing InSb shells for 30 min, 60 min, and 90 min, respectively, under the optimized conditions of a constant growth temperature (390 °C) and an

Sb/In BEP ratio of 4.36. As illustrated in Figs. 4(a)–4(l), with the increase in growth time, the surface of the InSb shell transitioned from rough to smoother, while the shell thickness remained unchanged. Based on the previous images (Figs. 2(a)–2(d)) and the work conducted by Rieger *et al.*, we reaffirmed that InSb shells initially tend to follow the Volmer–Weber growth mode, characterized by island formation, and subsequently develop into full shells with uniform thickness.[21]

To confirm the crystal structure of the GaAs/InSb core–shell nanowires, measurements were conducted using TEM. Figures 5(a)–5(e) display TEM images of a GaAs/InSb core–shell nanowire grown at 390 °C with an Sb/In flux ratio of 4.36 over a duration of 60 min. As illustrated in Fig. 5(a), a low-resolution TEM image of the nanowire reveals slight surface roughness. The colored rectangles indicate the regions where high-resolution TEM images and SAED patterns were recorded. Figure 5(b) presents the SAED pattern corresponding to the red-highlighted region in Fig. 5(a). Two types of nested lattice planes are observed, providing strong evidence for the formation of a core–shell structure. Both the GaAs core and InSb shell exhibit a zinc-blende crystal structure. The majority of the InSb shell demonstrates a high-quality zinc-blende crystal structure, as shown in Fig. 5(c). However, some parts of the shell contain unavoidable twin boundaries and dislocations, as depicted in Figs. 5(d) and 5(e), respectively, due to the significant lattice mismatch between GaAs and InSb. The dislocation density in the InSb shell is approximately 50 dislocations per micrometer (50/μm) according to detailed high-resolution TEM analysis.

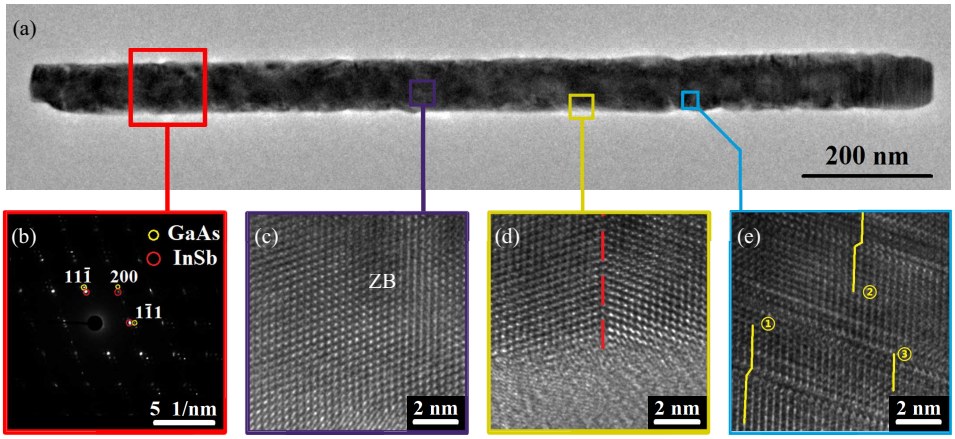


Fig. 5. Crystal structure information of GaAs/InSb core–shell nanowires. (a) Typical low-resolution TEM image of a GaAs/InSb core–shell nanowire grown with an Sb/In flux ratio of 4.36. (b) SAED pattern of the GaAs/InSb core–shell nanowire. (c)–(e) High-resolution TEM images of the GaAs/InSb core–shell nanowire taken from different regions of the nanowire. The red dotted line in panel (d) is a twin boundary between two zinc-blende crystals. Yellow lines in panel (e) mark Shockley partial dislocation (①), Frank partial dislocation (②) and perfect dislocation (③) in the InSb shell.

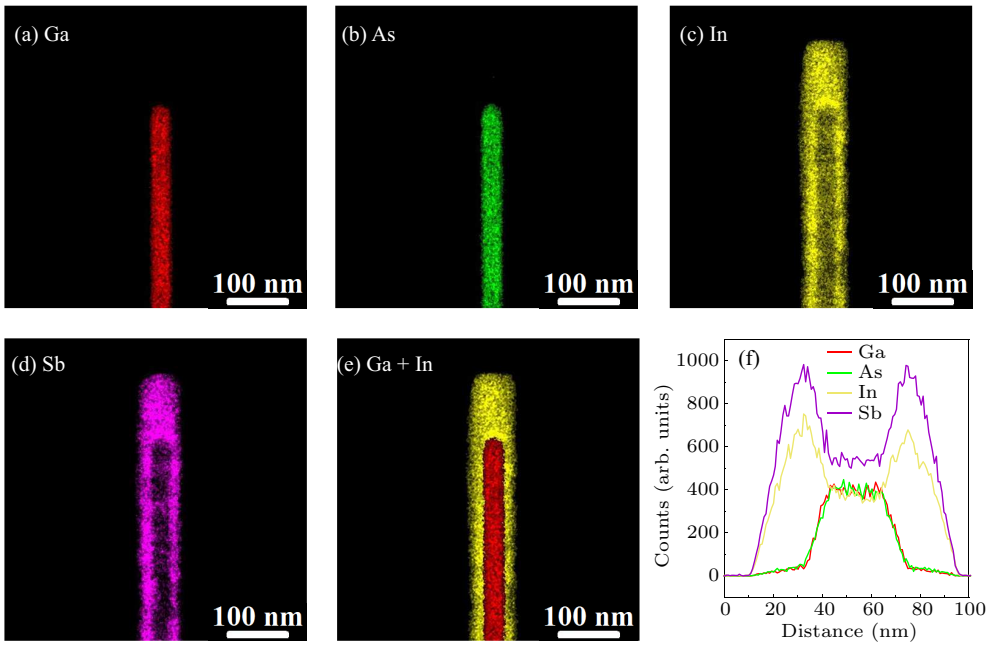


Fig. 6. Chemical composition analysis of the GaAs/InSb core–shell nanowires. (a)–(d) False-color EDS elemental maps showing the distribution of Ga, As, In, and Sb, respectively, from the upper section of the nanowire. (e) Composite EDS map showing the co-distribution of Ga and In. (f) Compositional line profile across the upper section of the nanowire.

To investigate the elemental distribution within the GaAs/InSb core–shell nanowires, EDS measurements were performed. Figures 6(a)–6(e) show the EDS images of the same GaAs/InSb core–shell nanowire as depicted in Fig. 5. The images clearly demonstrate that the GaAs core is fully coated by the InSb shell, as evidenced by the EDS results. Additionally, axial growth of InSb is observed at the top of the GaAs core, in addition to the radial growth of the InSb shell. Furthermore, using EDS line scans, as shown in Fig. 6(f), the diameter of the GaAs core and the thickness of the InSb shell were quantitatively measured to be approximately 50 nm and 25 nm, respectively.

To further obtain microstructural information on the GaAs/InSb core–shell nanowires, we prepared cross-sectional samples of the core–shell nanowires and conducted a detailed analysis of their cross-sectional microstructures and compositional distributions. As depicted in Fig. 7(a), the hexagonal cross-section, along with the GaAs/InSb core–shell structure and interface of a nanowire sample, can be clearly observed. As shown in Figs. 7(b)–7(e), the SAED pattern and high-resolution TEM images confirm that both the GaAs core and the InSb shell exhibit zinc-blende crystal structures. The InSb shell uniformly coats the GaAs core. For this sample, the diameter of the GaAs core and the thickness of the InSb shell were quantitatively measured to be approximately 50 nm and 20 nm, respectively, through high-resolution TEM imaging and EDS line scans (Figs. 7(f)–7(m)). Additionally, cross-sectional measurements were taken for the axial growth of InSb at the top of these nanowires (refer to Fig. S1 in supporting information).

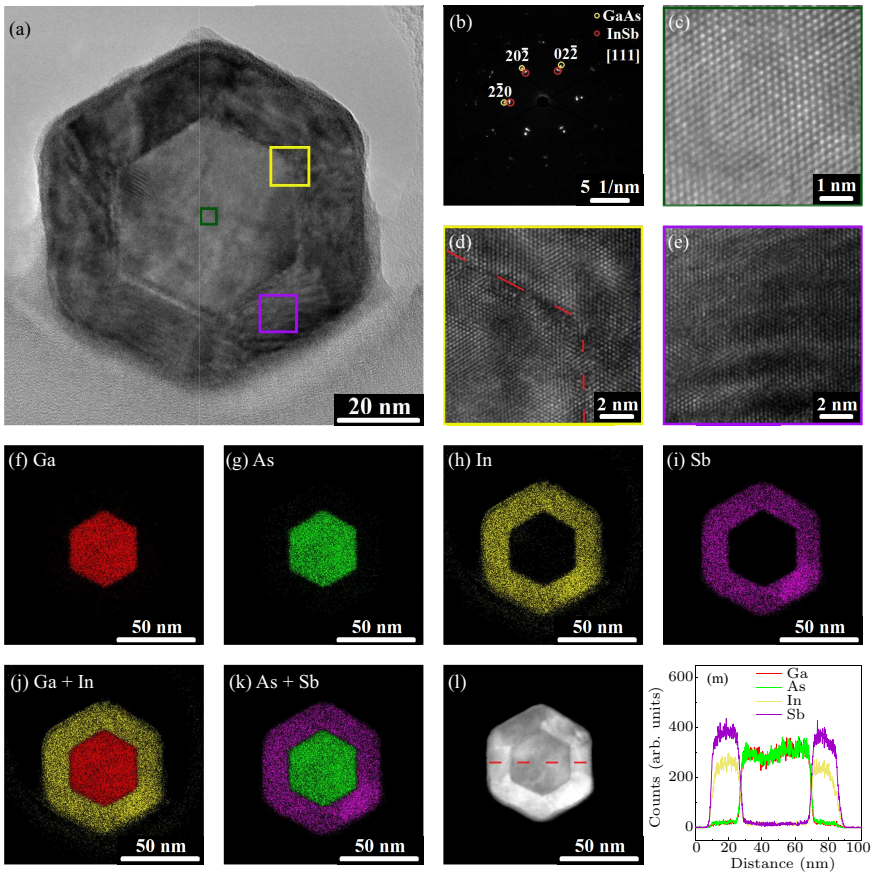


Fig. 7. Crystal structure and chemical composition of a cross-sectional sample of GaAs/InSb core–shell nanowires. (a) Low-resolution cross-sectional TEM image of the GaAs/InSb core–shell nanowire grown with an Sb/In flux ratio of 4.36. The colored rectangles highlight the regions where the high-resolution TEM images were recorded. (b) Fast Fourier transform pattern corresponding to the entire sample. (c)–(e) High resolution TEM images taken from the colored regions of panel (a). (f)–(i) False-color EDS elemental maps of Ga, As, In, and Sb of the sample, respectively. (j) False-color EDS elemental map of Ga and In of the sample. (k) False-color EDS elemental map of As and Sb of the sample. (l) HAADF–STEM image of the sample. (m) EDS line scans taken along the red dotted line in panel (l).

To further investigate the strain state of the sample, we performed filtering on high-resolution TEM images of cross-sectional GaAs/InSb core–shell nanowire samples. This filtering process aimed to reduce image noise and enhance resolution, enabling subsequent strain analysis using the geometric phase analysis method via Strain++ software. Initially, we examined the strain state at the GaAs/InSb interface. As clearly discernible from the high-resolution TEM image in Fig. 8(a), there exists a distinct interface between GaAs and InSb. The corresponding strain maps, ε_{xx}, ε_{xy}, and ε_{yy}, derived from the high-resolution TEM image in Fig. 8(a), are presented in Figs. 8(b)–8(d), with GaAs set as the reference for 0% strain. Similar to several previous studies, the ε_{xx} and ε_{yy} strain maps reveal approximately 15% strain between GaAs and InSb, consistent with the lattice mismatch between these two materials.[35,36] This observation underscores the charac-

teristic strain resulting from the coexistence of two materials with different lattice constants but the same crystal structure. However, the ε_{xy} map in Fig. 8(c) indicates that, in addition to stress relaxation through dislocations at the GaAs/InSb interface, residual strain persists within the InSb shell. This finding contrasts with the ε_{xy} maps reported in previous works,[35,36] where the material with a larger lattice constant exhibited 0% strain relative to the material with a smaller lattice constant. We hypothesize that this discrepancy arises from the hexagonal core–shell nanowire geometry of our sample, in contrast to the bulk material interfaces examined in previous studies. The strain states in these two scenarios differ significantly. Mengistu *et al.* conducted a theoretical calculation to analyze the strain state of a cross-sectional Ge/Si hexagonal core–shell nanowire and demonstrated the presence of a symmetrical stress distribution within the nanowire shell, which, to a certain extent, affects the strain of the nanowire core.[37] This finding aligns with our strain analysis results. Furthermore, due to the 14.6% lattice mismatch between InSb and GaAs, the InSb shell initially undergoes island growth before gradually transitioning from a rough to a smooth surface, rather than forming a single, integrated crystal. This growth process may also contribute to the complex strain state observed within the InSb shell. Additionally, strain analysis was performed on the axially grown InSb at the top of these nanowires (refer to Fig. S2). The results clearly indicate that there is virtually no strain in the axially grown InSb cross-section, suggesting that the strain has been fully released during the axial growth process. This observation is consistent with the TEM image of the entire nanowire (refer to Fig. 5(a)).

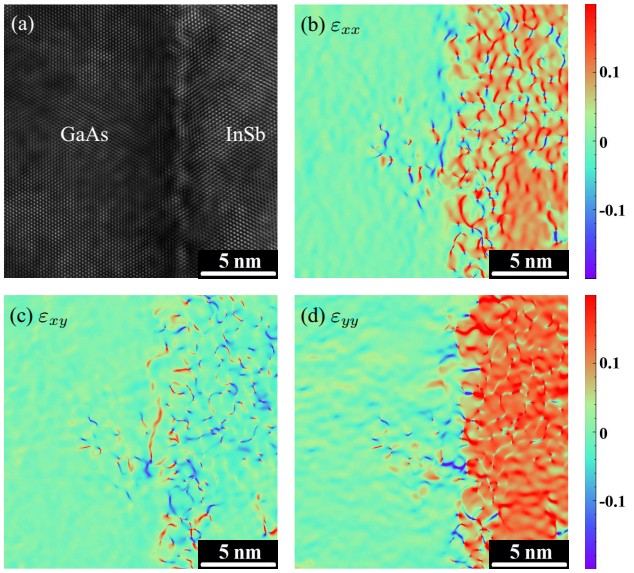


Fig. 8. Strain analysis of a cross-sectional sample of GaAs/InSb core–shell nanowires. (a) Filtered high-resolution TEM image of the cross-sectional GaAs/InSb core–shell nanowire grown with an Sb/In flux ratio of 4.36. (b)–(d) Strain maps of ε_{xx}, ε_{xy}, and ε_{yy}, respectively, corresponding to the high-resolution TEM image presented in panel (a).

To characterize the electrical properties of GaAs/InSb core–shell nanowires, we fabricated nanowire FET devices with a back-gate voltage (V_g) and source–drain voltage (V_{ds}). The current–voltage (I_{ds}–V_{ds}) curves and transfer characteristic (I_{ds}–V_g) curves were measured at 300 K. Figure 9(a) displays the I_{ds}–V_{ds} curves as a function of V_g ranging from −40 V to 40 V at 300 K. The nanowire device exhibits good linearity and current saturation, indicating that the device demonstrates favorable ohmic characteristics. The contact separation length of the nanowire device is approximately 1 μm (refer to Fig. 9(a)).

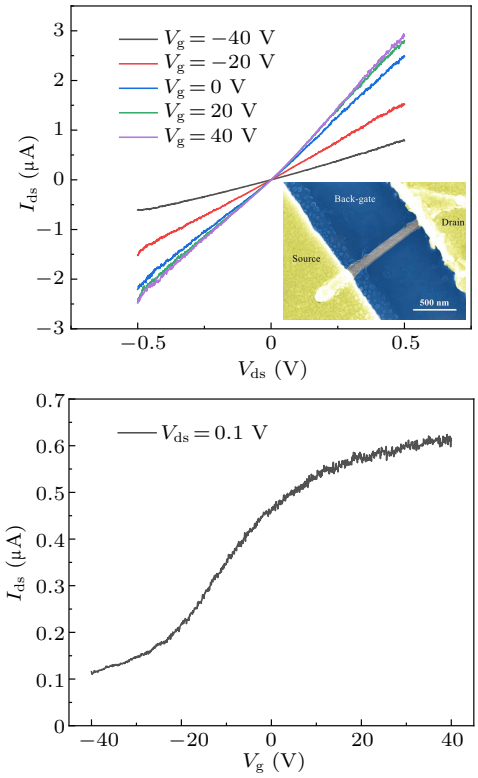


Fig. 9. Electrical properties of GaAs/InSb core–shell nanowires. (a) I_{ds}–V_{ds} curves with different gate voltages of ∼ 100-nm diameter GaAs/InSb nanowire FET with a gate length of ∼ 1 μm at $T = 300$ K. The inset shows the false-color SEM image of the GaAs/InSb nanowire FET. (b) I_{ds}–V_g curve of the FET at $T = 300$ K.

Furthermore, the diameter of the GaAs core and the thickness of the InSb shell were quantitatively measured to be approximately 40 nm and 25 nm, respectively, based on the EDS measurement results. The resistivity of the InSb shell at 300 K was calculated to be approximately 8.8×10^{-2} Ω·cm. As shown in the I_{ds}–V_g curve (refer to Fig. 9(b)), the device exhibits n-type conduction without any additional doping. However, the off-state current of the device is relatively high at room temperature, resulting in an on-off ratio of approximately 6, which indicates that the device cannot be fully turned off. This phenomenon is consistent with observations in previous studies and can be attributed to the narrow bandgap of the materials.[38,39] There are several other potential methods to enhance the on/off ratio of narrow-bandgap semiconductor nanowire devices, including surface passivation,[40–43] gate dielectric engineering[44] and heterostructure design.[45] Addi-

tionally, using the transfer characteristic curve, the carrier mobility of the nanowires was calculated to be 50 $cm^2 \cdot V^{-1} \cdot s^{-1}$ according to the relevant formula, $\mu = g_m L^2/(CV_{ds})$, where g_m is the transconductance, L is the channel length, C is the capacitance, and V_{ds} is the source–drain voltage.[46] For more information on device testing and the electrical properties of samples, please refer to the supporting information (Figs. S3 and S4). We acknowledge that the InSb shell in our GaAs/InSb core–shell nanowires contains defects due to lattice mismatch, leading to lower electron mobility compared to InSb nanowires/nanosheets;[47,48] going forward, we aim to optimize the InSb shell quality by exploring alternative growth methods, adjusting parameters, and thoroughly investigating strain relaxation's impact on device performance to enhance electron mobility.

4. Conclusion

In conclusion, by leveraging self-catalyzed pure zinc-blende GaAs nanowires as the core material, we achieved the epitaxial growth of InSb shells with optimized smoothness and continuity. The systematic investigation into the growth conditions revealed that precise control over the InSb shell growth temperature (390 °C) and Sb/In BEP ratio (4.36) is crucial for obtaining high-quality core–shell structures. Advanced TEM techniques, including high-resolution TEM, SAED, and EDS mapping, confirmed the successful formation of the core–shell architecture with a pure zinc-blende crystal structure for both the GaAs core and InSb shell. Despite the substantial lattice mismatch ($\sim 14.6\%$) between GaAs and InSb, the majority of the InSb shell exhibited high crystallinity, with only a limited number of twin boundaries and dislocations. Strain analysis using geometric phase analysis on cross-sectional high-resolution TEM images revealed significant strain at the GaAs/InSb interface, consistent with theoretical predictions. The ε_{xx} and ε_{yy} strain maps indicated approximately 15% strain, while the ε_{xy} map highlighted residual strain within the InSb shell, suggesting complex strain relaxation mechanisms influenced by the hexagonal core–shell nanowire geometry. Electrical characterization of back-gated FET devices fabricated from these nanowires demonstrated favorable ohmic characteristics and n-type conduction without intentional doping. The carrier mobility was calculated to be 50 $cm^2 \cdot V^{-1} \cdot s^{-1}$, and the resistivity of the InSb shell at 300 K was approximately 8.8×10^{-2} Ω·cm. Future research will focus on further optimizing the growth parameters to minimize defects and strain, thereby enhancing the electrical properties. Additionally, we will explore the integration of these nanowires into complex device architectures to fully harness their unique electronic and quantum properties, paving the way for advancements in quantum computing, spintronics, and optoelectronic applications.

Data availability statement

The data that support the findings of this study are openly available in Science Data Bank at https://doi.org/10.57760/sciencedb.j00113.00262.

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