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A novel stack-HfO_2 top-gate structure for improving performance of network carbon nanotube transistor

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Carbon nanotubes (CNTs) are regarded as a powerful contender to replace Si transistors after Moore's law due to their advantages such as quasi-ballistic transport, high carrier mobility, and low power consumption. In the traditional CNT preparation process, CNTs are deposited on SiO_2 substrate and then the gate dielectric is deposited. In this structure, pinholes will appear between CNTs and dielectric layer, which will affect the gate-control and increase the gate leakage current. Therefore, in this paper, we designed a new stack-HfO_2 top-gate (STG) network CNTFET. By filling the pinholes between CNTs and dielectric layer, the contact interface condition is improved, reducing the subthreshold swing and improving I_{on}/I_{off} of the device. Meanwhile, through first-principles calculations, compared with the conventional structure, the interface charge transfer value of the CNT/HfO_2 interface for STG is about 5 times smaller than that of CNT/SiO_2 interface. Specifically, the mobility and *SS*, and I_{on}/I_{off} of the STG structure are 130 $cm^2/V{\cdot}s$, 156 mV/dec, and 10^7, respectively. Taking into account the above advantages, the proposed STG structure has reference value for improving the performance of CNTFET.

Keywords: carbon nanotube, HfO_2, gate dielectric, interface

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1. Introduction

Over the past few decades, as Moore's law approaches its theoretical limit, Si CMOS technology will soon reach performance limit. Typically, as one of the emerging two-dimensional (2D) materials, carbon nanotubes (CNTs), due to excellent properties such as nanoscale size, high carrier mobility, and quasi-ballistic transport, can theoretically provide better scaling characteristics and lower power consumption than Si CMOS, and has become a strong contender for building the next-generation field-effect transistors.[1–3] Currently, aligned CNTs (A-CNT) are widely used to construct radio frequency integrated circuits, with typical applications including,[4–7] which have high DC and RF performance at mm-wave and THz frequencies.[8–10] However, for certain applications such as biological and gas sensors, the requirement for CNT films is to stack multiple layers to achieve a larger contact area, increase the specific surface area and adsorption sites.[11] Moreover, for the network CNT (N-CNT), the cross points of CNTs form natural electrical contacts, reducing interface resistance, while A-CNTs rely on end contacts, resulting in higher contact resistance. Besides, N-CNTs have advantages of low cost and easy fabrication. Given the superiority of N-CNTs, this work focuses on optimizing the performance of carbon nanotube field-effect transistor (CNTFET), which holds significant potential for practical applications. It is widely recognized that the performance of CNTFETs strongly depend on material, and high-quality, high-purity semiconductor films covering the substrate are necessary for CNT-based integrated circuits. Currently, solution-based CNT films are the most widely used material system in CNT thin film transistors, as they have been used to build multi-functional integrated circuits, including large-scale ICs composed of hundreds of transistors and ring oscillators with more than 300 stages.[6,12] However, like most semiconductor materials with high carrier mobility (such as Ge, and InSb), CNTs have a smaller bandgap width (below 1 eV) and effective mass.[13,14] Due to the small bandgap width and effective mass, CNTFETs do not have good structural design and are prone to severe gate-control degradation and bipolar behavior, especially under high drain voltage, which is unacceptable for low-power digital devices. Obviously, optimizing the deposition state of CNTs and structure of CNTFETs is urgent. In the conventional process of CNTFETs, the SiO_2 substrate is directly immersed in the high-purity CNT solution to form CNT film. The problem with this method is that the HfO_2 directly nucleates non-uniformly on the N-CNTs and the SiO_2 under

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the N-CNTs voids, forming a film with pinholes and causing discontinuity of the film. This will undoubtedly affect the gate-control characteristics of the device, deteriorating the I_{on}/I_{off} and *SS* of CNTFETs.

In this work, we proposed a new stack-HfO_2 top-gate transistor structure (STG). Moreover, we illustrate how to use a stack-HfO_2 structure to optimize the interface state between CNTs and gate dielectric, improving the continuity of gate dielectric. Through first-principles calculations, it was verified that the CNT/HfO_2 interface has a smaller Bader charge transfer quantities than the CNT/SiO_2 interface. This key factor causes the device to have a lower leakage current and improves I_{on}/I_{off} of the device, enhancing the gate-control capability of the device. Therefore, I_{on}/I_{off}, mobility and *SS* of the device have been significantly improved.

2. Experiment

To prove that the stack-HfO_2 structure can suppress gate degradation, this paper analyzed the deposition behaviors of CNTs and gate dielectric with and without the underlying HfO_2 film. For the traditional top-gate structure, CNTs are deposited on 250-nm SiO_2, while the HfO_2 gate dielectric is covered on the CNTs and the SiO_2 beneath the voids of N-CNTs. Moreover, according to reference,[15] for the conventional structure, under the ALD deposition condition of 90 °C, the HfO_2 gate dielectric will nucleate on both the bare SiO_2 and the CNTs (the nucleation on the CNTs may be due to the promotion of the physical adsorption of the precursor on the CNTs surface or the reduction of the surface diffusion rate).

However, since the deposition of HfO_2 on SiO_2 is a heterogeneous growth, inevitable film non-uniformity and lattice mismatch occurs, and the discontinuity of the dielectric layer leads to pinholes, thereby causing leakage current and reducing the dielectric performance of the HfO_2 film. Different from this growth mode, for the STG structure, the gate dielectric is deposited on the same type of film substrate (HfO_2) and the CNTs, the substrate and deposited material are homogeneous, the chemisorption of ALD precursor on the surface is more uniform, the self-limiting reaction is more sufficient, and the film formation uniformity is higher. That is, two structures present different CNT wrapped surfaces: the conventional structure (Fig. 1(a)) has parallel or trapezoidal interfaces, while the stack-HfO_2 structure has an Ω-shaped interface (the gate dielectric is tightly wrapped with the CNTs) (Fig. 1(b)). The cross-sectional TEM image of HfO_2-CNT interface and the EDX mapping are shown in Figs. 1(c) and 1(d), which demonstrate the improvement of the pinholes.

Therefore, we proposed the STG structure, which can produce an ideal interface to maximize the contact area between HfO_2 and carbon nanotubes, and thereby improve the gate-control capability. The schematic and process flow of the device are shown in Fig. 2(a).

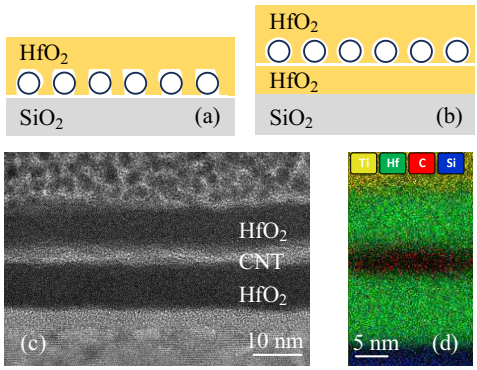


Fig. 1. Schematic diagram of HfO_2 and CNT interface for (a) conventional structure, (b) stack-HfO_2 structure, (c) cross-sectional TEM image of HfO_2–CNT–HfO_2 interface, and (d) the corresponding EDX mapping.

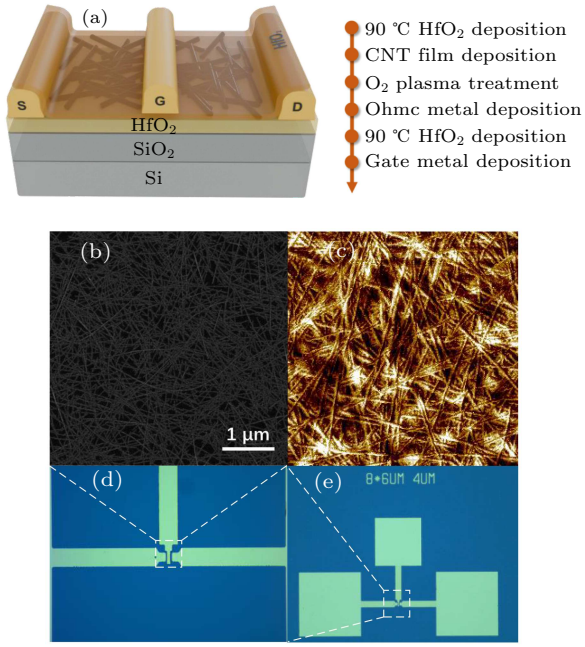


Fig. 2. (a) Schematic diagram and process flow of the STG-CNTFET, (b) SEM images of network CNT film, (c) AFM image of network CNT film in the area of 1 μm×1 μm, (d) and (e) optical images of the device after fabrication.

First, a 10-nm HfO_2 layer was prepared on an Si wafer with 250-nm SiO_2 at 90 °C by ALD. The substrate was then immersed in a CNT solution with semiconductor purity up to 99%. The carbon nanotube materials used in this article were purchased from the "Carbon Solution, Inc." company. The product descriptions are as follows: purified SWNTs; single-walled carbon nanotubes were prepared by the arc discharge method. AP. SWNT purified by air oxidation and subsequently treated to remove the catalyst. Carbonaceous purity reaches to 99% and the typical bundle length is 1 μm–5 μm and 1.55 ± 0.1 nm, respectively. A random network CNT film was prepared. The SEM and AFM characterization images of the CNT film at 3×10^4 magnification and within 1 μm×1 μm range are shown in Figs. 2(b) and 2(c). It can

be seen that the CNT film has good uniformity, with a density of approximately 40 CNTs/μm and a diameter distribution of 1.5 ± 0.25 nm. This provides feasibility for the subsequent preparation of large-scale CNT-based ICs. Before the formation of CNTFETs, the samples were cleaned with toluene to remove polymers and impurities on the sample surface. The manufacturers and models of key instruments key instruments are illustrated as follows: The SEM and TEM test analysis uses the *Apreo HiVac* and *Talos F200X* product from Thermo Fisher Scientific, respectively. And the AFM test analysis uses the *Park NX20* product from Park Systems.

The STG device was fabricated according to the following process flow: FIDU alignment mark was prepared by Cl-based ICP etching on the substrate, then ohmic contacts were formed by photolithography and Pd (50 nm) electron beam evaporation (EBE), and then standard metal lift-off process was carried out. Then, the device isolation was performed by oxygen plasma treatment. The CNTs in the passive region were removed by using a power of 100 W and O_2 flow rate of 100 sccm for 1 min. The 10-nm HfO_2 gate dielectric was prepared by ALD at 90 °C. The gate electrode was defined by photolithography, and the gate metal Ti/Pd (5/50 nm) was formed by EBE and lift-off. Both HfO_2 film processes were completely the same, and CNTFETs were prepared on 2 cm×2 cm chips. The optical inspection images of the device are shown in Figs. 2(d) and 2(e). All device sizes were uniform, that is, the channel length (L_{sd}) and gate length (L_g) were 8 μm and 4 μm, respectively. Then, the devices were measured at room temperature using the Cascade probe station and Keithley 4200 semiconductor analyzer.

3. Results

To further demonstrate the improvement of the STG structure, the transfer characteristics of multiple STG and traditional top-gate structure (TTG) devices were measured under $V_d = -1$ V as shown in Fig. 3(a). The I_{dmax} and g_m of the STG device were 4 μA/μm and 2.6 μS/μm, respectively, with an *SS* of 156 mV/dec and a V_{th} of −0.75 V (the voltage at 10^{-6}-μA/μm current). The subthreshold characteristics of this device are at the forefront of network CNTFETs of the same size.[13,16] Figure 3(b) shows the DC characteristic of different channel length with STG structure. I_d and V_{bias} show an ideal linear relationship, indicating that the interface between CNTs and metal is good and there are no excess contaminants.[10] The contact resistance R_c extracted by the TLM model is 14.6 Ω·mm, and the sheet resistance R_{sh} is 50401 Ω/sq. Figure 3(c) shows the output curves of two structures. At the bias of $V_g = -5$ V and $V_d = -5$ V, the I_{dmax} of the STG device is 9.2 μA/μm, which is greater than 4.5 μA/μm for the TTG structure. Figure 3(d) shows the I_{on}/I_{off} and *SS* statistics of the STG and TTG structures. The results show that the interface conditions between the CNTs and gate dielectric are significantly improved, which is reflected in lower I_{off} and higher I_{on}. We found that the introduction of the underlying HfO_2 layer compared to the TTG structure improved the gate-control ability of the device and significantly increased the I_{on}/I_{off} of the device, reaching above 10^7. Figure 3(e) shows the *C*–*V* curves of two structures.

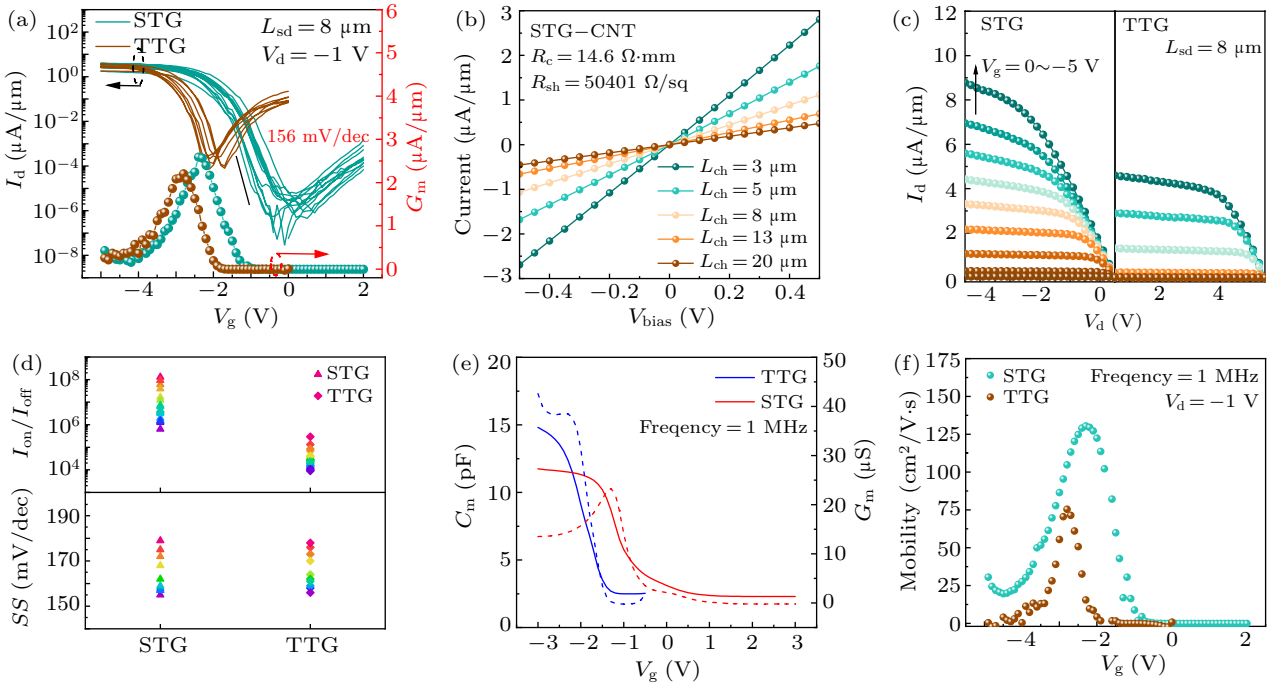


Fig. 3. (a) Transfer characteristic curves of STG and TTG–CNT under $V_d = -1$ V, (b) *I*–*V* characteristics of devices with W_g of 100 μm, (c) output curves of STG and TTG–CNT with V_g varying from 0 to −5 V, (d) I_{on}/I_{off} and *SS* statistics of different CNTFET structures, (e) measured *C*–*V* (solid line) and *G*–*V* (dashed line) curves of two MOS structures at 1 MHz, (f) field-effect mobility of STG and TTG–CNT.

The capacitance was obtained at 1 MHz for the FATFET devices, with a size of $W_g = 100$ μm and $L_g = 50$ μm. Figure 3(f) shows the mobility curves extracted from the *C*–*V* tests of two structures, according to the following formula:[17]

$$\mu = \frac{g_m \times L}{W \times C_g \times V_d}, \tag{1}$$

where g_m represents the transconductance of the device, L and W denote the gate length and gate width of the device, C_g is the gate capacitance. For calculation of the capacitance, we did not use the parallel plate estimate, because this method overestimates the oxide capacitance (and hence under-estimates the mobility) when the network density is not high enough.[18] We can observe that the STG structure significantly enhances the carrier mobility of the device, reaching up to 130 $cm^2/V{\cdot}s$. There are more defects at the interface between SiO_2 and HfO_2, and these interface charge traps capture hole carriers, forming Coulomb scattering centers. When the hole moves in the channel, these scattering centers will hinder its movement, increase the scattering probability, and thus reduce the channel mobility. This leads to the STG-CNTFET having a higher on-state current. Here, a comparison of the performance of this work with that of previously published network and aligned carbon nanotube films,[8,20–32] is presented in Figs. 4(a) and 4(b).

This paper also quantitatively compared the charge transfer characteristics of two structures. First-principles calculations based on density functional theory (DFT) were conducted to investigate the interfacial properties of CNT/SiO_2 and CNT/HfO_2 heterostructures. The exchange–correlation interactions were treated using the Perdew–Burke–Ernzerhof (PBE) of the generalized gradient approximation (GGA), with a plane-wave kinetic energy cutoff of 500 eV.[33] The computational models were constructed by aligning a (19,0) single-walled carbon nanotube (SWCNT) on two distinct substrates: the (100) surface of stishovite-phase SiO_2 and the (100) surface of cubic-phase HfO_2, respectively. The interfacial lattice mismatch between the CNTs and both oxide substrates was systematically minimized to below 5%, ensuring coherent heterointerface formation. A 20-Å vacuum layer was introduced along the non-periodic direction to effectively eliminate spurious interactions between periodic images of the heterostructures. To analyze the evolution process of charge transfer under the action of an applied electric field, the electric field was applied in the calculation. The Bader charge (BC) provides reference for the electron distribution around each atom. Therefore, ΔBC can be used as an indicator of charge transfer at the interface.[34] ΔBC is defined as the charge transfer between two sides of the heterojunction. The direction of the applied electric field in the heterostructure is aligned with the positive *z*-axis direction, that is, along the direction of the oxide-CNT.

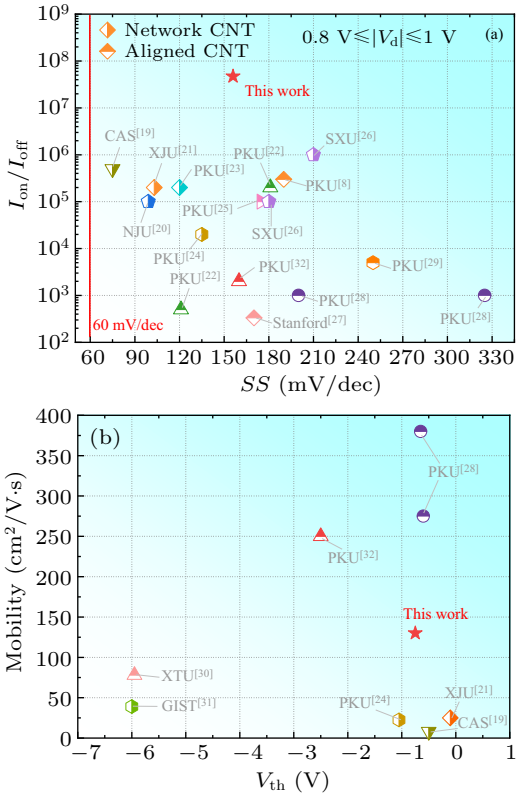


Fig. 4. Comparisons of (a) *SS* and I_{on}/I_{off}, (b) V_{th} and mobility of previously reported aligned and network CNTFET.

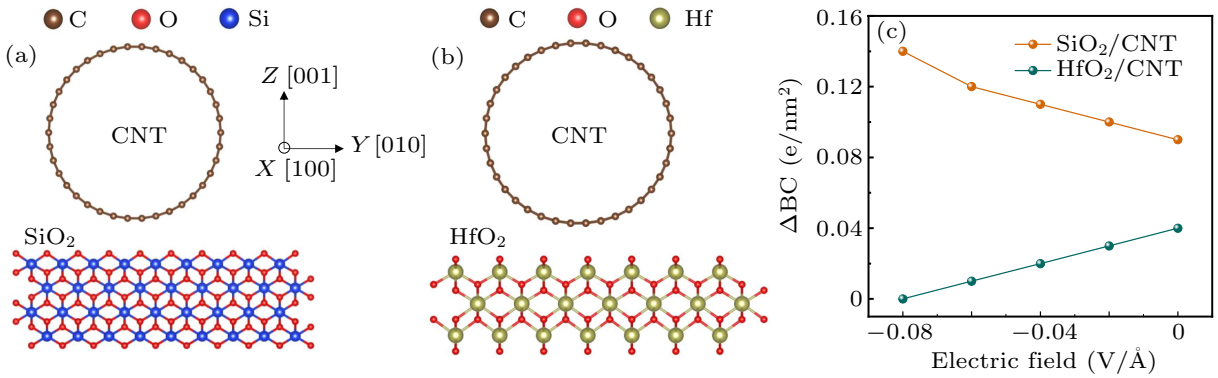


Fig. 5. Views of relaxed structures of (a) CNT/SiO_2 and (b) CNT/HfO_2 heterostructures, (c) ΔBC as a function of electric field at CNT/HfO_2 and CNT/SiO_2 interface, respectively.

The heterojunction structures of SiO_2 and HfO_2 with CNT are shown in Figs. 5(a) and 5(b). Figure 5(c) shows the transfer charge quantities of the interfaces for the two heterojunction structures. When the electric field changes from 0 to 0.08 V/Å, ΔBC of the CNT/HfO_2 interface is 3–5 times smaller than that of the CNT/SiO_2 interface. The accumulation of Bader charge causes holes tunneling at the heterojunction interface, thereby increasing the leakage current at the off-state of the device. Thus, the interface of CNT/HfO_2 is more likely to suppress charge transfer under negative V_g, thereby improving the off-state characteristics of the device.

4. Conclusions

In conclusion, we fabricated a novel stack-HfO_2 top-gate CNTFET by depositing an HfO_2 on the substrate prior to CNT film deposition. The introduction of the bottom HfO_2 layer enhances the overall performance of CNTFET, manifesting in a higher I_{on}/I_{off}, lower leakage current, and smaller *SS*. A comparative analysis of the gate dielectric formation processes for two structures reveals that the improved gate controllability for STG arises from the homogeneous growth of HfO_2 gate dielectric within the CNT network gaps. This process minimizes pinholes, improves film quality, and enhances encapsulation of gate dielectric to CNTs, collective contributing to superior performance. Besides, first-principles calculations of interfacial transfer charge under electric fields demonstrate that the CNT/HfO_2 interface exhibits significantly less BC transfer compared to the conventional CNT/SiO_2 interface, thereby reducing I_{off}. Obviously, this novel STG-CNTFET exhibits better characteristics, including higher mobility, higher gate modulation efficiency and lower static power consumption. It has potential for enhancing the performance of CNTFETs and even for constructing large-scale CNT-based ICs.

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