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Effect of a deep virtual guard ring on performance of a miniaturized high-photosensitivity silicon single-photon avalanche diode

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We developed a miniaturized high-sensitivity single-photon avalanche diode (SPAD) device based on 180 nm bipolar complementary metal–oxide–semiconductor double-diffused metal–oxide–semiconductor technology and investigated the effect of a deep virtual guard ring (VGR) on device performance. To mitigate the degradation in photon detection efficiency (PDE) and dark count rate (DCR) induced by device scaling, we innovatively implemented a P-type implant/high-voltage n-well SPAD structure. This configuration deepens and widens the multiplication region to broaden the spectral response, while the specialized adoption of the P-type epitaxial VGR technology suppresses premature edge breakdown and reduces dark noise. Furthermore, a unique layout was devised to maximize the photosensitive area and increase the fill factor of the device. Through technology computer-aided design simulations, the effect of the guard ring width on the electric field distribution inside the device was systematically studied. Experimental results demonstrate that the fill factor of the device reaches 31.5% when the pitch is scaled down to 8.5 μm. The novel device achieves a high peak PDE of 24% at 555 nm and an ultralow DCR of 0.41 cps·μm^{-2} at 5 V excess bias voltage.

Keywords: single-photon avalanche diode (SPAD), virtual guard ring (VGR), photon detection efficiency (PDE), dark count rate (DCR), premature edge breakdown (PEB)

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1. Introduction

Silicon-based single-photon avalanche diodes (SPADs) exhibit remarkable performance characteristics, distinguished by their notable advantages in low-cost manufacturing, large-scale production capacity and the capacity for monolithic integration with complementary metal–oxide–semiconductor (CMOS) circuits.[1–3] These attributes have rendered them indispensable in a wide array of applications, including, but not limited to, three-dimensional (3D) ranging and imaging systems, fluorescence lifetime imaging (FLIM) techniques, Förster resonance energy transfer (FRET), Raman spectroscopic analyses and other low-light detection scenarios.[4–7] The current trend is to use submicron standard CMOS technologies to implement densely integrated arrays based on small pixels. Consequently, key performance requirements include a high photon detection efficiency (PDE) across the visible to near-infrared (NIR) spectrum, a low dark count rate (DCR), reduced pixel pitch and enhanced integration density on a single chip.

Over the years, researchers have explored various technological paradigms for SPAD fabrication. Conventional CMOS-based SPADs utilizing p+/n-well (NW) or n+/p-well (PW) junctions frequently exhibit increased tunneling-induced noise due to their high doping concentrations.[8] While employing lightly doped PW and deep n-well (DNW) junctions can partially suppress tunneling effects,[9] such structures typically demonstrate insufficient sensitivity in the green-to-red spectral range, which is essential for applications such as FLIM, FRET and fluorescence correlation spectroscopy.[10,11] In contrast, custom silicon fabrication processes, specifically optimized for SPAD performance, achieve a very high PDE of 50% at 550 nm, while maintaining a low DCR below 10 counts per second (cps) at room temperature and superior dynamic range characteristics.[12] These performance improvements arise from the enhanced design flexibility in doping profiles and electric field optimization offered by dedicated fabrication technologies. Nevertheless, the complexity of these specialized processes inevitably leads to higher production costs.

A parallel challenge in SPAD development lies in device miniaturization.[13,14] Reducing the guard ring width (GRW) helps to increase the effective photosensitive area but enhances the edge electric field, causing band-to-band tunneling (BTBT) and trap-assisted tunneling (TAT) effects to become the dominant mechanisms of dark count generation.[15] Reducing the size of the active region can improve the SPAD integration density but directly lowers the fill factor (FF), limiting the PDE of the device.[16] Therefore, optimizing the guard ring size and structure is crucial for realizing a SPAD array with both a high PDE and low DCR.

In this paper, we propose an innovative solution to im-

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prove the overall performance of the SPAD in 180 nm bipolar CMOS-double-diffused metal–oxide–semiconductor (DMOS) (BCD) technology. A deep-junction P-type implant/high-voltage n-well (HVNW) structure with a deep virtual guard ring is used for NIR enhancement and dark noise reduction. Precise control of the electric field inside the guard ring is performed for the achievement of high light sensitivity and a low DCR. The effect of the physical mechanism on the device characteristics is analyzed and explained by means of technology computer-aided design (TCAD) simulations.

2. Structure design and TCAD simulation

2.1. Device structure

Figure 1(a) shows a 3D cross-section of the proposed compact SPAD optimized for high-density integration. To attain superior PDE performance, two pivotal design strategies have been implemented. Firstly, the avalanche multiplication region of the device is positioned at the P-type implant/HVNW interface. This deep-junction design enhances the absorption efficiency of NIR photons. Secondly, the adoption of a lightly doped P-type epitaxial (P-epi) layer to construct a virtual guard ring (VGR) can effectively mitigate the degradation in photon detection probability (PDP) caused by traditional GRW reduction.

For DCR suppression, a comprehensive approach incorporating multiple advanced techniques has been employed. Primarily, the integration of shallow trench isolation (STI) between P+ and N+ layers serves to disperse surface electric fields, thereby reducing tunneling-induced dark counts at defect sites. Furthermore, the implemented VGR structure not only attenuates the electric field intensity within the VGR region but also functions as an effective barrier that prevents the diffusion of STI interface defects into the critical avalanche region, consequently diminishing the dark noise. Additional structural innovations include the incorporation of a high-voltage N-type buried layer (HVBN), which forms a reverse-bias PN junction with the substrate to effectively suppress electrical crosstalk between adjacent pixels.

In addition, a unique layout shown in Fig. 1(b) has been devised to maximize the FF of the device. The avalanche multiplication region of the device adopts a chamfered-square geometric configuration, where the device cathodes are positioned at the four chamfered corners. This design shortens the width of the cathode ring, thereby maximizing the device FF to the greatest extent. The choice of proper physical dimensions, especially the sizes of the GRW and active diameter (AD), is important for the better performance of Si SPADs. Theoretical analysis reveals that reducing the GRW under a fixed active size enhances the FF but may intensify the electric field in the guard ring (GR), potentially leading to an increased DCR. To elucidate the underlying physical mechanisms, device simulations were performed using Silvaco TCAD tools.

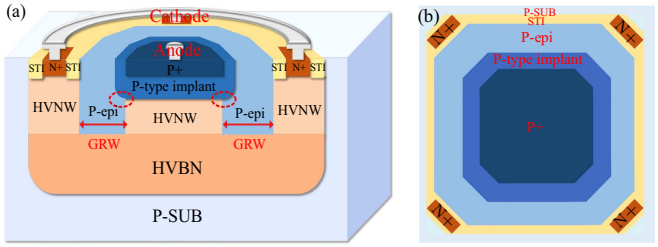


Fig. 1. (a) 3D cross-sectional view of the proposed SPAD. (b) Top view of the proposed SAPD.

2.2. TCAD simulation

Figures 2(a)–2(d) show the 2D electric field distributions with varying GRWs at 5 V excess bias for a fixed AD of 5 μm.

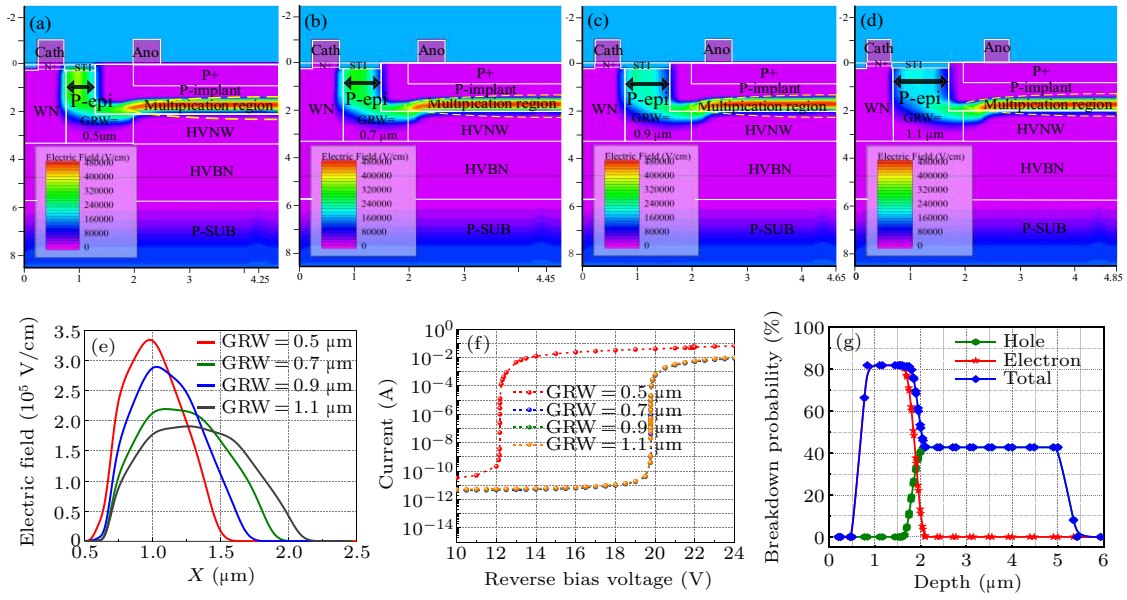


Fig. 2. (a–d) The 2D electric field distributions of four SPADs with GRWs of 0.5 μm, 0.7 μm, 0.9 μm and 1.1 μm, respectively. (e) 1D electric field profiles and (f) simulated *I*–*V* curves of four SPADs. (g) Distribution of carrier avalanche triggering probability along the active region depth at GRW = 0.7 μm.

When the GRW is shrunk to 0.5 μm, severe field crowding is found in the narrow VGR region, producing a critical peak electric field of 3.4×10^5 V·cm^{-1} that risks premature surface breakdown. The 1D electric field profiles along a line at a depth of 1 μm in the guard ring are extracted, as illustrated in Fig. 2(e). With the GRW increasing to above 0.7 μm, this peak electric field is reduced to below 3.02×10^5 V·cm^{-1}, demonstrating that a wider GRW mitigates the edge field effect. The reverse *I*–*V* curves in Fig. 2(f) further confirm stable Geiger-mode operation with breakdown voltage (V_{BD}) of 20.5 V for all designs except the device with GRW = 0.5 μm, which suffers premature edge breakdown (PEB). Figure 2(g) extracts the depth-dependent distribution of the carrier avalanche triggering probability along the active region depth for the device with a GRW of 0.7 μm under an excess bias of 5 V. It is seen that the maximum avalanche probability of electrons is higher than that of holes, and the total avalanche triggering probability in the multiplication region reaches approximately 80%, demonstrating excellent photon detection sensitivity. Although TCAD simulations reveal that GRW critically modulates the guard ring electric field, probably diminishing BTBT and TAT effects to suppress DCR, experimental validation is needed to confirm these correlations.

3. Experimental results

Three SPAD devices with varying GRW sizes were fabricated in SMIC 180 nm BCD technology, and their chip micrographs are displayed in Fig. 3(a). Devices D2, D3 and D4 were designed with GRWs of 0.7 μm, 0.9 μm and 1.1 μm, respectively, and the same AD of 5 μm. Notably, the calculated FF value of D2 is as high as 31.5%, with a small pitch of 8.5 μm. D3 and D4 have a reduced FF because of the increased GRW.

3.1. The *I*–*V* characteristics

The *I*–*V* electrical characterization using a Keithley 4200A on the probe station shows a consistent breakdown voltage of about 20.5 V for all devices in dark conditions, and no PEB phenomenon is found in the small guard ring structures (Fig. 3(b)). The V_{BD} under illumination exhibits a marginal reduction due to the avalanche multiplication effect induced by photo-generated carriers. Owing to identical active-area doping and dimensions, all dark currents are at the pA level. The smaller GRW of 0.7 μm does not cause a larger dark current.

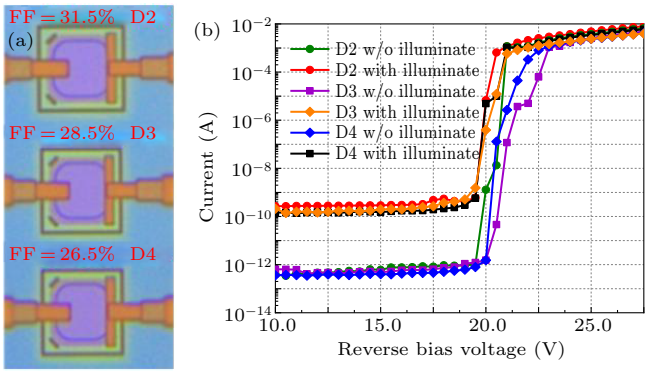


Fig. 3. (a) Microphotograph of devices D2, D3 and D4. (b) *I*–*V* curves for the three SPADs in dark and illuminated environments at room temperature.

3.2. Photon detection probability

As illustrated in Fig. 4, the PDP and DCR are measured by a passive quench/active recharge circuit through an off-chip quenching resistor of 50 kΩ,[17] with a dead time of 700 ns. To suppress the inherent background noise of the board-level circuit, a reference voltage of 800 mV is selected, ensuring that only avalanche signals triggered by genuine photons or dark counts exceeding this threshold are counted by subsequent circuits. The avalanche events are recorded and counted using a synchronous acquisition system implemented in a field-programmable gate array.

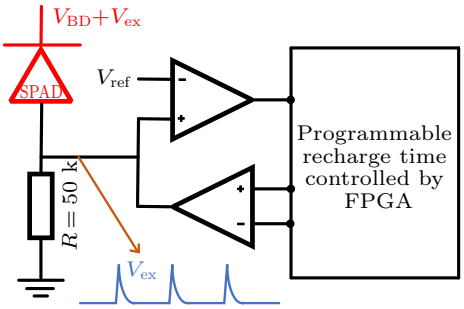


Fig. 4. Schematic of the passive quench/active recharge circuit with a dead time of 700 ns.

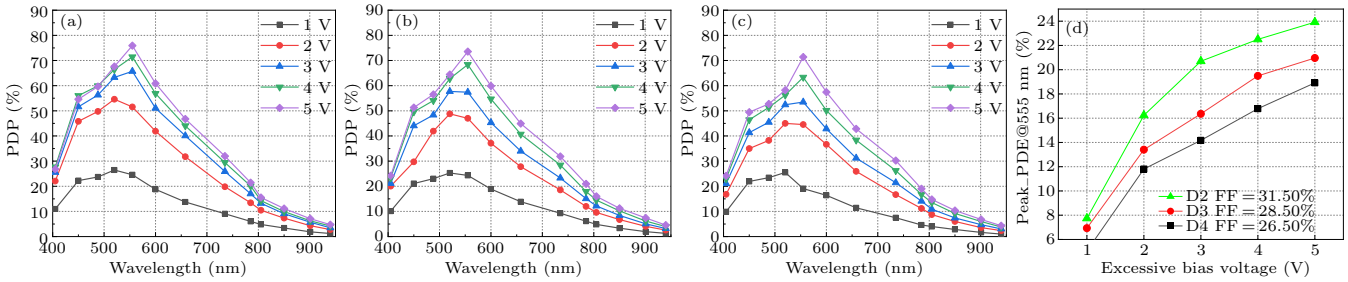


Fig. 5. (a)–(c) PDP versus photon wavelength response for devices D2, D3 and D4 at different excess biases. (d) Comparison of peak PDE at 555 nm for three SPADs with different FFs. PDE is defined as PDP × FF.

Figures 5(a)–5(c) depict the relationship between PDP and incident wavelength for devices D2–D4 under different excess bias voltages (V_{ex}). The proposed devices demonstrate a wide spectral response and infrared enhancement characteristics. Under $V_{ex} = 5$ V, the peak PDP values reach 75.93%, 73.55% and 71.37% at 555 nm for D2, D3 and D4, respectively. Moreover, D2 also reveals a higher NIR PDP of 7.09% at 905 nm than D3 and D4. The enhanced PDP of D2 stems from the stronger electric field confinement in the active region at a reduced GRW, improving carrier avalanche multiplication and thus boosting the PDP of the device.

Figure 5(d) compares the variation of peak PDE with V_{ex} for devices D2–D4. The peak PDE is enhanced from 26.5% to 31.5% with the GRW decreasing from 1.1 μm to 0.7 μm. This geometric modification directly increases the effective light-collection area, thereby emerging as a critical limiting factor for PDE enhancement.

3.3. Dark count rate

The essence of DCR lies in the avalanche effect induced by non-equilibrium carriers in the multiplication region, whose carrier generation mechanism is fundamentally similar to that of dark current under a conventional bias voltage. Only a portion of the carriers in the dark current can pass through the multiplication region and trigger avalanche events. If the surface dark current does not flow over the multiplication region it cannot trigger an avalanche and does not contribute to the dark count noise. Figure 6(a) depicts the variation of DCR with V_{ex} for the three devices at room temperature. At $V_{ex} = 5$ V, device D2 with GRW = 0.7 μm exhibits the highest DCR value (0.41 cps·μm^{-2}), while larger GRWs of 0.9 μm and 1.1 μm reduce the DCR by 47.6% and 60.8%, respectively. This phenomenon is closely associated with edge electric field enhancement in a smaller GRW, aggravating the TAT effect and ultimately elevating DCR. Although the DCR of device D2 is higher than that of D3 and D4, its measured value remains at a low level. This low DCR is achieved through the implementation of a VGR structure. Specifically, the VGR extends the depletion region, which reduces the peak electric field at the edge of the depletion region. This suppression effectively reduces dark counts dominated by BTBT and the TAT effect. Additionally, the VGR serves as a physical barrier, preventing carriers generated by interface defects and dangling bonds at the STI interface from drifting into the avalanche region. As a result, it significantly lowers dark counts, primarily dominated by interface traps.

To elucidate the physical origin of dark counts, the activation energy (E_a) is extracted from the Arrhenius analysis. As illustrated in the inset of Fig. 6(b), within the high-temperature regime exceeding 323 K, the E_a of the device decreases from 1.25 eV to 0.96 eV with increasing V_{ex}. Notably, these values remain higher than half the silicon bandgap energy, suggesting that the DCR is predominantly governed by the Shockley–Read–Hall recombination mechanism in this regime. With decreasing temperature, a significant shift in the dominant generation mechanism is observed. At $V_{ex} = 1$ V, $E_a = 0.48$ eV, indicating a transition where TAT becomes the primary mechanism responsible for dark counts. Furthermore, E_a exhibits a gradual reduction as the applied V_{ex} is increased. This trend signifies the increasingly significant contribution of the TAT effect to the dark count generation process.

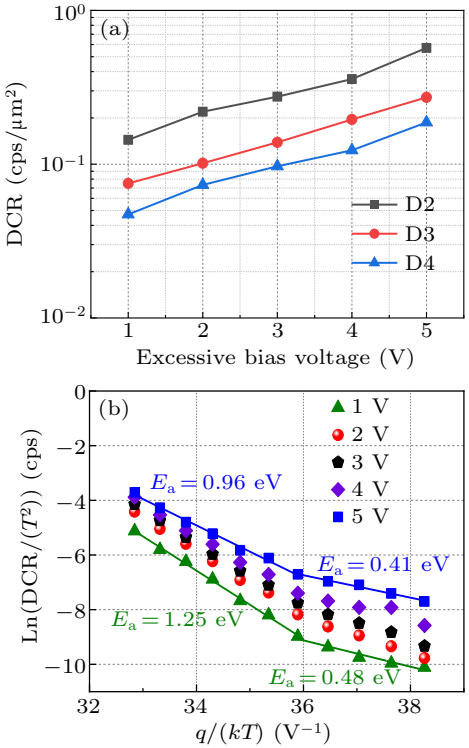


Fig. 6. (a) DCR versus excess bias voltage for devices D2, D3 and D4 at $T = 27$ °C. (b) The Arrhenius plot of the DCR of D2.

3.4. Afterpulsing probability

Afterpulsing in SPADs results from carrier trapping and subsequent re-emission at defect sites during the quenching-reset process, leading to secondary avalanches. Figure 7(a) displays the histogram of 50590 dark counts and its fitted curve for D2. An afterpulsing probability (AP) of 2.7% is obtained under $V_{ex} = 5$ V and a dead time of 700 ns, suggesting minimal defects in the multiplication region. As V_{ex} grows from 1 V to 5 V, the AP increases from 1.3% to 2.7%, which is because a stronger electric field enhances carrier kinetic energy and reduces the emission time constants of trapped carriers, thereby elevating the likelihood of secondary avalanche events.

3.5. Timing jitter

Measurement of timing jitter was performed using a 905 nm picosecond laser source with a pulse width of 30 ps and a repetition frequency of 31.25 kHz, along with a Taiko

MSO72504DX oscilloscope. Figure 7(b) shows the histogram timing distribution at $V_{ex} = 5$ V. The full-width at half-maximum (FWHM) of the timing jitter is 228 ps. The low timing jitter performance of the device is attributed to the strong lateral electric field distribution within the deep depletion region formed by the P-type/HVNW structure. Therefore, the vast majority of incident photons absorbed in the deep multiplication zone can trigger an avalanche. A few carriers generated in the P-type neutral layer enter the multiplication region through diffusion and drift and cause an avalanche pulse, ultimately manifesting as temporal dispersion in avalanche pulses. However, the use of an off-chip passive quenching scheme during timing jitter measurement, coupled with the inherent timing jitter of the laser itself, resulted in higher timing jitter for this device compared with other miniature devices.

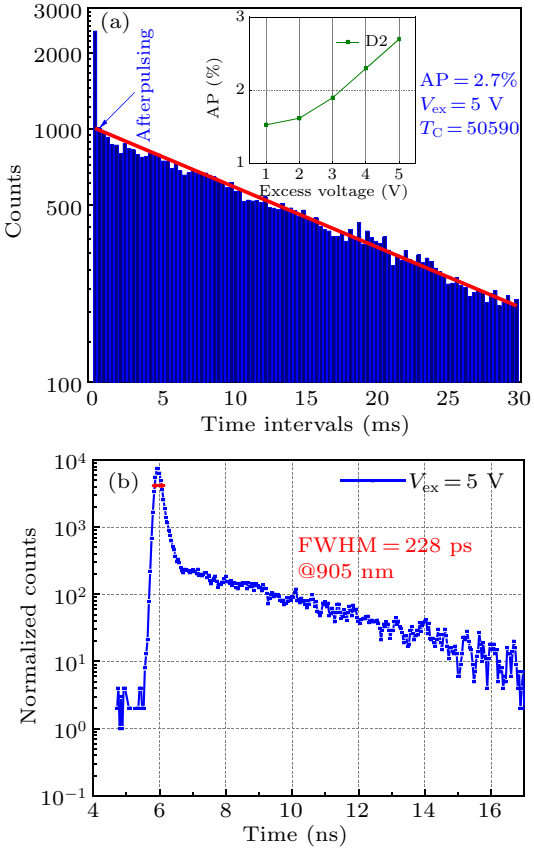


Fig. 7. (a) Inter-avalanche time histogram for D2 with a dead time of 700 ns at $V_{ex} = 5$ V and $T = 27$ °C. (b) Timing jitter results performed with a 905 nm laser.

4. Discussion

Table 1 summarizes the key performance metrics of recently reported devices. Reference [16] achieved reduced temporal jitter by optimizing the doping distribution between the main avalanche region and the deep PW layer, enabling a pitch size of 8.5 μm. However, the device exhibited suboptimal performance in both peak PDP and DCR. In Ref. [18], a pitch of 4 μm was enabled by exploiting the less-doped n-well region to surround the vertical PW/DNW multiplication region, but with a FF of only 17.7% and a notably high DCR of 73 cps·μm^{-2}. In Ref. [19], a retrograde doped and separated deep DNW combined with a junction-optimized p-well within the photosensitive region achieved an STI-free structure, significantly minimizing the DCR caused by the etching traps and surface states, and also obtaining a FF of 39%. Nevertheless, the device pitch remained relatively large, and the peak PDP was still low. Reference [20] utilized polysilicon to keep the STI oxide away from the active region and created a VGR through a retrograde DNW, achieving a device pitch of 10 μm and a FF of 35%, but its peak PDP remained suboptimal.

Table 1. Comparison of the latest silicon SAPDs.

References	[16]	[18]	[19]	[20]	This work
Process technology	55 nm COMS	65 nm CMOS	130 nm CMOS	110 nm CIS	180 nm BCD
PN junction	NW/PW	PW/DNW	PW/DNW	PW/DNW	P-implant/HVNW
Pitch (μm)	8.5	4	13	10	8.5
Active diameter (μm)	4.4	0.95	8	6	5
V_{BD} (V)	17.1	9.6	16.08	18.05	20.5
Fill factor (%)	21	17.7	39	35	31.5
Peak PDP (%@nm)	48.9@450	52@480	50.6@505	64@500	75.93@555
PDP@NIR (%@nm)	6.7@850	2.3@900	5.05@905	10@850	7.09@905
DCR (cps·μm^{-2}@V)	19.1@3	73@2.2	0.64@2	0.4@3	0.41@5
AP (%@V)	3.9@3	N/A	0.16@2	0.5@3	2.7@5
Jitter (ps@nm)	39@850	158@485	56@793	92@850	228@905

In contrast, the compact SPAD developed in this work demonstrates a peak PDP of 75.93% and a FF of 31.5%, while maintaining an ultra-low DCR of 0.41 cps·μm^{-2} — all achieved in a cost-effective 180 nm BCD process. Three key innovations contribute to these advancements. First, a P-type implantation/HVNW structure forms a deep and wide avalanche multiplication region, which significantly increases the photosensitivity, especially in the NIR band. Second, a strategically designed low-doped P-type epitaxial VGR synergistically suppresses edge breakdown while minimizing carrier generation–recombination losses. Third, the avalanche multiplication region adopts a chamfered-square geometric configuration with device cathodes positioned at the four chamfered corners, thus enhancing the FF without compro-

mising other performance metrics. This novel design approach effectively mitigates the performance degradation typically associated with device scaling.

5. Conclusion and perspectives

This work successfully demonstrates the fabrication of a compact SPAD device with concurrently high PDE and low DCR. The implementation of a P-type implantation/HVNW structure for the main multiplication region significantly enhances NIR PDP performance, while a lightly doped P-type epitaxial layer forms a deep VGR structure that effectively circumvents the performance limitations imposed by conventional GRW scaling. Combined with an innovative layout and design methodology to maximize the photosensitive area ratio, the device dimensions have been successfully reduced to 8.5 μm. Experimental results demonstrate that with a GRW of 0.7 μm, the device achieves a PDP of over 10% across a broad spectral range of 400–850 nm, exhibiting a peak PDE of 24% at a wavelength of 555 nm, while maintaining more than 7% effective PDP in the 905 nm NIR region. The optimized device shows controlled DCR below 0.41 cps·μm^{-2}, an AP of 2.7% and a timing jitter with a FWHM of 228 ps. The proposed SPAD design scheme overcomes conventional performance trade-off limitations, offering a highly competitive solution for high-density, low-cost integrated 3D imaging sensors.

Acknowledgements

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