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RAPID COMMUNICATION

Experimental demonstration and mechanism study of single-event gate leakage current in 4H-SiC power MOSFET with top oxide and double P-well structures

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This work proposes and fabricates the 4H-SiC power MOSFET with top oxide and double P-well (TODP-MOSFET) to enhance the single-event radiation tolerance of the gate oxide. Simulation results suggest that the proposed TODP structure reduces the peak electric field within the oxide and minimizes the sensitive region by more than 70% compared to C-MOSFETs. Experimental results show that the gate degradation voltage of the TODP-MOSFET is higher than that of the C-MOSFET, and the gate leakage current is reduced by 95% compared to the C-MOSFET under heavy-ion irradiation with a linear energy transfer (LET) value exceeding 75 MeV·cm^2/mg.

Keywords: silicon carbide, single-event leakage current (SELC), gate oxide, electric field, gate leakage current velocity

PACS: 77.55.dj, 43.72.+q, 43.38.Hz

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1. Introduction

Silicon carbide (SiC) power devices have excellent electrical and thermal properties, such as higher power density, higher thermal conductivity, and a wider operating temperature range than silicon-based devices. Therefore, SiC has great potential in aerospace and aviation power electronic applications.[1] Although SiC materials have strong radiation resistance, it has been found that SiC power devices are susceptible to heavy-ion irradiation, including leakage current degradation (SELC) and single-event burnout (SEB).[2–4] Moreover, single-event gate rupture (SEGR) and leakage current degradation at a lower bias voltage (lower than 10% of the rated voltage) have also been observed in SiC metal oxide semiconductor field effect transistors (MOSFETs),[5] which makes the gate oxide the weakest point limiting SiC aerospace applications.

Many researchers have investigated the single-event effects of SiC MOSFET gate oxide through experiments and simulations.[6–8] So far, SEGR and gate leakage current degradation are caused by gate oxide damage induced by heavy-ion irradiation, which is closely related to carrier accumulation in the JFET region.[9] Some researchers proposed that the transient high electric field in the gate oxide layer under irradiation is responsible for the gate leakage current in SiC MOSFETs. To reduce the electric field of the oxide, Jiang *et al.* proposed various buffer layer designs to reduce the peak electric field in planar MOSFETs.[10–12] Zhang *et al.*[13] proposed split-gate designs to suppress the influence of the parasitic transistor during single-event responses. However, most studies on single-event irradiation-hardened designs have focused on TACD-based numerical simulations. There are few studies on modulating the gate oxide electric field during heavy-ion irradiation, and they lack experimental validation.

To address these shortcomings, the 4H-SiC power MOSFET with top oxide and double P-well (TODP-MOSFET) is proposed and fabricated. Simulation results show that the electric field within the oxide of the TODP-MOSFET is reduced by about 79% compared to the C-MOSFET. Experimental results show that the gate leakage current is reduced by about 95% compared to the C-MOSFET. By sacrificing part of the on-resistance, the TODP-MOSFET demonstrates better SELC performance in the gate oxide than the C-MOSFET.

2. Device fabrication and mechanism

2.1. Device structure and fabrication

Figure 1 illustrates the schematic structures and the SEM cross-sectional views of the proposed TODP-MOSFET. Compared to the conventional 4H-SiC MOSFET (C-MOSFET), the TODP-MOSFET features a special top-oxide island design and a double P-well structure, which are intended to protect

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sensitive areas of the device, such as the junction field-effect transistor (JFET) region. The special top-oxide structure features an island-shaped counter top-oxide layer and a larger radius of curvature at the bottom corner, which helps reduce the transient electric field inside the oxide layer and minimize the sensitive volume of the device under single-event irradiation. In addition, the double P-well structure can shorten the hole collection path by adding an additional nested P-well layer based on the same channel design, significantly reducing carrier accumulation in the JFET region.

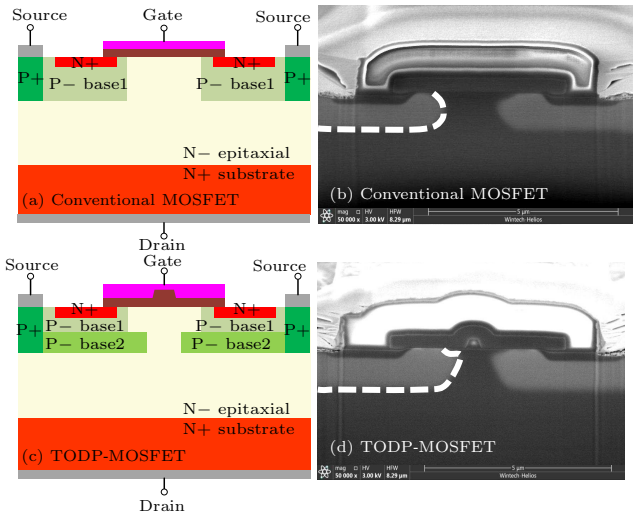


Fig. 1. Schematic structures and SEM cross-sectional views of the 4H-SiC C-MOSFET and the TODP-MOSFET.

The TODP-MOSFET was fabricated on an n-type SiC substrate with an epitaxial layer, where the thickness and doping concentration are 10 μm and 6×10^{15} cm^{-3}. The top-oxide island-shaped structure in this work was formed by the superposition of two gate oxide processes, which is approximately five times thicker than the conventional gate oxide thickness. The double P-well structure in this work was designed by Monte Carlo simulations and formed by multiple-energy Al^{+} implantation. To fabricate the double P-well structure in the proposed TODP-MOSFET, the first P-well was formed by three implantations at energies ranging from 150 keV to 350 keV, and the second P-well was offset from the first P-well by 0.6 μm, and was finally formed by independent implantations at energies ranging from 350 keV to 650 keV. The major structural parameters of the TODP-MOSFET are shown in Table 1.

Table 1. Structure parameters of TODP-MOSFET.

Structural parameter	Value for TODP-MOSFET
Epitaxial thickness	10 μm
Epitaxial doping	6×10^{15} cm^{-3}
Substrate doping	5×10^{18} cm^{-3}
Conventional oxide height	0.05 μm
Top oxide island height	0.25 μm
JFET length	2.2 μm

2.2. Device details and mechanism

To evaluate the heavy-ion radiation hardening performance of the proposed structure, the single-event performance of the TODP-MOSFET was simulated using the 2D Sentaurus simulator. The physics models used in this work are based on information from the published literature, including incomplete ionization, impact ionization, electrothermal coupling, and related effects.[14–16] The parameters of the single-event model in this work were set to be consistent with the actual experimental conditions (^{181}Ta at 1.6 GeV), corresponding to values ranging from 0.54 pC/μm to 0.59 pC/μm for the linear energy transfer (LET). The heavy-ion strike position was set at the center of the JFET region, which is the most sensitive area for SiC MOSFET gate oxides.

Figure 2 shows the transient electric field responses for the C-MOSFET and TODP-MOSFET at a reverse bias of 140 V. It can be seen from Fig. 2 that the maximum electric field of the C-MOSFET exceeds 22.3 MV/cm, which is likely the main cause of oxide damage and rupture during heavy-ion irradiation. The proposed TODP structure shifts the transient electric field along the heavy-ion track toward the corners of the top oxide, thereby moving the maximum electric field away from the most sensitive locations in the center of the JFET region. As shown in Fig. 2, the TODP structure reduces the peak electric field within the oxide to 18.4 MV/cm, which is about 18% smaller compared to the C-MOSFET. At the same time, the electric field at the most sensitive location within the oxide is reduced to 4.6 MV/cm, which is approximately 79% lower than that of the C-MOSFET.

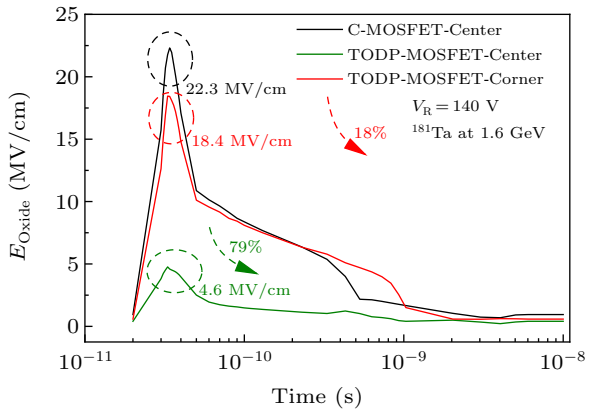


Fig. 2. Transient electric field in the oxide of the C-MOSFET and the TODP-MOSFET as a function of time under the same bias condition ($V_R = 140$ V).

To clarify the radiation hardening mechanism of TODP-MOSFET more clearly, Fig. 3 shows the surface plots of electric field distribution in the JFET region after the ion's strike at different times. At the beginning ($t = 0$ ps), the electric fields of the C-MOSFET and TODP-MOSFET are almost the same. After a heavy-ion strike ($t = 4$ ps), the electric field of the C-MOSFET reaches the maximum value, and the af-

fected region covers almost all the oxide above the JFET region, which are the oxide regions most sensitive to damage, as shown in Fig. 3(b). The TODP structure not only reduces the magnitude of the transient electric field in the oxide, but also effectively shrinks the range of sensitive regions during heavy-ion irradiation. The sensitive area of TODP-MOSFET is reduced by more than 70% compared to C-MOSFET, as shown in Fig. 3(f). After that, the electric field in the oxides of the two devices starts to decrease with time. The electric field peak and range of the TODP-MOSFET is consistently lower than that of the C-MOSFET, which is mainly because the proposed TODP structure effectively modulates excess carrier distribution within the JFET region.

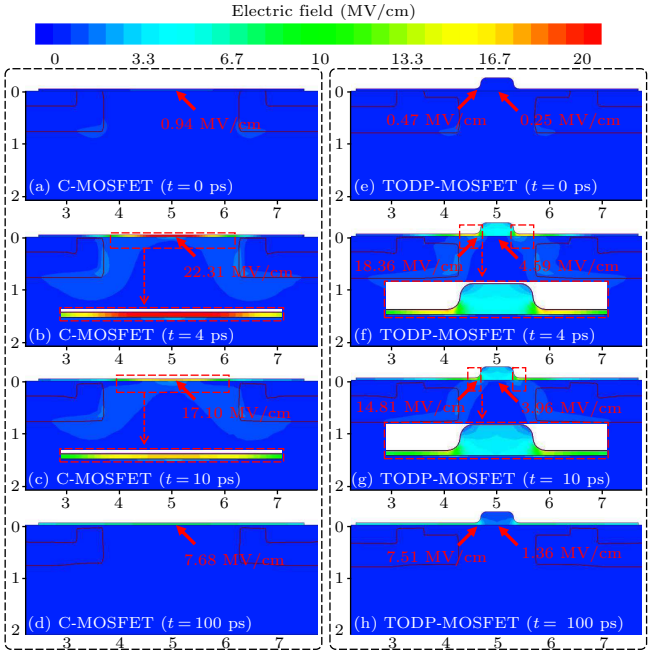


Fig. 3. The 2D surface plots of the electric field for the C-MOSFET and the TODP-MOSFET at $t = 0$ ps, 4 ps, 10 ps, and 100 ps, respectively. The insets show enlarged views of the electric field distribution in the oxide.

Figure 4 shows the profiles of internal hole density distributions in the C-MOSFET and TODP-MOSFET at 4 ps and 10 ps after the ion's strike. After a heavy-ion strike ($t =$ 4 ps), the distribution range of holes in the TODP-MOSFET is more dispersed, and the peak concentration of holes along the heavy-ion track is 3.12×10^{19} cm^{-3}, which is about 75% lower than that in the C-MOSFET. Meanwhile, the hole density away from the heavy-ion track is 1.47×10^{17} cm^{-3}, which is about twice that in the C-MOSFET, as shown in Fig. 4(b). This causes the holes in the TODP-MOSFET to be trapped and extracted by the double P-well structure more easily, thus weakening the hole accumulation in the JFET region. As a result, the excess holes in the TODP-MOSFET are extracted faster than in the C-MOSFET, which ultimately change the distribution of space charge in the JFET region.

In essence, the excess carriers accumulate at the interface, altering the distribution of internal space charge and ultimately inducing the high transient internal electric field. As the excess holes in the TODP-MOSFET are extracted more quickly over time, and less space charge accumulates within the JFET region compared to the C-MOSFET, as shown in Fig. 5. The space charge near the center of the oxide region can be reduced to 3.31×10^{19} cm^{-3}, which is about 74% smaller than that of the C-MOSFET. The space charge near the corner of the top oxide is reduced by about 48% compared to the C-MOSFET. It can be concluded that the space charge near the top oxide is reduced, while the space charge close to the double P-well is increased. This is due to the enhanced charge extraction capability in the TODP-MOSFET, which results in a narrower and lower distribution of the oxide electric field.

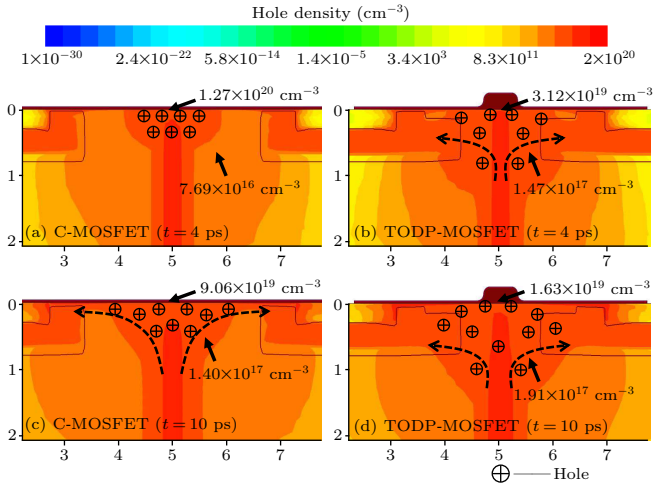


Fig. 4. The 2D surface plots of the internal hole density of the C-MOSFET and the TODP-MOSFET at $t = 4$ ps and $t = 10$ ps, respectively.

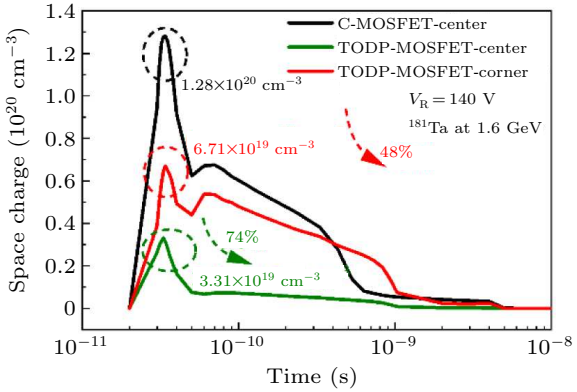


Fig. 5. The space charge near the oxide region of the C-MOSFET and the TODP-MOSFET as a function of time under the same bias condition ($V_R = 140$ V).

The heavy-ion irradiation experiments were performed at the Heavy Ion Research Facility in Lanzhou (HIRFL). The heavy ion used was ^{181}Ta at 1.6 GeV and possessed an LET greater than 75 MeV·cm^2/mg in 4H-SiC, which can cope with most radiation environments. All irradiation was performed at normal incidence and room temperature, and the devices under test were exposed to a flux of about 1×10^4 ions/(cm^2·s).

Figure 6(a) shows the real-time gate leakage current of the C-MOSFET and the TODP-MOSFET during irradiation, and

the corresponding gate leakage current velocities are shown in Fig. 6(b). The drain bias voltage ranges from 120 V to 280 V with 20 V increments. It can be seen that the single-event gate leakage current degradation voltages of the TODP-MOSFET are 140 V, which provides an improvement of 20 V compared to the C-MOSFET. In particular, under a drain bias voltage of 160 V, the TODP-MOSFET reduces the gate leakage current velocity from 48.5 nA/s to 2.3 nA/s, which is up to 95% slower than that of the C-MOSFET, as shown in Fig. 6(b). Therefore, the TODP-MOSFET exhibits a lower gate leakage current velocity than the C-MOSFET, which could be attributed to its smaller sensitive region.

Figure 7 compares the reverse and output characteristics of the TODP-MOSFET and the C-MOSFET before and after irradiation. It can be concluded that the reverse drain leakage current of both devices significantly increased after irradiation with ^{181}Ta at 1.6 GeV, but the TODP-MOSFET can still sustain a blocking voltage over 1600 V, whereas the blocking voltage of the C-MOSFET significantly degraded, demonstrating the radiation hardening performance of the proposed structure. Compared with the C-MOSFET, the output characteristics of the TODP-MOSFET are reduced, but the degradation after irradiation is smaller, as shown in Figs. 7(b) and 7(c). This is due to the presence of the double P-well structure resulting in a lower channel density, which inevitably increases the on-resistance of the device. Therefore, by sacrificing part of the on-resistance, the TODP-MOSFET achieves better SELC performance of the gate oxide than the C-MOSFET.

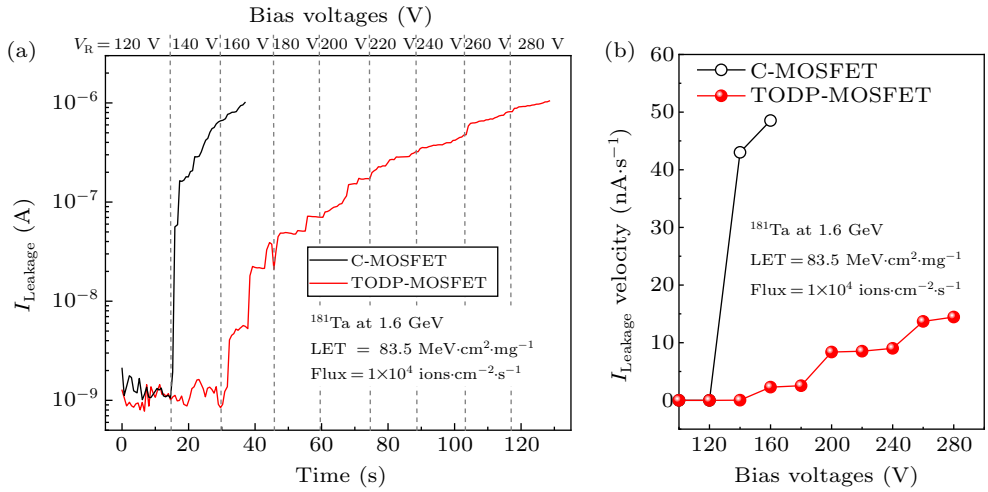


Fig. 6. Curves of the gate leakage current (a) and the gate leakage current velocity (b) of the C-MOSFET and the TODP-MOSFET during irradiation.

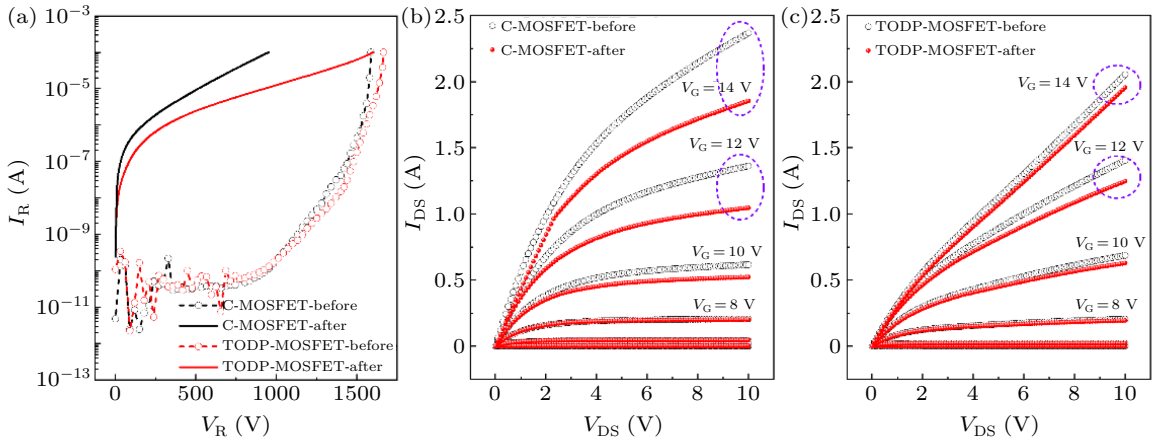


Fig. 7. The reverse and output characteristics of the TODP-MOSFET and the C-MOSFET before and after irradiation.

3. Conclusion

In this work, the TODP-MOSFET is proposed and fabricated to evaluate the single-event radiation performance of the gate oxide. The proposed TODP structure effectively reduces the peak electric field within the oxide and protects the most sensitive locations in the center of the JFET region. The sensitive area of the TODP-MOSFET is reduced by more than 70% compared to the C-MOSFET. The experiments show that the single-event gate leakage current degradation threshold of the TODP-MOSFET is higher than that of the C-MOSFET, and the TODP-MOSFET can reduce the gate leakage current velocity from 48.5 nA/s to 2.3 nA/s, which is up to 95% slower than that of the C-MOSFET. After irradia-

tion with ^{181}Ta at 1.6 GeV, the TODP-MOSFET still maintains its blocking and output characteristics. Therefore, the proposed TODP-MOSFET may provide an effective approach to improve the single-event radiation performance of SiC MOSFETs.

Acknowledgments

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