


# Memristor-based analog noise correction for infrared sensors

Xiao Huang(黄潇), Peiwen Tong(童霈文), Qingjiang Li(李清江), Tuo Ma(马拓), Shuo Han(韩硕), Wei Wang(王伟), and Yi Sun(孙毅)

**Citation:**Chin. Phys. B, 2026, 35 (**2**): 028501. DOI: 10.1088/1674-1056/adecf9
http://cpb.iphy.ac.cn; http://iopscience.iop.org/cpb

**What follows is a list of articles you may be interested in**

---

## High throughput *N*-modular redundancy for error correction design of memristive stateful logic

Xi Zhu(朱熙), Hui Xu(徐晖), Weiping Yang(杨为平), Zhiwei Li(李智炜), Haijun Liu(刘海军), Sen Liu(刘森), Yinan Wang(王义楠), and Hongchang Long(龙泓昌)

Chin. Phys. B, 2023, 32 (**1**): 018502. DOI: 10.1088/1674-1056/ac8f38

## Universal memory based on phase-change materials: From phase-change random access memory to optoelectronic hybrid storage

Bo Liu(刘波), Tao Wei(魏涛), Jing Hu(胡敬), Wanfei Li(李宛飞), Yun Ling(凌云), Qianqian Liu(刘倩倩), Miao Cheng(程淼), and Zhitang Song(宋志棠)

Chin. Phys. B, 2021, 30 (**5**): 058504. DOI: 10.1088/1674-1056/abeedf

## Recent progress in optoelectronic neuromorphic devices

Yan-Bo Guo(郭延博), Li-Qiang Zhu(竺立强)

Chin. Phys. B, 2020, 29 (**7**): 078502. DOI: 10.1088/1674-1056/ab99b6

## A method of generating random bits by using electronic bipolar memristor

Bin-Bin Yang(杨彬彬), Nuo Xu(许诺), Er-Rui Zhou(周二瑞), Zhi-Wei Li(李智炜), Cheng Li(李成), Pin-Yun Yi(易品筠), Liang Fang(方粮)

Chin. Phys. B, 2020, 29 (**4**): 048505. DOI: 10.1088/1674-1056/ab77fd

## Memristor-based vector neural network architecture

Hai-Jun Liu(刘海军), Chang-Lin Chen(陈长林), Xi Zhu(朱熙), Sheng-Yang Sun(孙盛阳), Qing-Jiang Li(李清江), Zhi-Wei Li(李智炜)

Chin. Phys. B, 2020, 29 (**2**): 028502. DOI: 10.1088/1674-1056/ab65b5

---

# Memristor-based analog noise correction for infrared sensors

Xiao Huang(黄潇)[†], Peiwen Tong(童霈文)[†], Qingjiang Li(李清江), Tuo Ma(马拓), Shuo Han(韩硕), Wei Wang(王伟)[‡], and Yi Sun(孙毅)[§]

*College of Electronic Science and Technology, National University of Defense Technology, Changsha* 410073, *China*

(Received 15 April 2025; revised manuscript received 12 June 2025; accepted manuscript online 8 July 2025)

Sensor noise is a critical factor that degrades the performance of image processing systems. In traditional computing systems, noise correction is implemented in the digital domain, resulting in redundant latency and power consumption overhead in the analog-to-digital conversion. In this work, we propose an analog-domain image correction architecture based on a proposed small-scale UNet, which implements a compact noise correction network within a one-transistor-one-memristor (1T1R) array. The statistical non-idealities of the fabricated 1T1R array (e.g., device variability) are rigorously incorporated into the network's training and inference simulations. This correction network architecture leverages memristors for conducting multiply-accumulate operations aimed at rectifying non-uniform noise, defective pixels (stuck-at-bright/dark), and exposure mismatch. Compared to systems without correction, the proposed architecture achieves up to 50.13% improvement in recognition accuracy while demonstrating robust tolerance to memristor device-level errors. The proposed system achieves a 2.13-fold latency reduction and three orders of magnitude higher energy efficiency compared to conventional architecture. This work establishes a new paradigm for advancing the development of low-power, low-latency, and high-precision image processing systems.

**Keywords:** infrared sensor noise, memristor, analog-domain neuromorphic computing, correction network, one-transistor-one-memristor (1T1R) array

**PACS:** 85.35.–p, 84.37.+q, 07.05.Mh, 31.30.–i

**DOI:** 10.1088/1674-1056/adecf9 **CSTR:** 32038.14.CPB.adecf9

## 1. Introduction

With the increasing scale of sensor arrays, sensor noise emerges as a critical factor that significantly impacts the performance of image acquisition and processing systems.[1,2] As the number of integrated sensors continues to grow and the pixel unit area shrinks, these noise sources exert an increasingly pronounced effect on both the quality of image sensors and the processing capabilities of image processing systems, which underscores the urgent need for advanced image correction techniques.

In-memory computing in or near the sensor affords a time-efficient and energy-efficient solution for image processing system, which simulates the human visual system.[3–8] The in-memory computing system does not need to convert the data from the analog domain to the digital domain, which reduces the power consumption and processing latency of the system. Traditional noise correction circuits are affected by high energy consumption and large latency resulting from the A/D conversion process and the separation of memory and computing units.[9–12] Therefore, there is a pressing need for an architecture for image noise correction in analog domain based on the in-memory computing system, reducing both latency and power consumption during image transmission.

The advent of memristor-based image processing systems has provided unprecedented opportunities for high-efficiency and biologically plausible computation. Memristors, leveraging their excellent properties, such as tunable switching dynamics, exceptional retention capabilities, quasi-linear current–voltage relationships, and intrinsic biomimetic characteristics, have been harnessed to enable analog-domain image processing.[13,14] These intrinsic characteristics not only exhibit fundamental compatibility with neuromorphic computing architectures through their synaptic-like dynamics, but also effectively address the inherent limitations of von Neumann-based digital systems in distributed signal processing.

Here, we propose a memristor-based infrared sensor noise correction scheme. This scheme performs noise correction in the analog domain, with the aim of improving the accuracy of in-memory computing systems. The benefits of this approach include low power consumption and reduced latency. The proposed architecture directly processes analog signals through a one-transistor-one-memristor (1T1R) crossbar array for real-time noise suppression, followed by immediate pattern recognition via memristor-based neural networks, eliminating analog-to-digital conversion requirements. Experimental results demonstrate a 78.63% improvement in peak signal-to-noise ratio (PSNR) compared to uncorrected systems. No-

[†]These authors contributed equally to this work.
[‡]Corresponding author. E-mail: wangwei_esss@nudt.edu.cn
[§]Corresponding author. E-mail: sunyi12@nudt.edu.cn

© 2026 Chinese Physical Society and IOP Publishing Ltd. All rights, including for text and data mining, AI training, and similar technologies, are reserved.

tably, the correction network exhibits strong tolerance to device variations, with only 5.01% PSNR degradation under ±5% memristor conductance fluctuations. Upon integrating the recognition network, it becomes evident that the inclusion of a correction network markedly enhances the recognition accuracy to 97%, representing a substantial enhancement. This noise correction and computation paradigm provides a novel hardware solution for high-precision infrared image processing with sub-millisecond latency and microwatt-level power consumption.

## 2. In-memory computing system with correction network based on memristor arrays

### 2.1. Analog noise correction based on memristor arrays

Figure 1(a) illustrates a traditional image processing system with analog-to-digital conversion and separate storage and computing architecture, which causes high latency and power consumption. The system we propose is shown in Fig. 1(b), which incorporates both noise correction and image recognition processes within a memristor array. Multiply-accumulate (MAC) operations constitute the computational core of noise correction algorithms due to their intensive arithmetic requirements. Memristor crossbar arrays present a transformative approach by enabling analog-domain parallel MAC computations through intrinsic physical laws (e.g., Ohm's law for multiplication and Kirchhoff's law for summation). The system depicted in Fig. 1(b) converts the analog current signal obtained from the sensor array into a voltage signal using TIAs. This voltage signal is then utilized as the input for the noise-correction memristor array where MAC operations are executed. The resulting current vector is later transformed into voltage signals through TIAs, serving as the input excitation for the subsequent memristor array for recognition. Following the second computation within the memristor array, the final recognition outcome can be obtained. This paradigm inherently bypasses the von Neumann bottleneck caused by data shuttling between separated memory and processing units, while eliminating latency and energy overheads from repeated analog-to-digital (A/D) conversions, helping to improve the latency, power consumption, and scalability of applications. However, noise correction in memristor arrays is based on the characteristics of memristors or convolutional filtering, and complex noise cannot be processed. Therefore, a high-performance noise correction neural network that can adapt to practical memristor arrays and meet the high requirements of infrared sensor noise correction is of great significance.

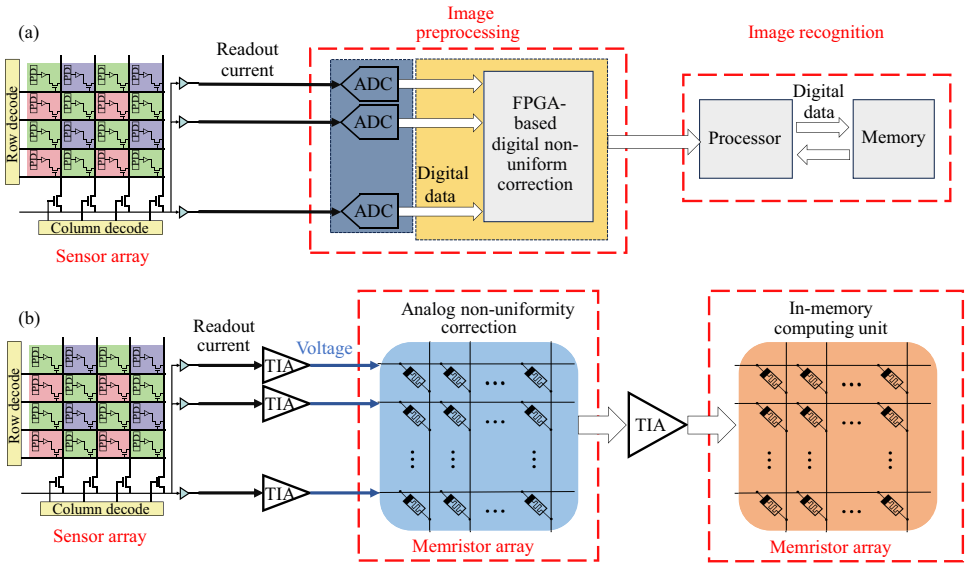



**Fig. 1.** Schematic diagrams of image processing system. (a) Traditional analog-digital hybrid architecture. (b) Analog-domain image processing architecture based on memristor arrays.

### 2.2. Device characterization and analysis

To make the experimental results more realistic, the electrical characteristics of the memristor are tested. A statistical analysis of weight modulation programming errors is conducted, and experimental data characterizing weight fluctuations are presented to validate the subsequent performance simulations.

The TiN/HfO$_x$/TaO$_x$/TiN 1T1R arrays are fabricated for tests. The electrical characteristics of the memristors are characterized using a Keithley 4200-SCS semiconductor parameter analyzer. All measurements are automated via the Keithley Interactive Test Environment (KITE) software.

The device structure is shown in the inset of Fig. 2(a), and the typical $I$–$V$ characteristics of a 1T1R memristor are shown in Fig. 2(a). The DC characterization of the 1T1R device is performed by applying a direct current voltage (DC voltage) to the gate terminal. The Set operation involves applying an electrical excitation voltage between 0 V and 0.9 V across the B-terminal in a bipolar electrode configuration. When the ex-

citation voltage exceeds the threshold voltage, the device transitions from high resistance to low resistance. On contrast, the Reset operation involves applying an electrical excitation voltage between 0 V and 1.3 V across the S-terminal. When the excitation voltage is greater than the threshold voltage, the device changes from low resistance to high resistance. In order to better display the DC characteristics of the device, we apply the Set voltage and Reset voltage 100 times in cycles, and continuously read the *I*–*V* characteristic curve, which supports the continuous modulation of the device conductance and great uniformity of the device. Figure 2(b) illustrates the progressive conductance modulation of the 1T1R cell under pulsed voltage stimulation, capturing two complete Set–Reset operational cycles, in which the red curve indicates the Reset operation and the blue curve indicates the Set operation. The curves illustrate that there are multiple tunable resistive states of the device, which provides the basis of accurate mapping of the network weights.

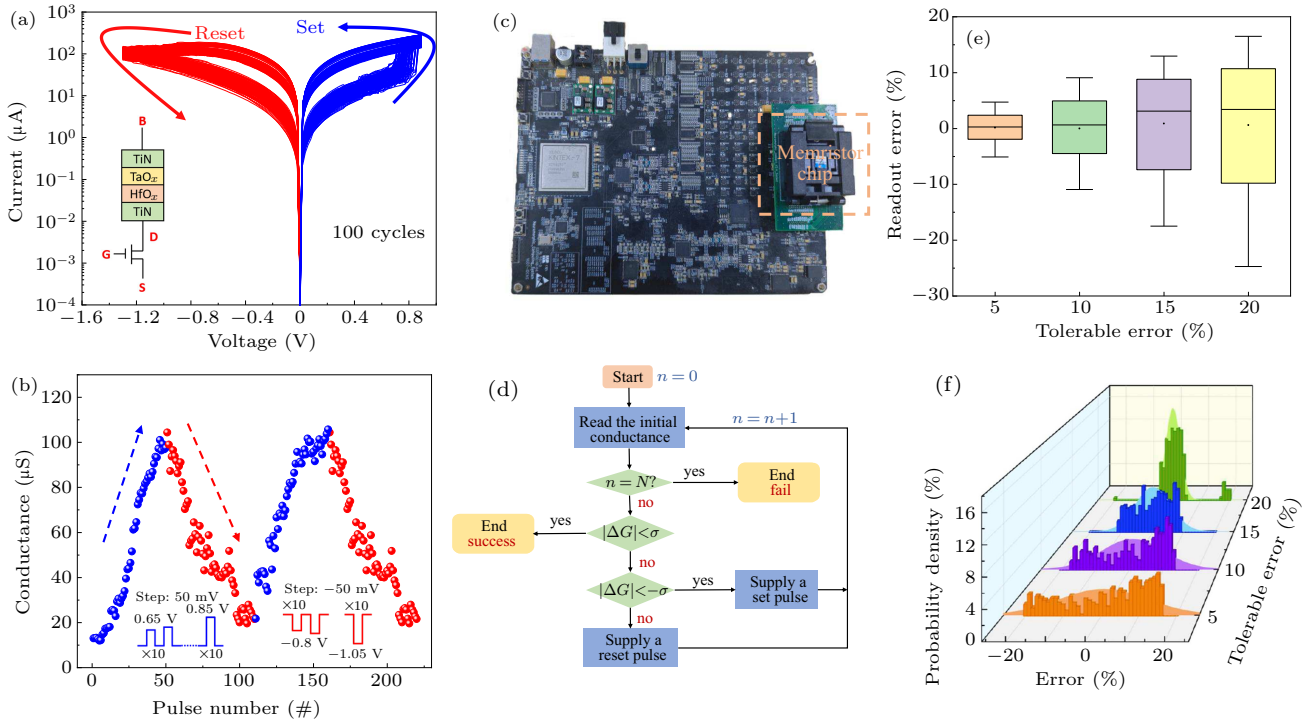



**Fig. 2.** (a) 100 cycles *V*–*I* curves of 1T1R unit. (b) 1T1R unit pulse modulation characteristics. (c) Composition of the 1T1Rchip board-level verification system. (d) Flow chart of memristor weight modulation. (e) Statistical distribution of the weight modulation error under different tolerable errors. (f) The histograms of the weight modulation error under different tolerable errors and fitting curve of Gaussian distribution.

We systematically analyze the programming error characteristics of memristor devices during the weight writing process using a board-level verification system based on 1T1R array architecture, as shown in Fig. 2(c). A closed-loop feedback control strategy, as depicted in Fig. 2(d), is employed to achieve precise programming regulation of memristor conductance. Real-time monitoring of the instantaneous conductance error $\Delta G = (G_{\text{target}} - G_{\text{measured}})/G_{\text{target}}$ was conducted before each programming operation, where $G_{\text{target}}$ represents the target conductance and $G_{\text{measured}}$ is the actual measured conductance. If $\Delta G$ exceeds the preset tolerance threshold $\sigma$, the system activates a dynamic adjustment mechanism: for $\Delta G > \sigma$, optimally designed voltage pulse sequences are applied to the B electrode to induce Set operation, leading to a gradual increase in conductance by forming a conductive filament; for $\Delta G < -\sigma$, a voltage pulse with specific parameters is applied to the S electrode to trigger Reset operation, resulting in a precise downward adjustment of conductance by partially dissolving conductive filaments. When the system detects $|\Delta G| < \sigma$, it confirms that the current programming operation meets the predetermined accuracy requirement, and the operation is stopped.

To assess the relationship between programming accuracy and tolerance threshold, we conduct comparative experiments with four gradient tolerance thresholds (5%, 10%, 15%, and 20%). Figure 2(e) displays the statistical distribution of memristor resistance write errors under different tolerance conditions. Upon Gaussian fitting, the experimental data exhibit a typical normal distribution pattern, as shown in Fig. 2(f). This finding furnishes dependable data on device non-ideal characteristics for memristor-based neuromorphic computing systems, offering valuable guidance for subsequent circuit simulations and system optimizations.

## 3. The correction network structure and performance simulation

### 3.1. Small-scale UNet and memristor mapping scheme

In order to realize a full analog-domain image processing system, the network is need to be mapped in the memris-

tor arrays, which place demands on the scale of the network. The U-Net network is a type of lightweight fully convolutional network, and its operations can all be decomposed into multiply-accumulate operations which can be implemented in memristor arrays.[15] The U-Net is restructured and dynamically adjusted to the small-scale UNet. The visual description of the network model is shown in Fig. 3(a), where the input is a noisy image. The small-scale U-Net architecture is composed of two primary components: an encoder and a decoder. The encoder module is designed to capture the feature information of input image, while the decoder module is responsible for reconstructing the fine details of the image. The architecture of UNet is instrumental in noise reduction while preserving the size and informational elements of the image. Additionally, the concatenation operation in U-Net links the high-resolution features from the encoder to the corresponding layers in the decoder, which is beneficial to restore the details and edge information in the output image.

The encoder in this small-scale UNet employs a single contracting stage to balance feature abstraction and computational efficiency. The contracting stage is consisted of the repeated application of two $3\times3$ convolutions (unpadded convolutions), each followed by a rectified linear unit (RELU) and a $2\times2$ max-pooling operation with stride 2 for downsampling, which achieves 75% parameter reduction compared to standard 4-stage UNet encoders. By compressing the layered architecture of the network, the small-scale UNet effectively compresses the number of parameters and calculations required for inference operations while maintaining the necessary receptive field growth ($5\times5$ effective kernel coverage via sequential convolutions).

The decoder in this small-scale UNet architecture employs a symmetric single expansive stage to restore spatial fidelity while strictly maintaining parameter efficiency. Utilizing a $2\times2$ transposed convolutional layer with stride 2 for upsampling, it concatenates the upscaled features (8 channels) with skip-connected high-resolution encoder outputs (4 channels) through channel-wise fusion, followed by two $3\times3$ convolutions with ReLU to refine features. Mirroring the encoder's compressed hierarchy, the decoder enables noise correction, establishing an optimal balance between compactness and performance.

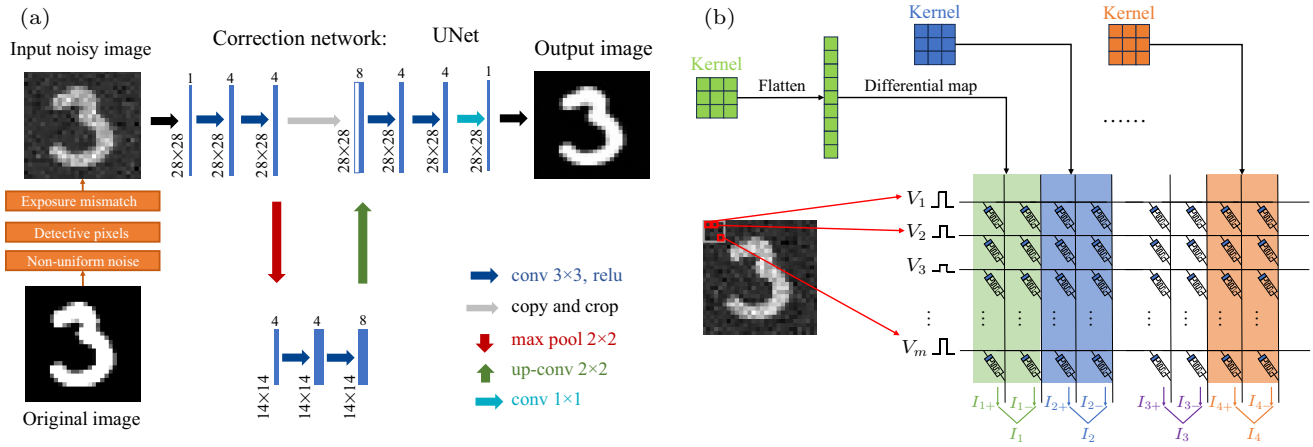



**Fig. 3.** Structure of the small-scale UNet network for noise correction. It mainly consists of an encoder (the left part of the net) and a decoder (the right part of the net). (b) The mapping scheme of convolution process.

To achieve the small-scale UNet by memristor, it is necessary to propose the network mapping strategy. The network mapping consists of two parts: weight mapping and input data mapping. After the network model parameters are obtained from offline network training, the parameters in the network model are mapped to the memristor array, as shown in Fig. 3(a). Since the weights can be either positive or negative, a kernel weight should be mapped to two adjacent columns within the memristor crossbar array. This dual-column mapping strategy enables differential readout operations, the mapping formula for the conductance value are as follows:

$$G_{i+} = S^{+} \times \left|\frac{a_i}{|a_{\max}|}\right| \times (G_{\max} - G_{\min}) + G_{\min}, \tag{1}$$

$$G_{i-} = S^{-} \times \left|\frac{a_i}{|a_{\max}|}\right| \times (G_{\max} - G_{\min}) + G_{\min}, \tag{2}$$

$$\begin{cases} S^{+} = 0 \ \text{ and } \ S^{-} = 1, \ a_i \le 0, \\ S^{+} = 1 \ \text{ and } \ S^{-} = 0, \ a_i \ge 0, \end{cases} \tag{3}$$

where the $G_{i+}$ is the conductance of the positive column, $G_{i-}$ is the conductance of the negative column, $a_i$ is the weight, $a_{\max}$ is the maximum of the wights, and $G_{\min}$ and $G_{\max}$ are respectively the minimum and the maximum of the memristor conductance. The input value is encoded by the pulse amplitude, and the formula is as follows:

$$V_{\text{in}} = \frac{(x_{\text{in}} - x_{\min})}{(x_{\max} - x_{\min})} \times (V_{\max} - V_{\min}) + V_{\min}, \tag{4}$$

where $x_{\text{in}}$ is the input value, $x_{\max}$ and $x_{\min}$ are respectively the maximum and the minimum of the input values, and $V_{\max}$ and

$V_{\min}$ are respectively the maximum and the minimum of the input voltages. Then we can calculate the output current

$$I_n = \sum_{m=1}^{i} V_m \times G_{nm}^{+} - \sum_{m=1}^{i} V_m \times G_{nm}^{-}. \tag{5}$$

In this manner, distinct kernel-weight combinations are allocated to separate differential column pairs of the memristor array, while the memristor array simultaneously performs multiply-accumulate operations across shared input signals through parallel computation.

### 3.2. Infrared sensor noise model

To train the correction network, we should first define the noise model of the infrared sensor. This sensor converts infrared light into electrical signals, with the output signal strength being directly proportional to the incident light intensity. The device's noise characteristics primarily include non-uniformity noise, defective pixels, and exposure synchronization errors, as shown in Fig. 4(a).

Non-uniform noise primarily includes photon shot noise, read noise, and row noise. The noisy image can be represented by the following formula:[16]

$$D = \text{image} + N_{\text{P}} \times K_{\text{a}} \times K_{\text{d}} + N_{\text{row}} \times K_{\text{d}} + N_{\text{read}} \times K_{\text{d}}, \tag{6}$$

where $D$ is the grayscale value of the sensor output image, $K_{\text{a}}$ is the sensor analog gain, $K_{\text{d}}$ is the sensor digital gain, image is the ideal grayscale value, $N_{\text{P}}$ represents photon shot noise, $N_{\text{read}}$ denotes read noise, and $N_{\text{row}}$ indicates row noise. The quantum nature of light introduces statistical uncertainty in the number of photons collected by the sensor photosensitive elements, which follows a Poisson distribution

$$\left(\frac{\text{image}}{K_{\text{a}} \times K_{\text{d}}} + N_{\text{P}}\right) \sim P\left(\frac{\text{image}}{K_{\text{a}} \times K_{\text{d}}}\right), \tag{7}$$

where $P$ denotes a Poisson distribution. Read noise includes dark current shot noise, dark current fixed-pattern noise, reset noise, and source follower noise. This type of noise conforms to the heavy-tailed Tukey lambda distribution

$$N_{\text{read}} \sim T(\lambda; \mu_{\text{c}}, \sigma_{\text{TL}}), \tag{8}$$

where $T$ represents a Tukey lambda distribution, $\lambda$ and $\sigma$ are the shape and scale parameters of the read noise distribution, respectively, and $\mu_{\text{c}}$ is the DC noise component. Row noise follows a Gaussian distribution, where $\sigma_{\text{r}}$ is the scale parameter of the Gaussian distribution

$$N_{\text{row}} \sim N(0, \sigma_{\text{r}}). \tag{9}$$

We refer to the parameter calibration values from the literature,[16] as listed in the following Table 1.

**Table 1.** The calibration values of the non-uniform noise model.

| Model parameter | Calibrated value |
|---|---|
| $K_{\text{a}}$ | 1.4 |
| $K_{\text{d}}$ | 4 |
| $\mu_{\text{c}}$ | 101.318 |
| $\lambda$ | –0.164 |
| $\sigma_{\text{TL}}$ | 2.126 |
| $\sigma_{\text{r}}$ | 0.2 |

Since the parameters lack specific physical meanings, the magnitude of non-uniformity noise is quantified using the mean squared error (MSE). The formula for MSE is given by

$$\text{MSE} = \frac{1}{n}\sum_{i=1}^{n}(y_i - \widehat{y}_i)^2, \tag{10}$$

where $\widehat{y}_i$ represents the pixel value of the actual image, and $y_i$ denotes the pixel value of the ideal image.

Defective pixels are another critical factor contributing to sensor noise, quantified by the yield rate $y$, where a proportion $(1-y)$ of the sensor units in the array are defective and fail to respond to changes in infrared intensity. These defective pixels manifest in two forms: stuck-at-bright pixels, which are permanently fixed at the maximum value (e.g., pixel value = 1), and stuck-at-dark pixels, which remain fixed at the minimum value (e.g., pixel value = 0). Due to manufacturing process limitations, all defective pixels within the same sensor array are uniformly either stuck-at-bright or stuck-at-dark, rather than a mixture of both types.

The third type of noise is exposure mismatch, where the sensor's output is significantly influenced by external lighting conditions. The received image signal becomes a superposition of the ideal image signal and the external illumination, leading to over-exposed or under-exposed scenarios. These effects are mathematically expressed as

$$\text{noisy_image} = \text{clamp}(\text{image} + l, 0, 255), \tag{11}$$

$$\text{noisy_image} = \text{clamp}(\text{image} - l, 0, 255), \tag{12}$$

$$\text{clamp}(x, a, b) = \begin{cases} a, x < a, \\ x, a \le x \le b, \\ b, x > b. \end{cases} \tag{13}$$

Here, noisy_image represents the output image under over- or under-exposure conditions, and l denotes the pixel value shift caused by the exposure mismatch. This noise type directly alters pixel intensities in a uniform manner across the image, depending on the lighting environment.

### 3.3. Noise correction network performance simulation

To verify the performance of noise correction network achieved by small-scale UNet with limited scale, we compare the image quality before and after the noise correction network. Here, we use the peak signal-to-noise ratio (PSNR) to measure image quality. The formula for PSNR is

$$\text{PSNR} = 10 \cdot \log_{10}\left(\frac{\text{MAX}_I^2}{\text{MSE}}\right), \tag{14}$$

where $MAX_I$ is the maximum possible pixel value, and MSE is the mean squared error between the actual and ideal images, as defined previously.

The dataset is generated by introducing three types (non-uniform noise, defective pixels and exposure mismatch) of noise simultaneously to an ideal image, following the noise model detailed in Subsection 3.2, depicted in Fig. 3(a). To enhance the ability of the trained network to effectively correct various types of noise with varying intensities, we conducted preliminary evaluations on the training datasets with diverse parameters. The experimental results indicate that under the parameter configuration of non-uniform noise ($\mu_c = 15$), yield rate (90%), and exposure mismatch (50 units), the system demonstrates optimal average recognition performance across heterogeneous noise types. Consequently, this subset is selected as the training set.

Figure 4(a) presents a comparative analysis of four image conditions: the original reference image, nonuniform noise contamination, defective pixel artifacts, and exposure mismatch. The figure demonstrates that these three kinds of noise collectively induce significant edge blurring and structural ambiguity in numeric regions, severely compromising machine readability. This empirical evidence substantiates the requirement for an adaptive correction framework to address the compound degradation effects through targeted noise suppression and feature reconstruction.

Figures 4(b)–4(e) present comparative statistical box plots analyzing the variations in peak signal-to-noise ratio (PSNR) metrics between original and corrected image outputs. Each experimental configuration was subjected to 100 independent trials, with the red schematic elements (boxes and whiskers) representing the enhanced results through our correction network implementation, while blue counterparts indicate baseline performance without correction. In Fig. 4(b), the graph displays the PSNR when exclusively non-uniform noise is introduced. Following correction network, a substantial and consistent enhancement in image PSNR is observed. Figure 4(c) depicts the PSNR trend with respect to yield when the defective element is set at dark. There is an improvement in image PSNR after correction network; however, a decline is noted with decreasing yield. Figure 4(d) illustrates the relationship between PSNR and yield when the defective element is fixed at bright, revealing that the PSNR of the corrected image remains consistently high. Figure 4(e) showcases the impact of exposure mismatch on image PSNR, where negative values on the horizontal axis signify underexposure, positive values denote overexposure. PSNR rises after the correction network, yet diminishes with increasing overexposure and underexposure values. When the exposure is set to , the image is expected to be identical to the original image. However, in the depicted scenario, the PSNR is not maximized. This discrepancy arises because, theoretically, if the MSE is reduced to 0, the PSNR would approach positive infinity according to the PSNR formula. This outcome is mathematically undefined. To address this issue, a ground noise is introduced to the image, specifically non-uniform noise when the parameter $\mu_c$ is designated as 0. This adjustment aligns with the data and rationalizes the observed phenomenon where the PSNR is not maximum when the exposure level is set to in the image.

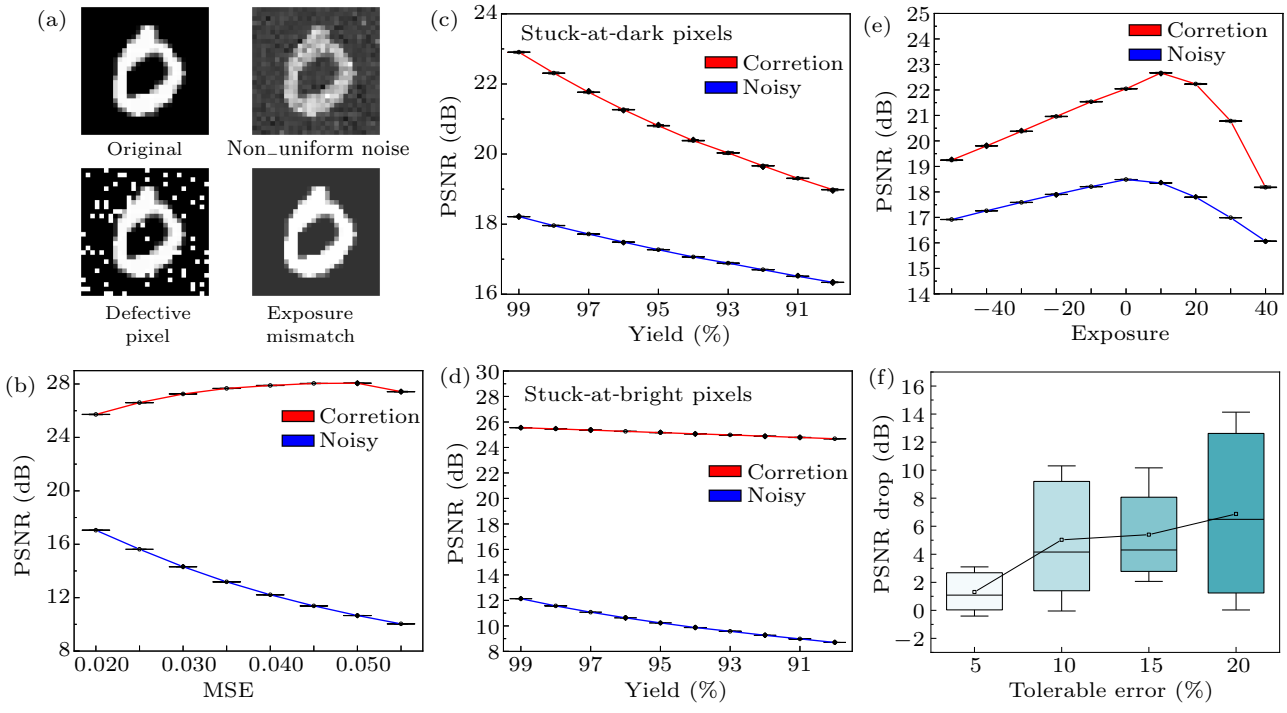



**Fig. 4.** (a) The effect of three kinds of infrared sensor noise. (b)–(e) PSNRs of the pictures before and after correction network under 100 experiments. Red boxes represent the results with correction network, blue boxes represent the results without correction network. (f) The effect of memristor tolerance error on the PSNR of the pictures.

To evaluate network robustness, we incorporated statistics for the practical weight modulation errors under different tolerable errors into the network. Owing to stochastic resistance variations inn devices, programmed weight values exhibit inherent errors during repeated writing operations. This is the tolerable error of the memristor, as depicted in Fig. 2(f), is quantified through Gaussian fitting. This error is represented by a Gaussian distribution function: $r = N(\mu, \sigma)$, with $\mu$ and $\sigma$ derived from the fitting outcomes. Incorporating this tolerable error into the weight $G$ in the correction network yields the adjusted weight $G'$, which is defined as: $G' = G(1 + r)$. The results under realistic non-uniformity memristor conditions are shown in Fig. 5(f). In practical applications, the allowable tolerance of memristors is typically within 5%. Under this 5% tolerance threshold, the reconstructed image exhibits only a 5.01% decrease in PSNR, demonstrating that the noise correction network retains robust performance even within the permissible error range.

To evaluate the holistic recognition efficacy of the image processing system enhanced by the compensation network, we integrated the proposed compensation module (see system architecture in Fig. 5(a)). The system combines a recognition network (a 784-500-10 MLP) and a correction network. Comparative experiments between the baseline (without compensation) and the compensated system demonstrate the latter's superior recognition accuracy, validating the module's role in improving robustness against noise-induced distortions.

Figures 5(b)–5(e) illustrate the system recognition rates before and after correction under varying noise levels for non-uniform noise, stuck-at-bright pixels, stuck-at-dark pixels, exposure mismatch, respectively. For each parameter configuration, 100 experimental trials were conducted, with the results visualized as box plots: red boxes represent the recognition rates with the correction network, while blue boxes denote the baseline system without correction. In Fig. 5(e), it is observed that a negative exposure does not significantly reduce the recognition rate, a phenomenon that may appear counterintuitive. Nonetheless, our experimental findings indicate that under-exposure accentuates the edges of numbers in images, a crucial image feature. Preserving this feature sustains the network's recognition accuracy at a high level. As depicted in the figures, the system integrated with the correction network exhibits significant improvements in recognition accuracy, achieving a maximum enhancement of 50.13%.

Figure 5(f) quantitatively characterizes the degradation pattern of recognition accuracy under different tolerable errors. The experimental data reveal that introducing ±5% operational tolerance thresholds (simulating non-ideal memristive device characteristics in analog crossbar arrays) induces only marginal performance degradation, with a statistically insignificant reduction of 6.67% compared to ideal hardware assumptions. This empirical evidence substantiates the neural network architecture's inherent error resilience when interfacing with emerging analog computing architectures, particularly in correcting the intrinsic non-idealities of memristor-based hardware implementations. This robust performance underscores the correction network's effectiveness in mitigating sensor noise within the image processing pipeline.

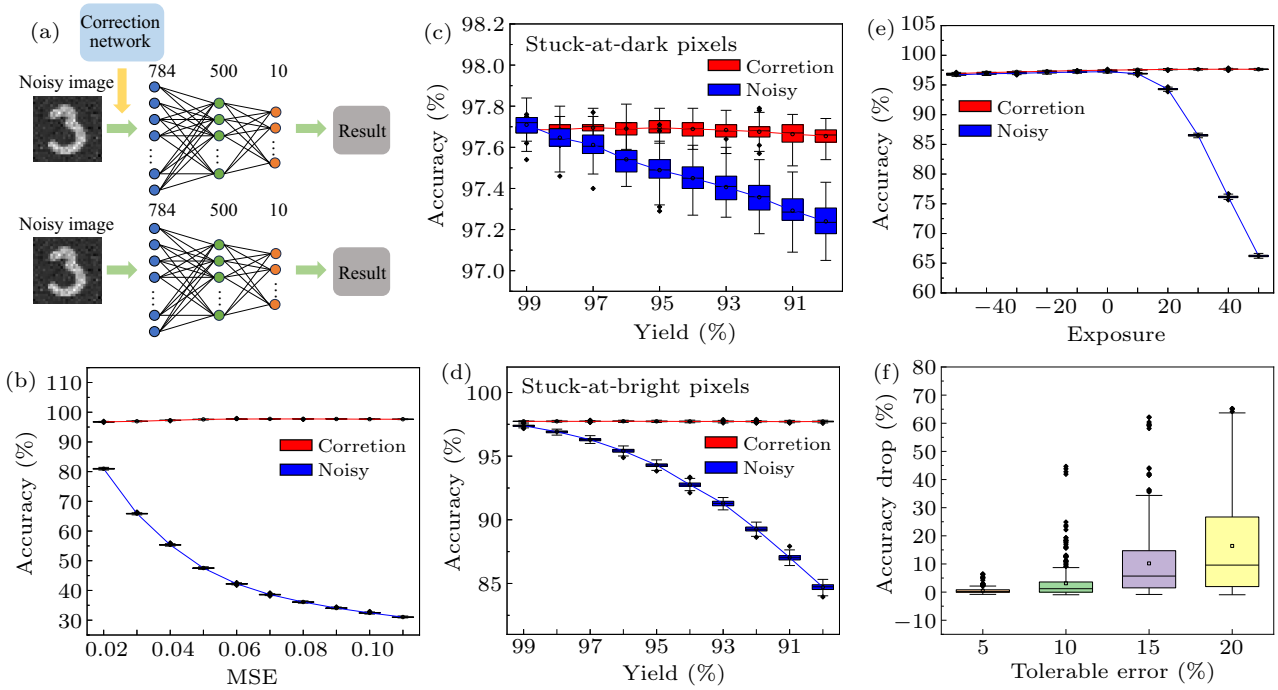



**Fig. 5.** (a) Image processing system with correction network (top panel) and without correction network (bottom panel); (b)–(e) Recognition accuracies of the two systems under varying noise parameters under 100 experiments. Red boxes represent the results with correction network, blue boxes represent the results without correction network. (f) The effect of memristor tolerance error on the accuracy of noise correction network.

A comprehensive performance comparison between the proposed memristor crossbar system and conventional CMOS architectures was conducted for UNet inference tasks, with particular focus on computational latency and energy efficiency. Benchmark measurements from FPGA-based UNet implementations demonstrate baseline performance characteristics of 16.23-ms inference latency and 221.6-mJ/image energy consumption.[17] The power of a single memristor is determined by the applied voltage and average conductance, and can be computed as $(0.15\ \mathrm{V})^2 \times 32.5\ \mu\mathrm{S} = 0.73125\ \mu\mathrm{W}$. The authors in Ref. [18] indicated the memristor's computation time as 50 ns. Therefore, the power consumption of the first layer of the network is estimated at 2.15 nJ. Through sequential accumulation of all network layers, the total system consumption reaches 82.3 nJ/image. In the memristor-based UNet architecture employing multilayer crossbar arrays, signal transmission between successive layers necessitates current-to-voltage conversion through TIAs. To comprehensively evaluate system energy efficiency, quantitative analysis of TIA modules' power consumption and temporal characteristics becomes imperative. Experimental studies indicate that under a $\pm$12-$\mu$A dynamic input current range, the quiescent power consumption of a single TIA module approximates 0.2 mW.[18] Coupled with the memristor unit's 50 ns computational cycle, the per-operation energy consumption of the TIA is derived as $E_{\mathrm{TIA}} = P \times t = 0.2\ \mathrm{mW} \times 50\ \mathrm{ns} = 0.01\ \mathrm{nJ}$. Topological analysis reveals that the cumulative energy consumption of TIAs across the UNet network reaches $\sum E_{\mathrm{TIA}} = 99.61\ \mu\mathrm{J}$, resulting in a cumulative power dissipation of the memristor system at 99.69 $\mu$J, which is $2.2 \times 10^{-3}$ times that of the CMOS system. The temporal analysis reveals 7.624 ms inference latency through parallel analog computation and pipelined dataflow optimization, corresponding to a 2.13 times reduction in processing delay. These performance enhancements stem from the intrinsic advantages of in-memory computing architecture, which eliminates von Neumann bottlenecks while enabling simultaneous analog operations, thereby demonstrating the paradigm-shifting potential of neuromorphic systems for energy-aware edge computing applications.

## 4. Conclusion and perspectives

In this work, we proposed an analog noise correction framework for infrared sensors leveraging memristor-based architecture to address critical challenges such as non-uniform noise, defective pixels (stuck-at-bright/dark), and exposure mismatch. By integrating a lightweight correction network into the image processing pipeline, our system achieves significant enhancements in both noise suppression and recognition accuracy. Experimental results demonstrate that the proposed correction network improves the peak signal-to-noise ratio (PSNR) by up to 78.63% and elevates system recognition rates by 50.13% under diverse noise conditions. And benchmarked against conventional architectures, the proposed system demonstrates significant enhancements in performance metrics, achieving a 2.13-fold reduction in computational latency while simultaneously attaining a three-order-of-magnitude improvement in energy efficiency. This work offers a novel approach for designing image processing systems with ultra-low latency and minimal power consumption, achieved through memristor-enabled analog-domain computation and adaptive noise correction.

## Acknowledgements

Project supported by the National Key Research and Development Program of China (Grant No. 2024YFA1208800) and the National Natural Science Foundation of China (Grant Nos. 62404253, 62304254, and U23A20322).

## References

[1] Irie K, McKinnon A E, Unsworth K and Woodhead I M 2008 *IEEE Trans. Circuits Syst. Video Technol.* **18** 28
[2] Bu F, Yao D, Yang Y and Cao W 2023 *Third International Conference on Optics and Image Processing*, April 7–9, 2023, Xi'an, China, pp. 121–127
[3] Chen S, Lou Z, Chen D and Shen G 2018 *Adv. Mater.* **30** 1705400
[4] Du W, Li C, Huang Y, Zou J, Luo L, Teng C, Kuo H C, Wu J and Wang Z 2022 *IEEE Electron Dev. Lett.* **43** 406
[5] Liu K, Zhang T, Dang B, Bao L, Xu L, Cheng C, Yang Z, Huang R and Yang Y 2022 *Nat. Electron.* **5** 761
[6] Sun Y, Li Q, Zhu X, Liao C, Wang Y, Li Z, Liu S, Xu H and Wang W 2023 *Adv. Intell. Syst.* **5** 2200196
[7] Dang B, Liu K, Wu X, Yang Z, Xu L, Yang Y and Huang R 2023 *Adv. Mater.* **35** 2204844
[8] Zhou G, Li J, Song Q, Wang L, Ren Z, Sun B, Hu X, Wang W, Xu G, Chen X, Cheng L, Zhou F and Duan S 2023 *Nat. Commun.* **14** 8489
[9] Zhan Y, Ding M, Xiao F and Zhang X 2011 *International Conference on Intelligent Computation and Bio-Medical Instrumentation*, December 14–17, 2011, Wuhan, China, pp. 31–34
[10] Dabov K, Foi A, Katkovnik V and Egiazarian K 2007 *IEEE Trans. Image Process.* **16** 2080
[11] Burger H C, Schuler C J and Harmeling S 2012 *IEEE Conference on Computer Vision and Pattern Recognition*, June 16–21, 2012, Providence, Rhode Island, pp. 2392–2399
[12] Zhang K, Zuo W, Chen Y, Meng D and Zhang L 2017 *IEEE Trans. Image Process.* **26** 3142
[13] Xia Q and Yang J J 2019 *Nat. Mater.* **18** 309
[14] Ielmini D and Wong H S P 2018 *Nat. Electron.* **1** 333
[15] Ronneberger O, Fischer P and Brox T 2015 *Medical Image Computing and Computer-Assisted Intervention*, October 5–9, 2015, Munich Germany, pp. 234–241
[16] Chen J Y, Liu X, Du L L, Song B and Sun X B 2024 *Acta Optica Sinica* **44** 375 (in Chinese)
[17] Posso J, Kieffer H, Menga N, Hlimi O, Tarris S, Guerard H, Bois G, Couderc M and Jenn E 2025 *Real-Time Semantic Segmentation of Aerial Images Using an Embedded U-Net: A Comparison of CPU, GPU, and FPGA Workflows*
[18] Liu Z, Tang J, Gao B, Yao P, Li X, Liu D, Zhou Y, Qian H, Hong B and Wu H 2020 *Nat. Commun.* **11** 4234