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INSTRUMENTATION AND MEASUREMENT

A low-noise and high-stability DC source for superconducting quantum circuits

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With the rapid scaling of superconducting quantum processors, electronic control systems relying on commercial off-the-shelf instruments face critical bottlenecks in signal density, power consumption, and crosstalk mitigation. Here we present a custom dual-channel direct current (DC) source module (QPower) dedicated to large-scale superconducting quantum processors. The module delivers a voltage range of ±7 V with 200 mA maximum current per channel, while achieving the following key performance benchmarks: noise spectral density of 20 nV/$\sqrt{\text{Hz}}$ at 10 kHz, output ripple <500 μV_{pp} within 20 MHz bandwidth, and long-term voltage drift <5 μV_{pp} over 12 hours. Integrated into the control electronics of a 66-qubit quantum processor, QPower enables qubit coherence time of $T_1 = 87.6$ μs and Ramsey dephasing time of $T_2 = 5.1$ μs, with qubit resonance frequency drift constrained to ±40 kHz during 12-hour operation. This modular design is compact in size and efficient in energy consumption, providing a scalable DC source solution for intermediate-scale quantum processors with stringent noise and stability requirements, with potential extensions to other quantum hardware platforms and precision measurement systems.

Keywords: superconducting quantum circuits, superconducting qubit, low noise DC source

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1. Introduction

The rapid advancement of superconducting quantum circuits has culminated in processors integrating over one hundred qubits, marking significant progress toward practical quantum computing.[1–6] However, scaling these systems to thousands of qubits required for intermediate-scale quantum applications introduces formidable engineering challenges, not only for the quantum processors themselves, but also for the classical electronic control infrastructure.[7–10] Modern quantum processors rely on precision instrumentation for high-fidelity qubit manipulation and state readout, demanding stringent noise suppression and timing synchronization.[11–15] While commercial off-the-shelf electronic systems have enabled early-stage quantum experiments, their scalability limitations become apparent as qubit counts approach the thousands — a regime where conventional architectures face critical bottlenecks in signal density, power consumption, and crosstalk mitigation.[16–19] This impending scalability barrier highlights an urgent need for integrated, application-specific control solutions that simultaneously optimize noise performance, power efficiency, and spatial footprint to meet the demands of next-generation quantum processors.

As superconducting qubits operate within the microwave frequency regime, microwave electronics are massively used to interface with their quantum dynamics.[10,20–22] At the core of this infrastructure are arbitrary waveform generators (AWGs), which deliver nanosecond-level timing precision for coherent qubit control, and high-speed data acquisition (DAQ) modules that demodulate weak microwave readout signals to resolve quantum states.[23–30] Critically, frequency-tunable qubits and couplers themselves require microvolt-precision direct-current (DC) biasing to stabilize their operating points, a task as essential as waveform generation for maintaining quantum coherence.[22,31–35] Furthermore, the

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microvolt-scale microwave responses from qubits demand a multi-stage amplification chain. Initial signal conditioning relies on cryogenic devices like Josephson parametric amplifiers (JPAs)[36] or low-noise amplifiers (LNAs),[37] followed by room-temperature amplification, each stage requiring stable DC biasing to maintain amplifier performance. Despite their foundational role, DC sources remain underappreciated compared to AWGs and DAQs. While commercial DC sources meet the noise and stability requirements for moderate-scale systems, scaling to thousands of qubits exposes critical bottlenecks: the cumulative cost, physical footprint, and power consumption of hundreds of discrete instruments become prohibitive.[9,38,39] Moreover, maintaining microvolt precision across thousands of channels exacerbates integration challenges, as crosstalk and ground loops degrade performance despite individual instruments meeting specifications.

To overcome these limitations, we introduce QPower, a modular, high-density DC source architecture optimized for scalability. By co-integrating precision biasing for qubits and cryogenic amplifiers within a unified platform, QPower minimizes cost, size and power consumption (15 W per channel), while ensuring the low-noise and high-stability performance required for quantum processors. QPower adopts a distributed reference topology with LTZ1000ACH voltage references,[22,40] achieving ripple noise below 500 μV_{pp}. Hybrid regulation combining low-dropout regulators (LDOs) and active current sharing enhances output stability, while a phase-compensated amplifier array delivers 200 mA drive current with a 64.8° phase margin. Implemented in 2U chassis modules (2 channels/board), the design achieves a long-term drift below 5 μV_{pp}, channel-to-channel crosstalk below 0.3 ppm, high-frequency spurious signals below -95 dBm (9 kHz–200 MHz), and low-frequency noise below 20 nV/$\sqrt{\text{Hz}}$ at 10 kHz.

Key performance metrics are summarized in Table 1. Experimental validation on a 66-qubit processor[41] demonstrates that QPower reliably supports intermediate-scale quantum systems, achieving $T_1 = 87.6 \pm 2.0$ μs and $T_{2,\text{ramsey}} = 5.1 \pm 0.4$ μs with $<$80 kHz peak-to-peak frequency drift over a 12-hour period.

Table 1. Overview of key metrics of QPower.

Performance	Value
Output	2 channels
Output voltage range	±7 V
Output current limit	200 mA
Maximum power consumption	30 W
Minimum step	15 μV
Ripple	$<$ 500 μV (20 MHz bandwidth)
Long-term voltage drift	$<$ 5 μV_{pp} (over 12 hours)
Channel-to-channel crosstalk	$<$ 0.3 ppm
Low-frequency noise	$<$ 20 nV/$\sqrt{\text{Hz}}$ (@10 kHz)
High-frequency spurious	$<$ −95 dBm (9 kHz–200 MHz)

QPower is tailored for DC biasing in quantum applications and omits several advanced features in commercial power supplies, such as arbitrary waveform generation and high-speed communication interfaces. The removal of graphical operating system and touchscreen display also makes it less accessible. These limitations make it less suitable for general-purpose laboratory use or applications requiring flexible control.

2. Electronics design and performance

The hardware architecture of QPower is shown in Fig. 1(a), comprising four functional parts: a digital control unit based on a microcontroller (MCU), a power supply unit employing LDOs, an output stage with a high-resolution digital-to-analog converter (DAC) and amplifier arrays, and a precision reference voltage source. The physical prototype, measuring 210 mm in length and 300 mm in width, is presented in Fig. 1(b).

The digital control unit is responsible for coordinating system operation and regulating output voltages across all channels. To meet the demands of precise voltage control and flexible system access, both remote and local operation are supported. The control architecture integrates three communication interfaces — universal asynchronous receiver–transmitter (UART), general purpose input/output (GPIO), and serial peripheral interface (SPI) — managed via a tri-state bus controller. UART provides communication with a host computer for command input and status monitoring. GPIO allows manual adjustment of parameters on-site. The dual-channel SPI bus simultaneously controls the DAC and liquid crystal display (LCD), enabling voltage updates and system feedback. To ensure reliable data transmission in multi-device configurations, the SPI interface incorporates tri-state logic, which places inactive devices in a high-impedance state to avoid signal contention. During operation, the MCU executes embedded algorithms to process remote commands received via UART and local inputs from GPIO. These are converted into digital control signals and transmitted to the DAC via SPI for high-precision analog voltage generation. Qpower supports both remote operation via a host computer and local manual adjustment, ensuring adaptable control of the system across various operational scenarios.

The power supply part forms the energy backbone of the system, delivering stable power to both digital (MCU, peripherals) and analog (DAC, reference source, amplifier arrays) subsystems through a three-stage noise suppression architecture. First, front–end isolation achieves complete domain separation using dual DC–DC converters: one steps down the external +15 V input to 5 V for digital control circuits, while the other generates isolated ±15 V outputs for analog subsystems, complemented by optical isolators in control signal

paths to maintain electrical isolation. Second, mid-stage regulation employs LT3045/LT3094 LDOs in serial–parallel topology, leveraging their high PSRR ($>$ 90 dB at 1 kHz) and low noise ($<$ 0.8 μV_{rms}) characteristics to condition the $\pm$15 V rails for precision analog components. Finally, post-stage filtering implements a π-type Butterworth low-pass network (100 Hz cutoff, 20 dB attenuation at 1 kHz) to suppress residual high-frequency noise, completing the multi-level noise control strategy that ensures $<$ 20 nV/$\sqrt{\text{Hz}}$ output noise floor at 10 kHz.

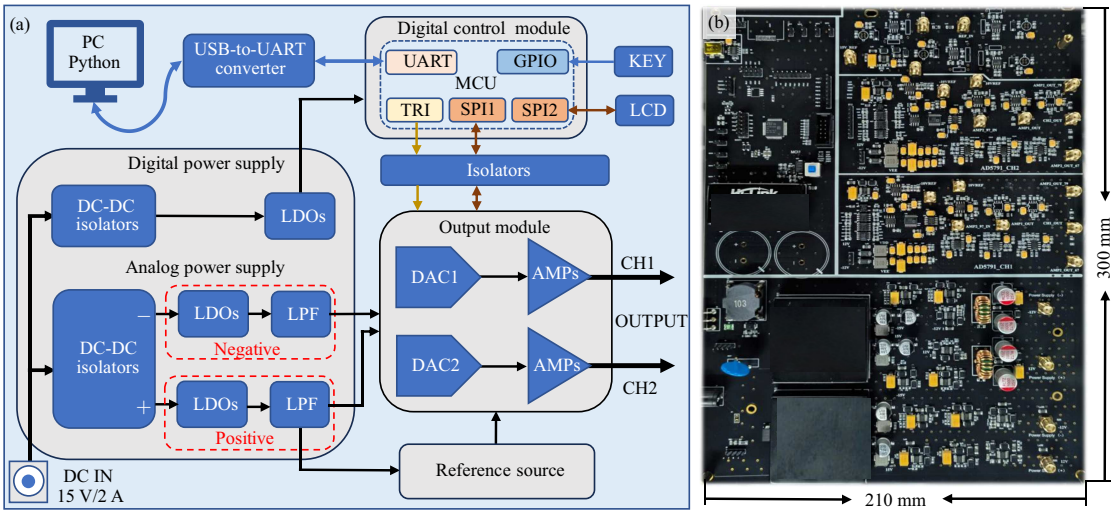


Fig. 1. System architecture of QPower. (a) Block diagram of the hardware design. (b) Photograph of QPower.

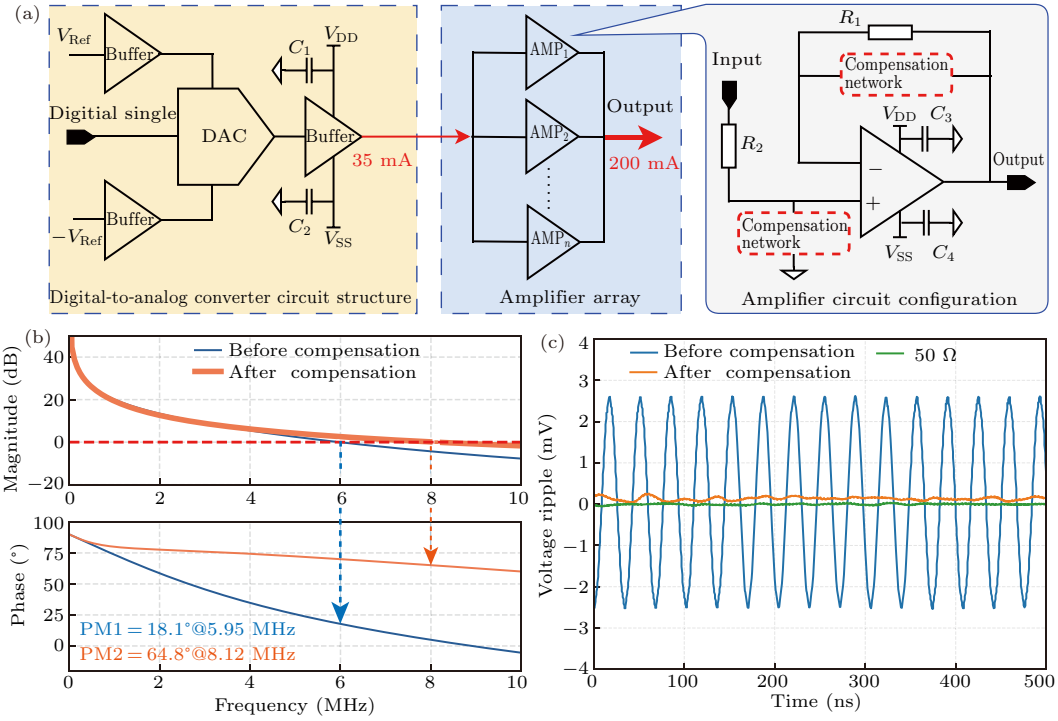


Fig. 2. QPower output design optimization. (a) Schematic of the output design. The yellow region marks the DAC and buffer amplifier stage, the blue region shows the amplifier array, and the gray region highlights the compensation network. (b) Simulated open-loop gain and phase response of the output design. Phase margin (PM) increases from 18.1° (PM1) to 64.8° (PM2) after compensation, with the unity-gain bandwidth extended from 5.95 MHz to 8.12 MHz. (c) Measured output ripple before and after compensation. The blue trace shows ripple before compensation (5 mV_{pp}), while the green trace shows post-compensation results (500 μV_{pp}). The yellow trace indicates the oscilloscope noise floor under a 50 Ω load.

The output part uses a cascade architecture of a 20-bit high-precision DAC (AD5791) and an instrumentation amplifier (AD8676), whose transfer function can be expressed as[42]

$$V_{OUT} = \frac{(V_{REFP} - V_{REFN}) \times D}{2^{20} - 1} + V_{REFN}, \tag{1}$$

where V_{REFP} is the positive reference voltage, and V_{REFN} is the negative reference voltage, D is the 20-bit digital code written to the DAC register, with a range from 0 to $2^{20} - 1$. The reference voltage range of the DAC, $V_{REFP} - V_{REFN}$, determines the dynamic range of the output voltage. The output voltage V_{OUT} is obtained by linearly mapping the digital code D to the reference voltage range.

While the design fulfills the required voltage conversion functionality, practical implementation must address the limited driving capability of the AD5791 DAC, which exhibits a 3.4 kΩ output impedance causing significant signal attenuation in low-impedance or high-capacitance applications. To resolve this, we implement a two-stage architecture combining low-noise operational amplifier arrays and power amplification: First, the initial buffer stage (yellow box in Fig. 2(a))[43] provides high-precision signal conditioning and noise suppression, though its maximum driving current of 35 mA proves inadequate for superconducting quantum system requirements. To enhance current capacity, we cascade a power amplifier array (blue area in Fig. 2(a)), boosting the maximum drive current to 200 mA — achieving performance parity with commercial precision DC sources. This current enhancement introduces potential stability challenges, as the added amplification stage reduces phase margin (PM), risking self-oscillation.[44,45] Through careful phase margin optimization within the stable range of 45° to 70°,[46–48] we implement a compensation network (gray box in Fig. 2(a)) that increases the unity gain bandwidth from 5.95 MHz to 8.12 MHz and improves PM from 18.1° to 64.8°, as verified by LTspice simulations (Fig. 2(b)). Experimental validation (Fig. 2(c)) confirms the compensation eliminates self-oscillation, reducing output ripple from 5 mV_{pp} to 500 μV_{pp}, aligning precisely with simulation predictions.

To ensure the precision of the 20-bit DAC, the reference voltage module is designed to deliver an ultra-low-noise and high stable output. The LTZ1000ACH is selected as the core reference device for its superior performance in precision voltage applications.[22,40] It exhibits a noise of 1.2 μV_{pp} and a temperature coefficient of 0.05 ppm/°C.[40] These characteristics provide the necessary voltage stability and low noise required to maintain system accuracy. The LTZ1000ACH's low intrinsic noise also minimizes signal interference within the analog output chain.

The electronic performance of QPower is systematically characterized by benchmarking six key metrics: output ripple, root mean square (RMS) noise, low-frequency noise, high-frequency noise, long-term stability and crosstalk.

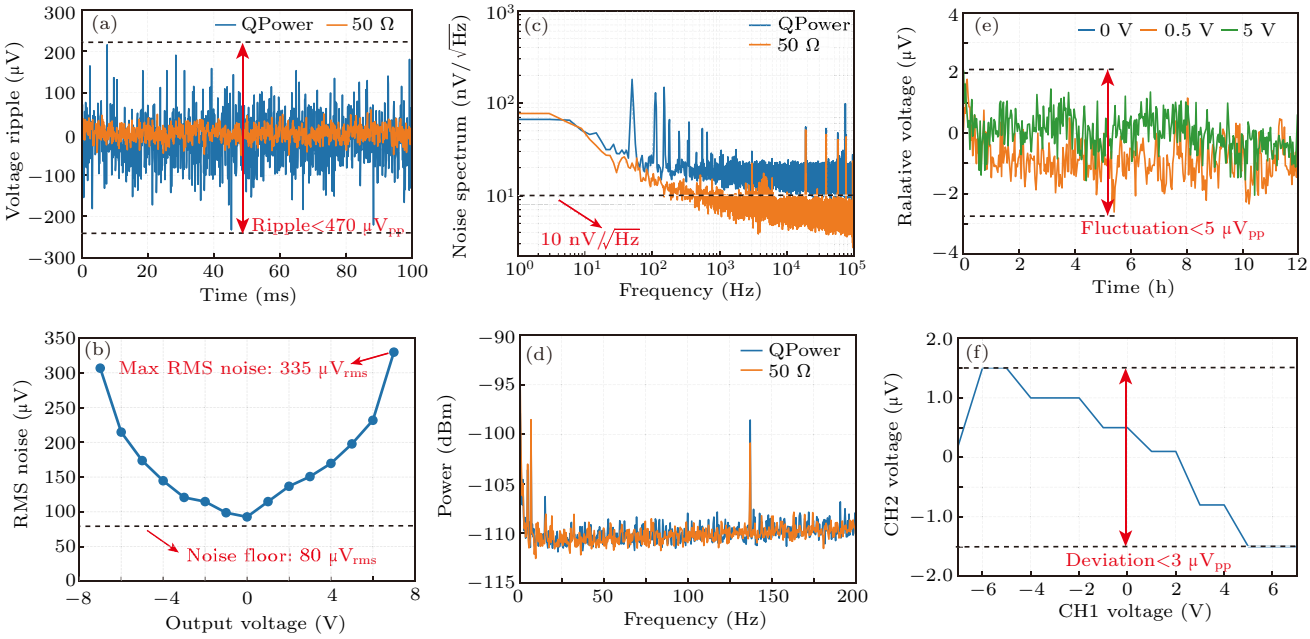


Fig. 3. Electronics performance. (a) DC output ripple benchmark. Within the DC–20 MHz bandwidth, the DC output ripple remains below 500 μV. The oscilloscope noise floor (approximately 100 μV) is verified using a 50 Ω load. (b) RMS noise benchmark. The RMS noise varies with output voltage, with a maximum value of 335 μV_{rms} at 7 V output. The instrument noise floor is approximately 80 μV_{rms}. (c) Low-frequency noise spectrum of the DC output, showing a noise floor of 20 $nV/\sqrt{Hz}$ at 10 kHz. The instrument noise floor, approximately 10 $nV/\sqrt{Hz}$, is validated with a 50 Ω load. (d) High-frequency noise spectrum of the DC output. The noise remains below −95 dBm across the 9 kHz–200 MHz bandwidth. The instrument noise floor, approximately −110 dBm, as well as the peak at 137 MHz, is confirmed using a 50 Ω load. (e) Voltage fluctuation over 12 hours with the DC output set to 0 V, 0.5 V, and 5 V, respectively. The peak-to-peak fluctuation is less than 5 μV. (f) Channel-to-channel crosstalk: The peak-to-peak voltage deviation at channel 2 (CH2) remains below 3 μV_{pp} when the channel 1 (CH1) output is swept from −7 V to +7 V.

The output ripple, representing residual AC voltage superimposed on DC output, is quantified using a RIGOL DHO4804 oscilloscope in AC-coupled mode (20 MHz bandwidth limit). As shown in Fig. 3(a), the peak-to-peak ripple remains below 500 μV_{pp}, with the instrument's intrinsic noise floor characterized as 100 μV_{pp} via 50 Ω termination. Output noise is further evaluated by measuring RMS noise under identical configurations. Figure 3(b) demonstrates RMS noise dependence on output voltage, peaking at 335 μV_{rms} for 7 V output. Slight asymmetry in noise performance is observed between positive and negative outputs, with lower RMS noise measured on the negative side. This is primarily attributed to

the fact that the positive power rail consumes a higher load current than the negative rail, leading to increased noise at positive outputs. Similar asymmetry has also been observed in Ref. [49]. The oscilloscope's RMS noise floor, confirmed under a 50 Ω load, is approximately 80 μV_{rms}.

To evaluate the noise performance comprehensively, low-frequency (10 Hz–100 kHz) and high-frequency (9 kHz–200 MHz) noise characteristics are measured using a Rohde & Schwarz UPV audio analyzer and an FSL18 spectrum analyzer, respectively. As depicted in Fig. 3(c), the low-frequency noise spectral density at 10 kHz is approximately 20 $nV/\sqrt{Hz}$, with some peaks also attributable to the measurement system's inherent noise (verified to be 10 $nV/\sqrt{Hz}$ with a 50 Ω load). Figure 3(d) shows the high-frequency spurious signals remain consistently below −95 dBm, with certain peaks originating from the analyzer itself.

Long-term stability is critical for frequency-tunable superconducting qubits, as DC voltage drift can lead to frequency shifts and coherence degradation. QPower employs instrumentation amplifier arrays combined with multi-stage positive and negative LDOs to minimize drift. Continuous stability measurements at three typical output voltages (0 V, 0.5 V, and 5 V) are performed over 12 hours using a KEITHLEY DMM6500 6.5-digit digital multimeter. As illustrated in Fig. 3(e), peak-to-peak voltage fluctuations at all measurement points remain below 5 μV_{pp}.

For multi-channel DC sources, channel-to-channel crosstalk is a critical concern, particularly in superconducting quantum circuits, where stringent electrical isolation is required to minimize interference between channels. To evaluate the channel-to-channel crosstalk within the same QPower module, the output of channel 1 (CH1) is swept from −7 V to +7 V, while the output of channel 2 (CH2) is monitored. A peak-to-peak deviation of less than 3 μV, corresponding to 0.3 ppm relative to the 14 V output range, is observed, as shown in Fig. 3(f).

3. Benchmark with superconducting qubits

To rigorously evaluate QPower's performance in practical quantum applications, we integrated QPower modules into the Microwave Measurement and Control System (M^2CS)[10] of

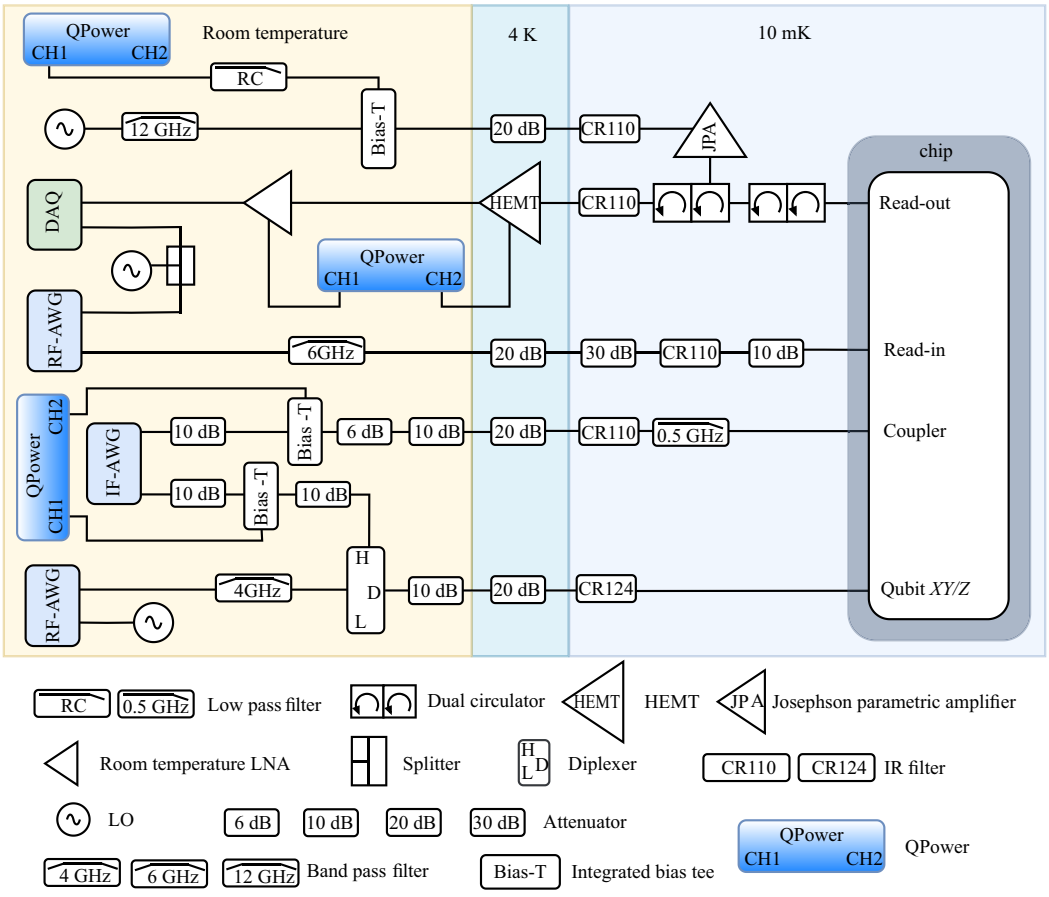


Fig. 4. Schematic of the control and readout setup for superconducting qubits. The M^2CS RF-AWG module generates *XY*-axis microwave driving signals, while the *Z*-axis control signals are synthesized through coordinated operation of the IF-AWG module and QPower, collectively enabling quantum bit manipulation. In the readout pathway, 6–8 GHz microwave probe pulses generated by the RF-AWG module are injected into the quantum chip via cryogenic transmission lines. The returning quantum state response signals undergo isolation through circulators before being sequentially amplified by the JPA for primary parametric amplification, followed by secondary amplification through a HEMT, and tertiary gain enhancement via room-temperature low-noise amplifiers. The processed signals are ultimately demodulated and digitized by a M^2CS DAQ module. Three QPower modules are employed to provide the DC bias for the JPA, HEMT, and room-temperature LNA, a qubit, and a tunable coupler.

a 66-qubit superconducting quantum processor.[41] Specifically, three QPower modules are deployed: (1) DC biasing of a JPA at the mixing chamber stage, (2) simultaneous biasing of a cryogenic (4 K) high electron mobility transistor (HEMT) LNA and a room-temperature LNA, and (3) precise flux control for both a qubit and a tunable coupler, as illustrated in Fig. 4. The quantum processor and JPA are thermally anchored to the dilution refrigerator's mixing chamber, maintained at < 10 mK.

The qubit state measurement chain employs multi-stage filtering networks that suppress thermal noise interference across all cryogenic stages: RF-AWG generated probe signals undergo attenuation and filtering before entering the quantum chip, while the weak response signals experience sequential amplification through JPA (base temperature), cryogenic HEMT LNA, and room-temperature LNA prior to digitization by M^{2}CS's DAQ module. This architecture enables high-fidelity quantum state discrimination through noise-optimized signal conditioning.

QPower's stability directly impacts qubit coherence metrics. We systematically evaluated energy relaxation time (T_1), Ramsey dephasing time ($T_{2,\text{ramsey}}$), and spin-echo coherence time ($T_{2,\text{echo}}$) at 3.8 GHz, an operating point that is most sensitive to external flux noise. As shown in Figs. 5(a) and 5(b), the measured T_1 reaches 87.6 ± 2.0 μs through π-pulse excited state decay measurements. Ramsey interferometry reveals $T_{2,\text{ramsey}} = 5.1 \pm 0.4$ μs, while spin-echo sequences extend coherence to $T_{2,\text{echo}} = 23.5 \pm 1.2$ μs through low-frequency noise suppression.[10]

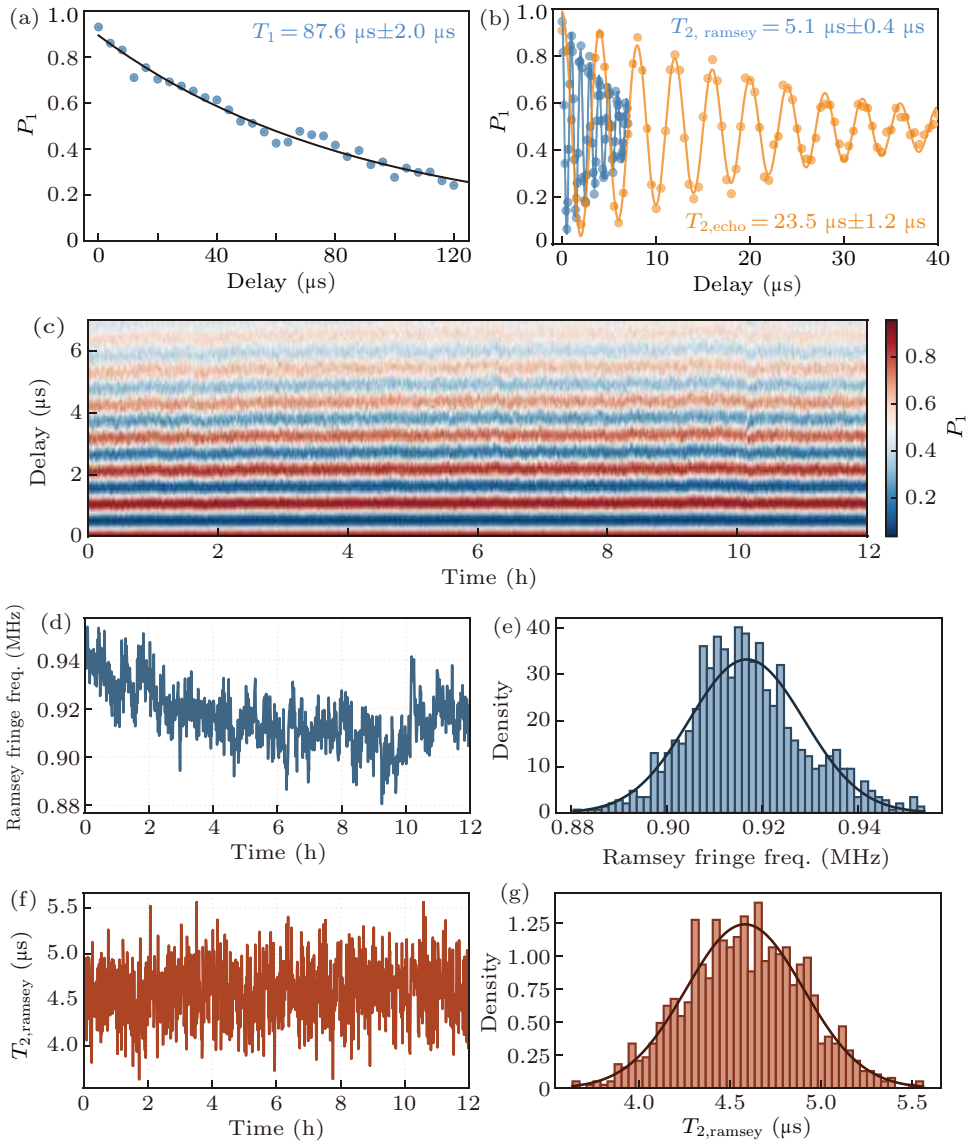


Fig. 5. Benchmarking QPower with superconducting qubits. (a), (b) Qubit coherence benchmark showing $T_1 = 87.6 \pm 2.0$ μs, $T_{2,\text{ramsey}} = 5.1 \pm 0.4$ μs, and $T_{2,\text{echo}} = 23.5 \pm 1.2$ μs, measured at the qubit's steepest point. (c) Qubit dephasing time $T_{2,\text{ramsey}}$ and resonance frequency test based on Ramsey interference, monitored over a 12-hour period. The frequency color fades as the qubit's frequency identification shifts into the noise background, representing $T_{2,\text{ramsey}}$. (d) Ramsey fringe frequency monitored over a 12-hour period. (e) Histogram of data from (d), showing frequency fluctuation within ±40 kHz (peak-to-peak < 80 kHz). (f) 12-hour $T_{2,\text{ramsey}}$ monitoring. (g) Histogram of data from (f), showing a Gaussian distribution of $T_{2,\text{ramsey}}$ between 3.5 μs and 5.5 μs.

Long-term stability was quantified through 12-hour continuous monitoring of the Ramsey interferometry, as shown in Fig. 5(c). Statistical analysis of 1000 repeated measurements reveals two key performance metrics: First, the Ramsey fringe exhibits ±40 kHz fluctuation, corresponding to peak-to-peak variations below 80 kHz in the qubit resonant frequency (Figs. 5(d) and 5(e)). Second, the Ramsey $T_{2,\mathrm{ramsey}}$ maintains consistent performance within 3.5–5.5 μs throughout the duration (Figs. 5(f) and 5(g)). These stability metrics demonstrate QPower's capability to maintain ppm-level frequency control while preserving quantum coherence characteristics — critical requirements for large-scale quantum computing systems.

4. Conclusion

We develop QPower, a low-noise, high-stability DC source tailored specifically for the demanding requirements of large-scale superconducting quantum processors. The system's hierarchical noise suppression architecture achieves benchmark performance metrics including: (1) voltage noise density $< 20\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 10 kHz, and (2) long-term drift $< 5\ \mu\mathrm{V}$ over 12 hour operation — parameters competitive with premium commercial instruments while consuming only 15 W per channel. This performance enables simultaneous support for multi-stage quantum measurement chains, including JPA biasing, cryogenic HEMT and room-temperature LNA powering, and qubit flux control in intermediate-scale quantum systems.

Experimental validation using a 66-qubit superconducting processor demonstrates QPower's capability to sustain quantum coherence characteristics matching state-of-the-art requirements: measured relaxation time $T_1 = 87.6 \pm 2.0$ μs and Ramsey dephasing time $T_{2,\mathrm{ramsey}} = 5.1 \pm 0.4$ μs at the flux-sensitive operating point. The system maintains qubit frequency stability with ±40 kHz deviation during 12-hour continuous operation, directly correlating DC source noise performance with quantum coherence preservation — a critical requirement for scalable quantum computing.

Furthermore, the modular design principle underlying QPower demonstrates extensibility to alternative quantum computing platforms, such as silicon-based quantum dot systems.[50–52] This architectural flexibility positions QPower as a versatile solution for emerging quantum processor control architectures requiring distributed power systems, and high-precision measurement applications beyond quantum computing.

Although we only benchmark a few channels in this paper, the current architecture can be directly scaled to dozens of channels. Further scaling to much larger sizes introduces challenges in thermal management and signal integrity. For instance, a 1000-qubit processor with tunable qubits and couplers may require approximately 3000 concurrent DC channels, consuming roughly 45 kW with QPower. At this scale, passive cooling becomes inadequate, necessitating liquid cooling to maintain thermal stability. High-density layouts also raise risks of crosstalk from electromagnetic interference and power supply coupling, which can be mitigated through careful circuit design, spacing, and shielding. The use of compact, efficient power modules could further improve thermal efficiency and system scalability.

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