

Impact of surface passivation on the electrical stability of strained germanium devices

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Impact of surface passivation on the electrical stability of strained germanium devices

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Strained germanium hole spin qubits are promising for quantum computing, but the devices hosting these qubits face challenges from high interface trap density, which originates from the naturally oxidized surface of the wafer. These traps can degrade the device stability and cause an excessively high threshold voltage. Surface passivation is regarded as an effective method to mitigate these impacts. In this study, we perform low-thermal-budget chemical passivation using the nitric acid oxidation of silicon method on the surface of strained germanium devices and investigate the impact of passivation on the device stability. The results demonstrate that surface passivation effectively reduces the interface defect density. This not only improves the stability of the device's threshold voltage but also enhances its long-term static stability. Furthermore, we construct a band diagram of hole surface tunneling at the static operating point to gain a deeper understanding of the physical mechanism through which passivation affects the device stability. This study provides valuable insights for future optimization of strained Ge-based quantum devices and advances our understanding of how interface states affect device stability.

Keywords: hole, strained germanium, interface trap, stability, surface passivation

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1. Introduction

Strained germanium hole qubits have shown significant promise in semiconductor quantum computing owing to their exceptional physical properties, such as weak hyperfine interactions,[1–4] strong spin–orbit coupling[3,5–7] and strain-engineered light–heavy hole splitting.[8,9] Recently, a wide range of advances have been reported, including various qubit encoding schemes and operations,[6,10–12] local scaling,[13–16] spin shuttling[17] and coupling with microwave resonators.[18–20] However, despite this promising potential, the devices hosting hole qubits face significant challenges in practical applications, particularly those caused by interface traps at the surface. These traps induce severe surface tunneling of holes within the quantum well (QW),[21–27] leading to threshold voltage drift and stability issues,[23,26,28,29] thereby complicating device measurements and degrading reliability.[18,21,23–25,30–32]

Interface traps arise from various dangling bonds at the interface.[33] These dangling bonds are typically caused by incomplete oxidation of the wafer during exposure to air after the epitaxial growth process,[32–35] and can be reduced through appropriate surface passivation methods.[24,32,36,37] Although thermal oxidation is effective for silicon and germanium passivation,[38] it risks heterostructure relaxation at high temperatures, making it unsuitable for strained germanium devices.[8,23] Therefore, strained germanium devices require lower-temperature methods such as hydrogen peroxide treatment or oxygen plasma passivation.[32,35] However, both passivation methods exhibit extremely fast oxidation rates, making it difficult to precisely control the oxide thickness,[35] and the latter method carries the risk of introducing plasma-induced damage.[33]

In contrast, the nitric acid oxidation of silicon (NAOS) method avoids the shortcomings of the aforementioned methods. By leveraging the strong oxidizing property of boiling concentrated nitric acid, it forms an ultra-thin, dense silicon oxide layer with quality comparable to that achieved by thermal oxidation.[39,40] The self-limiting nature of this reaction

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ensures the formation of an oxide layer with a fixed thickness, along with high repeatability and reliability.[39] This makes the method highly favorable for strained germanium heterostructures with complex stacking structures.

In this study, we perform a low-thermal-budget chemical passivation using the NAOS method on a strained germanium heterostructure and investigate the impact of surface passivation on device stability. Through cyclic scanning experiments on the transfer curve, we demonstrate that this passivation method reduces the interface defect density by half, thereby facilitating rapid stabilization of the threshold voltage. Moreover, we systematically investigate the impact of interface states on device stability through time-dependent current measurements. We develop a series of energy level diagrams to explain the current decay behavior and the underlying physical mechanisms at fixed and varying static operating points. Our study demonstrates that surface passivation not only effectively reduces interface trap density but also significantly enhances direct current (DC) stability.

2. Device fabrication and experimental setup

The devices used in this work are fabricated on a reverse-graded strained germanium substrate with a $Si_{0.2}Ge_{0.8}/Ge/Si_{0.2}Ge_{0.8}/Si$ cap heterostructure identical to that used in the work of Kong *et al.*,[23] where the 32 nm deep QW enhances the detectability of interface state effects. We observe that the silicon cap layer cannot be fully oxidized in air, leading to the formation of the stacked structure depicted in the left panel of Fig. 1(a) (see supplementary information B). In this structure, the original silicon cap layer, which was grown in the chamber, is replaced by the natural oxide (SiO_x) and the residual unoxidized silicon layer (new Si cap).

Therefore, before passivation, to ensure that the nitric acid fully reacts with silicon and forms a dense silicon oxide layer, we first use buffered oxide etch (BOE) solution to remove the natural oxide from the surface. Subsequently, the NAOS method is applied to form a high-quality oxide layer (see supplementary information A for fabrication details). Following surface passivation, cross-sectional transmission electron microscopy (TEM) and x-ray photoelectron spectroscopy (XPS) analyses confirm the complete depletion of the thin Si cap layer and the formation of an ultra-thin (1.5 nm), high-quality silicon–germanium oxide (see supplementary information B). This results in the stacked structure shown in the right panel of Fig. 1(a).

To verify the effect of passivation, we fabricate and measure Hall bar-type field-effect transistors (FETs) on two heterostructures shown in Fig. 1(a), referred to as the IDLE (without surface passivation) and BN (BOE + NAOS, with surface passivation) samples, respectively. The samples are measured at a temperature of $T \sim 4$ K, and the circuit diagrams used for subsequent characterization experiments are shown in Fig. 1(b). When a certain negative gate voltage V_{gs} is applied to the top gate, the FET is turned on and the transport current I_{ds} will be detected by a lock-in amplifier under source–drain excitation V_{ds}.

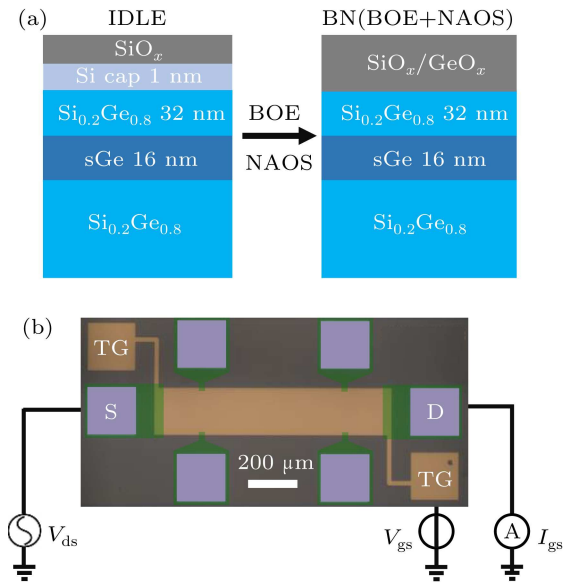


Fig. 1. Ge/SiGe heterostructure and field-effect transistor (FET) device. (a) Ge/SiGe layer schematics without (left panel) and with (right panel) passivation treatment. (b) Light field pattern of Hall bar-type FET and measurement setup of FET device [TG, top gate (brown), S (D), source (drain) consists of ion implantation (green) and contact metal (silver)].

3. Cyclic scanning experiments on transfer curves

Cyclic scanning experiments on the transfer curves are a commonly used and effective method for assessing voltage-induced hysteresis of heterostructure FET devices and stability of the threshold voltage V_{th}.[24,25,32] The measurement schematic is depicted in Fig. 2(a), which illustrates each different measurement cycle. For clarity, we consider the m-th cycle as an example. After completing the $(m-1)$-th measurement cycle and initiating the m-th measurement cycle, we first apply a negative gate voltage from $V_{gs} = V_{min,m-1}$ to $V_{gs} = V_{min,m}$ (indicated by a black horizontal left-pointing arrow), where $V_{min,m-1}$ and $V_{min,m}$ are the minimum gate voltage of the transfer curve during the $(m-1)$-th and m-th measurement cycles, respectively, wait for a holding time t_{hold} (indicated by black vertical down-pointing arrow) and then sweep V_{gs} back to 0 (indicated by the black dashed arrow).

In the holding period, non-equilibrium holes in the QW are induced by the electric field to tunnel to the surface, where they are trapped by defects.[21,24] These trapped holes act as positively charged centers and screen the electric field from the gate, increasing the threshold voltage V_{th} of the device. The threshold voltage shift $V_{th,it}$ caused by interface traps follows the relation (see supplementary information E for the deriva-

tion)

$$V_{\mathrm{th,it}} = -\frac{qp_{\mathrm{it}}}{C_{\mathrm{ox}}}, \tag{1}$$

where C_{ox} and q are capacitance of the gate oxide layer and elementary charge, respectively, and p_{it} is the density of interface traps filled by holes. Therefore, by monitoring the shift of the threshold voltage and after obtaining the capacitance of the gate oxide layer C_{ox} (the extraction of C_{ox} is detailed in supplementary information F), the density of filled interface traps p_{it} can be estimated.

The extraction of V_{th} can be achieved by scanning the transfer curve during the m-th measurement cycle (with V_{gs} scanned from 0 to $V_{\mathrm{min},m}$, represented by a colored horizontal left arrow, and the result of the m-th cycle scan is shown in the inset of Fig. 2(a)). In this experiment, V_{th} is defined as the V_{gs} at 20% of the maximum I_{ds} during the final scan in the sequence of transfer curves (indicated by the purple dashed line in the inset). Subsequently, V_{gs} is further reduced to a more negative voltage $V_{\mathrm{min},m+1} = V_{\mathrm{min},m} - \Delta V_{\mathrm{min}}$ to initiate the $(m+1)$-th measurement cycle and the above measurement process is repeated, where ΔV_{min} is the step size between consecutive cycles. This process is repeated until the threshold voltage stabilizes and reaches saturation. The measurement details are provided in supplementary information C. Figures 2(b) and 2(c) show the combined result of the transfer curves of the BN sample and IDLE sample for different values of V_{min}.

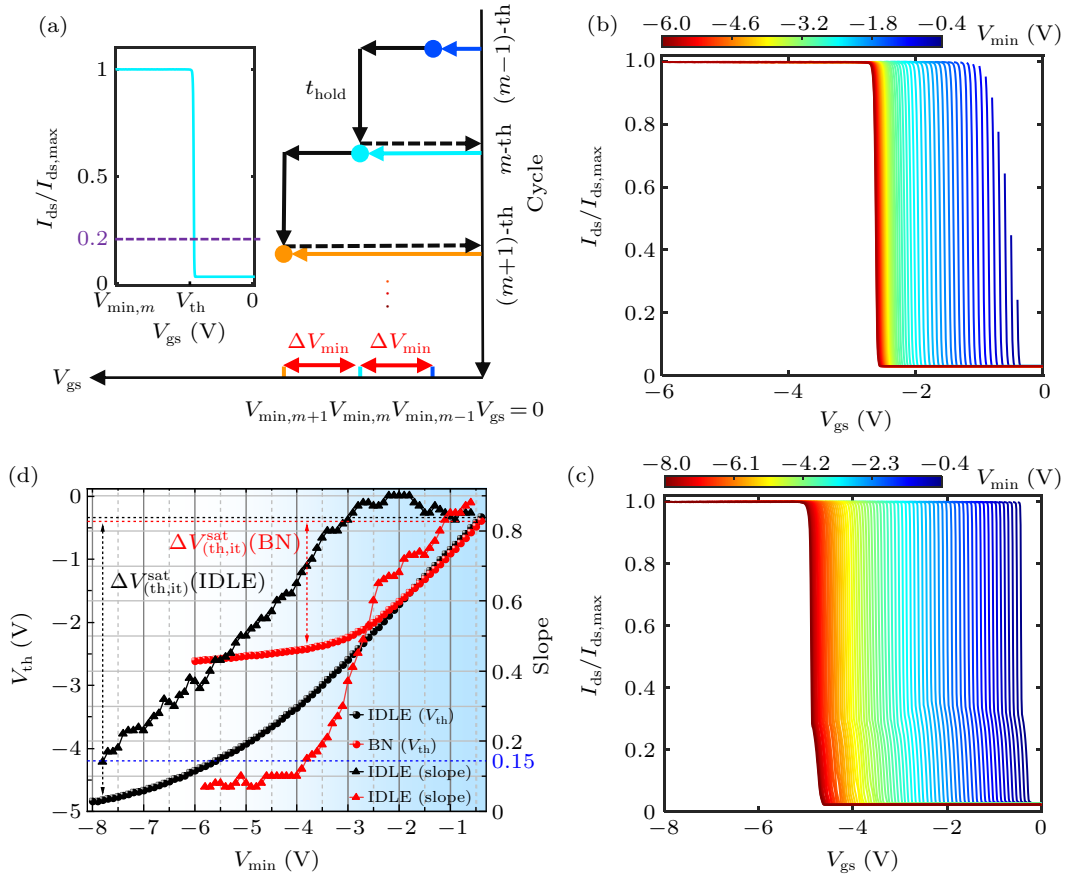


Fig. 2. Cyclic scanning experiments on transfer curves. (a) Measurement process of cyclic scanning of a transfer curve. The inset shows the transfer curve during the m-th cycle scanning with V_{gs} scanned from 0 to $V_{\mathrm{min},m}$. Here, $m = 29$ and $V_{\mathrm{min},m} = -3.2$ V. The current is normalized to $I_{\mathrm{ds}}/I_{\mathrm{ds,max}}$, where $I_{\mathrm{ds,max}}$ stands for the maximum current at the last cyclic scanning experiment. The purple dashed line represents the condition where the current ratio $I_{\mathrm{ds}}/I_{\mathrm{ds,max}} = 0.2$, and the corresponding gate voltage V_{gs} is defined as the threshold voltage V_{th}. (b) Transfer curves for V_{min} decreasing from -0.4 V (blue) to -6 V (red) of the BN sample. (c) Transfer curves for V_{min} decreasing from -0.4 V (blue) to -8 V (red) of the IDLE sample. (d) Threshold voltage V_{th} (circles) and slope of V_{th} (triangle) dependent on V_{min}. The black and red lines correspond to the results from the IDLE sample and BN sample, respectively. The blue gradient background represents the gradual saturation process of the threshold voltages V_{th} (from blue to white). The blue dashed line represents a slope of 0.15, which is defined as the standard for the threshold saturation in this experiment.

To allow for a clear comparison, the threshold voltages V_{th} of both IDLE and BN samples are shown in Fig. 2(d). As V_{min} decreases, the threshold voltage V_{th} undergoes a rapid drop followed by gradual saturation. This saturation behavior has been proved in a previous study to be caused by trap filling saturation.[21] Therefore, the overall interface trap density of the device can be estimated based on the threshold voltage difference between the state of no hole-filled defects and the saturation of hole-filled defects according to Eq. (1). The initial threshold voltage of the device, $V^0_{\mathrm{th,it}}$, is defined as the threshold voltage under defect-free conditions, indicated by the black dashed line for the IDLE sample ($V^0_{\mathrm{th,it}} = -0.33$ V)

and the red dashed line for the BN sample ($V^0_{\rm th,it} = -0.39$ V) in Fig. 2(d)). However, the threshold voltage saturation behavior of the device is a smooth process. To better describe this saturation behavior, we introduce the slope of $V_{\rm th}$ versus $V_{\rm min}$ based on the linear fit of the five nearest data points. Because the leakage in the IDLE sample begins after the slope reaches 0.15 and $V_{\rm th}$ is nearly saturated, we define slope = 0.15 as the threshold for defect filling saturation, which is indicated by the blue dashed line in Fig. 2(d). The corresponding threshold voltage at this point is defined as $V^{\rm sat}_{\rm th,it}$. At this slope, the IDLE sample has $V_{\rm min} = -8.00$ V and $V^{\rm sat}_{\rm th,it} = -4.82$ V, while for the BN sample, $V_{\rm min} = -3.80$ V and $V^{\rm sat}_{\rm th,it} = -2.42$ V. Based on above analysis, we can obtain the respective differences in threshold voltage between the state of no hole-filled defects and the saturation of hole-filled defects: $\Delta V^{\rm sat}_{\rm (th,it)}$ (IDLE) $= V^{\rm sat}_{\rm th,it} - V^0_{\rm th,it} = -(4.49 \pm 0.03)$ V (IDLE sample, black dashed double arrow), $\Delta V^{\rm sat}_{\rm (th,it)}$ (BN) $= -(2.03 \pm 0.02)$ V (BN sample, red dashed double arrow). We can calculate the interface state densities to be $(8.83 \pm 0.06) \times 10^{12}$ cm^{-2} for the IDLE sample and $(3.99 \pm 0.04) \times 10^{12}$ cm^{-2} for the BN sample. These values indicate that surface passivation could effectively reduce the density of interface traps by half.

4. Time-dependent current measurement

In practical applications, even under a constant gate voltage, holes can undergo Fowler–Nordheim tunneling (FNT) and be trapped by interface states, leading to a drift in the DC operating point.[24] This drift necessitates periodic real-time calibration to bring the DC operating point back to the desired value, which typically increases the measurement complexity.[30,31,41] To investigate the impact of interface states on this static stability, we conduct the time-dependent current measurement of the FET under a fixed gate voltage. As shown in Fig. 3(a), the time dependence of the current for the BN and IDLE samples is measured with gate voltages ranging from −0.4 V to −6 V.

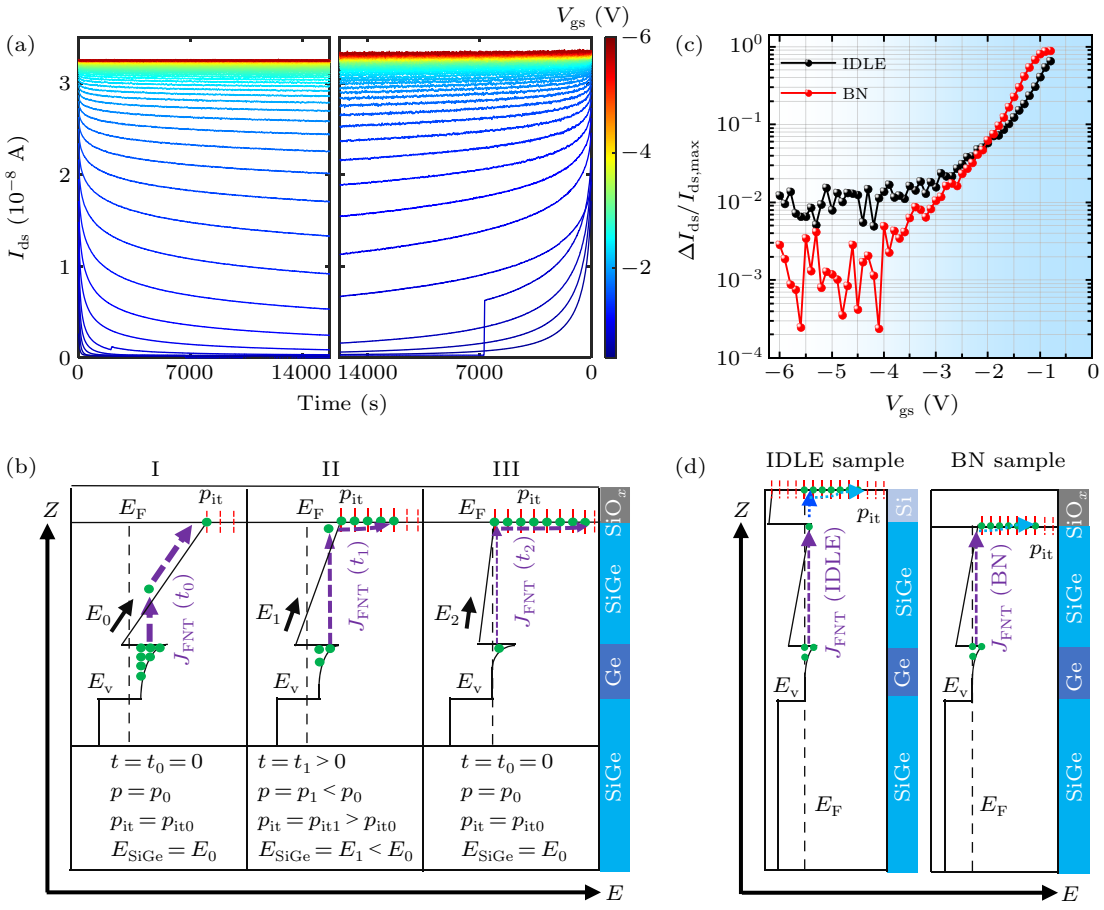


Fig. 3. Time-dependent current measurement. (a) Long-term current stability at different voltages from −0.4 V to −6 V for sample BN (left panel) and sample IDLE (right panel). (b) Energy levels at different times under a fixed gate voltage, corresponding to one of the colored curves in panel (a). Panels I to II represent a rapid decay process. Panels II to III represent a long-tail decay process. The solid green circles represent holes. The solid red line (dashed line) represents interface states with (without) holes filled, while the purple dashed arrow lines represent the FNT current $J_{\rm FNT}$, with varying widths indicating different magnitudes of $J_{\rm FNT}$. The black dashed line represents the Fermi level within the semiconductor. $E_{0,1,2}$ represents the electric field strengths in the SiGe barrier at three different times $t_{0,1,2}$. Additionally, Z represents the sample growth direction and E indicates the direction of increasing hole potential. (c) Normalized current decay in IDLE and BN samples at different gate voltages. (d) Schematic diagram of the process in which holes in the QW are captured by surface defects in IDLE and BN samples, respectively. The purple, blue and light blue dashed arrows represent the FNT process through the SiGe barrier layer, direct tunneling through the Si cap layer and the surface defect capture process, respectively.

As shown in the curve for a fixed gate voltage in Fig. 3(a), the rate of current decay over time is complex, exhibiting both rapid decay and long-tail decay. This phenomenon can be explained by the energy level diagram of the valence band maximum (VBM) shown in Fig. 3(b). As illustrated in panel I of Fig. 3(b), when a new measurement sequence begins ($t = t_0 = 0$ s), a more negative gate voltage V_{gs} is applied to the top gate, the VBM in the QW exhibits significant bending and reaches above the Fermi level, causing a large number of holes to be injected from the source–drain into the QW, forming a high-density two-dimensional hole gas (2DHG) $p = p_0$. Meanwhile, the application of a gate voltage also enhances the electric field with the SiGe barrier ($E_{SiGe} = E_0 > E_{FNT0}$, where E_{FNT0} is the critical tunneling field for FNT). These factors induce a large FNT current density $J_{FNT}(t_0)$ from the QW to the surface, causing holes in the QW to tunnel to the surface and be captured by surface traps (this tunneling process can be represented by the purple dashed line in the figure). As these captured holes form fixed charges on the surface, the surface potential will be lowered and the electric field generated by the gate voltage within the bulk will be screened according to Gauss's theorem (see supplementary information E and at this moment, for $t = t_1$, where $t_1 > t_0$). This indirectly drops the potential at the QW and reduces the density of the 2DHG, $p = p_1 < p_0$ (see panel II of Fig. 3(b)). As a result, both the reduced p and the weakened SiGe barrier field contribute to the drop in surface tunneling current density $J_{FNT}(t_1) < J_{FNT}(t_0)$ from the source and tunneling process, respectively, slowing down the decay rate of the current in the QW over time. Therefore, the above process will result in a rapid decay with a variable rate at the beginning of the measurement $(t = t_0 \rightarrow t_1)$. Furthermore, as more holes are filled into the interface states $p_{it} = p_{it2} > p_{it1}$ $(t = t_2 > t_1$; see panel III of Fig. 3(b)), the screening effect of the electric field will become more pronounced, $E_{SiGe} = E_2 < E_1$, and the hole density in the buried channel will decrease, $p = p_2 < p_1$. Under this circumstance, the hole tunneling current density will decline further, $J_{FNT}(t_2) < J_{FNT}(t_1)$, resulting in the observed long-tail decay behavior in the subsequent time period.

From the above analysis, it is evident that the tunneling rate changes continuously over time, making it difficult to describe the behavior analytically based on the available data. To clearly compare the current decay behaviors under different gate voltages, we normalize the current decay as $\Delta I_{ds}/I_{ds,max}$, where $\Delta I_{ds} = I_{ds,max} - I_{ds,min}$ with $I_{ds,max}$, $I_{ds,min}$ representing the maximum and minimum current obtained in one measurement sequence, respectively. The results are presented in Fig. 3(c). It is noticeable that the current decay behavior also exhibits a similar trend of saturation as the threshold voltage. This is likely also due to the saturation of defect filling.

Next, we focus on comparing the current decay in IDLE and BN samples. Interestingly, we observe an intersection point at around $V_{gs} = -2$ V, which could result from the interplay of differences in their stacking structures and the density of interface traps. When $V_{gs} \geq -2$ V, the current decay of the IDLE sample is slower than that of the BN sample. This can be attributed to the differences in the stacking structure and interface state distribution, as shown in Fig. 3(d), which illustrates the energy levels based on the material stacking structure in Fig. 1(a). As shown in the figure, for the IDLE sample, the holes in the QW are first captured by surface defects through FNT across the SiGe barrier layer. This is followed by direct tunneling of carriers through the Si cap layer to the surface defect sites. However, in the BN sample, due to the absence of the Si cap layer, holes that undergo FNT directly bypass this step and begin the next step, the defect capture process. In this process, the defect states preferentially occupy the shallowest energy interface states above the Fermi level. However, in the BN sample, the interface traps are located on the upper surface of the SiGe barrier layer, while in the IDLE sample, the interface traps reside on the upper surface of the Si cap layer. The higher VBM of the Si cap layer places the defect states further from the VBM. Consequently, the capture of holes in the IDLE sample is slower due to the increased distance between the defect states and the VBM.[42] Based on these two factors, the BN sample exhibits a faster decay of current than the IDLE sample at $V_{gs} > -2$ V. The above process demonstrates that the Si cap layer effectively reduces the rate of DC operating point drift, underscoring the significance of the device structure for device performance

However, when $V_{gs} < -2$ V, the decay behavior reverses. As mentioned earlier, the interface trap density in the BN sample is lower than that of the IDLE sample. Therefore, as the traps are gradually filled, the proportion of interface trap unoccupied by holes in the BN sample will decrease rapidly, weakening the FNT current. As a result, the BN sample exhibits excellent stability under lower gate voltages. Therefore, at a more negative voltage the decay mechanism dominated by interface state density becomes a critical factor when $V_{gs} < -2$ V.

Additionally, in Fig. 3(c), as the gate voltage decreases, the current decay for sample BN reaches 0.1% at $V_{gs} \approx -4$ V, which is comparable to the noise level. In contrast, the decay for the IDLE sample remains unchanged after $V_{gs} \approx -3$ V, approaching 1%, with a decay ratio at least an order of magnitude higher than that of the BN sample. This suggests that the large interface trap density in the IDLE sample causes holes to continuously tunnel via FNT to the surface, where they are captured by the high-density interface states. The results further demonstrate that the passivated samples, with their lower interface state density, exhibit faster stabilization and enhanced stability, which will significantly reduce the resources needed for future measurement calibration.

5. Conclusion

In conclusion, we have performed low-thermal-budget chemical passivation using the NAOS method on strained germanium FETs, and investigated the impact of surface passivation on device stability. By comparing the threshold voltage shift caused by saturated trap filling, we demonstrate that surface passivation effectively reduces the interface state density to half of its original value. Furthermore, we analyzed the impact of gate voltage and passivation on the stability of the transport current by presenting the energy band diagram of hole surface tunneling and explained the underlying physical mechanisms. Our results indicate that the device structure may play a significant role in device stability. However, the magnitude and speed of the gate voltage required for the device to ultimately reach a stable state are still determined by the interface traps. In future, we can improve device stability by combining these two approaches, such as increasing the thickness of the cap layer and introducing a series of tunneling suppression layers similar to the silicon cap. This study provides new methods, and perspectives for optimizing strained germanium devices, highlights the importance of interface trap density for device stability and lays a valuable foundation for further improving the performance of strained germanium devices.

Acknowledgments

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