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Citation: Chin. Phys. B, 2025, 34 (**7**): 077201. DOI: 10.1088/1674-1056/adcc86
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CMOS compatibility and excellent resistive switching of tantalum oxide-based resistive switching memory

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(Received 12 February 2025; revised manuscript received 7 March 2025; accepted manuscript online 15 April 2025)

A CMOS compatible RRAM device with TaN/Ta/TaO_x/TaN structure was proposed for nonvolatile memory applications. Excellent resistive switching characteristics, including low operation voltages (< 1 V), low operation current (< 100 μA), good programming/erasing endurance ($> 10^6$ cycles), satisfactory uniformity, and reliable data retention, have been demonstrated. Furthermore, all of the elements in the fabricated TaN/Ta/TaO_x/TaN devices are highly compatible with modern CMOS manufacturing process, showing promising application in the next generation of nonvolatile memory.

Keywords: resistive switching, tantalum oxide, CMOS compatibility

PACS: 72.20.–i, 73.40.Rw, 61.72.jd, 68.60.–p

DOI: 10.1088/1674-1056/adcc86 **CSTR:** 32038.14.CPB.adcc86

1. Introduction

Resistive random access memory (RRAM), based on resistive switching characteristics between a high resistance state (HRS) and a low resistance state (LRS) driven by voltage or current bias, has been intensively studied and regarded as prospective choice for next generation nonvolatile memory applications due to its simple structure, fast switching speed, low power consumption, and high density storage.[1–4] Because of the easy fabrication process, high endurance, excellent scalability, low cost, as well as excellent compatibility with the current complementary metal–oxide–semiconductor (CMOS) technology, binary transition metal–oxide-based RRAM devices create an even greater attraction from both industry and academic.[5–12]

In recent years, tantalum oxide, one of the most promising binary transition-metal–oxide materials, has been especially attractive for its application in RRAM devices because it exhibits advantages not only in its attraction for high switching endurance, fast switching speed, three-dimensional (3D) stacking, but also in its compatibility with back-end-of-line (BEOL) processing in CMOS integrated circuits.[13–20] Lee *et al.*, for example, have demonstrated a TaO_x-based asymmetric passive resistive switching device with Ta_2O_{5-x}/TaO_{2-x} bilayer structures which can simultaneously satisfies high-density application, fast switching speed, extreme switching endurance, excellent scalability, good retention, and most importantly power-consumption criteria,[13] but the use of the precious metal Pt as the preferred electrode may cause some concerns about high costs for applicability to semiconductor processes.

In this paper, a CMOS compatible RRAM device consisting of TaN/Ta/TaO_x/TaN structure was proposed with excellent bipolar resistive switching characteristics. Aside from the benefit of low operation voltage, good endurance, satisfactory uniformity, and reliable data retention, the operation current of the TaN/Ta/TaO_x/TaN structure device can be further reduced by decreasing the value of compliance current during the set process. It is also known that both Ta buffer layer and TaN electrodes are more compatible with modern CMOS technology.

2. Experimental details

The resistive switching device consisting of TaN/Ta/TaO_x/TaN structure was fabricated on SiO_2/Si substrate. The TaN as a bottom electrode was first deposited by sputtering on SiO_2 grown on Si substrate. After that, the SiO_2 layer with a thickness of 100 nm was deposited. Then, the via holes (0.5 μm) were defined in the SiO_2 dielectric by using optical lithography and etching process. Another optical lithography and etching step were necessary to open contact window to the TaN bottom electrode. The TaO_x resistive switching layer was deposited into the via holes by sputtering using pure Ta_2O_5 target. The sputtering power was maintained at 60 W with an Ar flow of 35 sccm at working gas pressure of about 7 mTorr (1 Torr = 1.33322×10^2 Pa). Next, a thin Ta metal as a buffer layer and the TaN as a top electrode were deposited on TaO_x resistive switching layer by sputtering. Finally, the lift-off process was done to fabricate the resistive switching device. The schematic structure of

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our fabricated TaN/Ta/TaO_x/TaN resistive switching device is shown in Fig. 1(a). The microstructure of the stacked layers were investigated by cross-sectional transmission electron microscopy (TEM), the thicknesses of the TaN bottom electrode, TaO_x resistive switching layer, Ta buffer layer, and the TaN top electrode, are about 25 nm, 5 nm, 4 nm, and 30 nm, respectively. Resistive switching characteristics, such as current–voltage (I–V) characteristics, endurance and retention, were performed by using an Agilent B1500A semiconductor device analyzer at room temperature. During the measurement, the top TaN was biased, and the bottom TaN was grounded.

3. Results and discussion

To explore the influence of a Ta buffer layer on resistive switching characteristics, a control device with TaN/TaO_x/TaN structure without the Ta buffer layer was also prepared. Figure 1(b) shows the I–V curve of the control TaN/TaO_x/TaN device. By sweeping the voltage from zero to a positive voltage, the current increased abruptly at about 2.15 V, and the device switched from HRS to LRS. Unfortunately, the LRS cannot be converted to the HRS again by using a negative voltage. This result means that the TaN/TaO_x/TaN device cannot achieve stable resistive switching characteristic. In contrast, by introduced a thin Ta buffer layer into the anodic side of the device cell, the TaN/Ta/TaO_x/TaN structure device (Fig. 1(a)) demonstrated a typical bipolar resistive switching with a clear I–V hysteresis loop by using a compliance current of 100 μA during the set process. As shown in Fig. 1(c), the as-deposited fresh device shows an initial HRS, a forming process (switching the fresh device from initial HRS to LRS) is needed to trigger the reversible resistive switching behavior by using a positive voltage of about 1.25 V. After the forming process, the TaN/Ta/TaO_x/TaN device can be successfully switched from the LRS to the HRS (reset process) by using a negative voltage less than −1 V, and from the HRS to the LRS (set process) again by using a lower positive voltage of about 0.85 V.

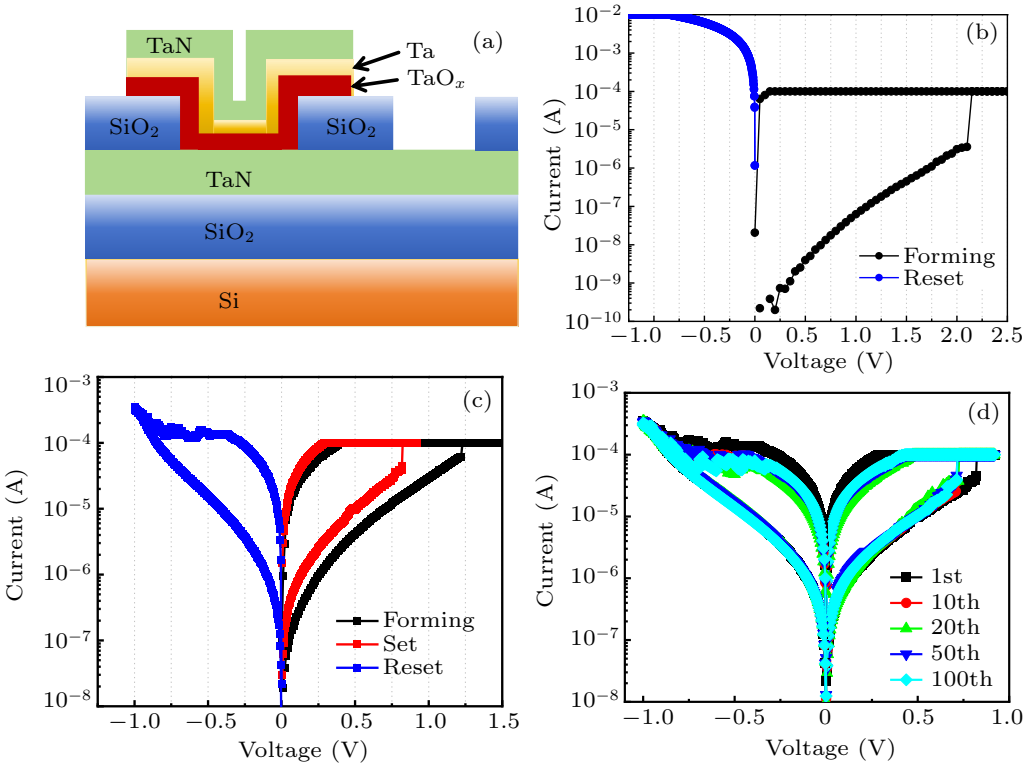


Fig. 1. (a) The schematic diagram of the fabricated TaN/Ta/TaO_x/TaN structure device. (b) The I–V curve of the TaN/TaO_x/TaN structure device. There is no significant resistive switching behavior in the device without a Ta buffer layer. (c) The I–V curve of the TaN/Ta/TaO_x/TaN device. (d) Reproducible resistive switching characteristics of the TaN/Ta/TaO_x/TaN device with 100 dc switching cycles.

This stable bipolar resistive switching characteristics of the TaN/Ta/TaO_x/TaN structure device can be attributed to the excellent ability of the thin Ta layer as oxygen getter to absorb oxygen ions from the TaO_x layer.[14–16] When a higher positive forming voltage is applied on the TaN/Ta top electrode, the oxygen ions in the TaO_x layer migrate to the Ta getter under the high forming electric field and accumulate near the TaN/Ta top electrode interface. At the same time, appropriate number of oxygen vacancies with positively charged are created in and accumulate near the cathode bottom electrode under the electric field. As a result, oxygen vacancies conductive filament channels are formed in the TaO_x film, resulting in the reversible resistive switching from the initial HRS to LRS. Vice versa, when a negative voltage is applied, some accumulated oxygen ions at the TaN/Ta top electrode interface are pushed away and migrate into the TaO_x film. As a result, the

conductive filament channels breaks and the device switches from the LRS to HRS. The reproducibility of the bipolar resistive switching in the device was also demonstrated, and several switching *I*–*V* curves are shown in Fig. 1(d). It can be seen from Fig. 1(d) that the device can successfully perform 100 resistive switching cycles in direct current (dc) sweeping mode without obvious deterioration. After 100 repeated switching cycles, the shape of the *I*–*V* curve is similar to that in the first sweep, indicating that the device can achieve good reproducible behavior.

It has been reported that the reset current of RRAM device can be controlled through the external compliance current.[10,18] The dependence of reset current on compliance current of the TaN/Ta/TaO$_x$/TaN device is shown in Fig. 2. It is clear that the compliance current strongly influences reset current, and the reset current decreases with decreasing compliance current. This result indicating that the reset current can be further reduced by using a lower compliance current during the set process. The low reset current (< 100 μA) together with the low operation voltages (< 1 V) demonstrate that the TaN/Ta/TaO$_x$/TaN device exhibits the capability of low operation power (< 0.1 mW).

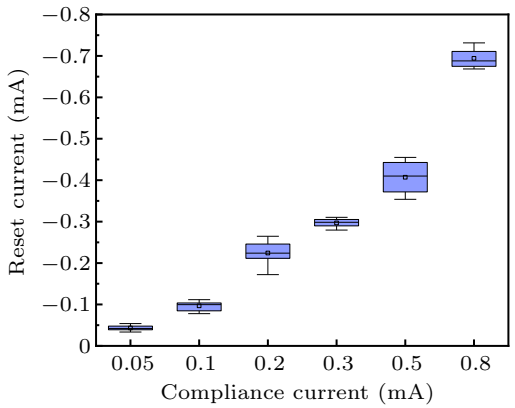


Fig. 2. Dependence of the reset current on the compliance current of the TaN/Ta/TaO$_x$/TaN device.

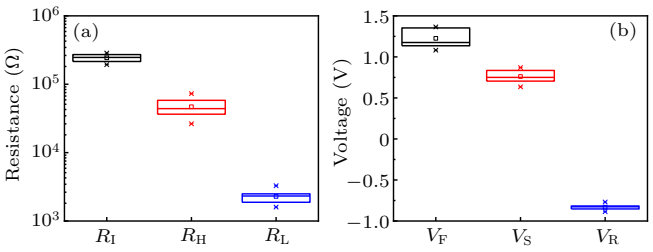


Fig. 3. Device-to-device uniformity of the TaN/Ta/TaO$_x$/TaN structure devices with 20 randomly chosen devices. (a) Distributions of the initial resistances (R_I), HRS resistances (R_H), and LRS resistances (R_L). (b) Distributions of the operation voltages for forming (V_F), set (V_S), and reset (V_R).

For RRAM devices, uniformity is also very important, the statistical measurements for device-to-device uniformity of different resistive switching parameters, including the initial resistances (R_I), HRS resistances (R_H), LRS resistances (R_L), forming voltages (V_F), set voltages (V_S), and reset voltages (V_R), were performed in 20 randomly chosen devices, as shown in Figs. 3(a) and 3(b). It is worth noting that all the aforementioned parameters exhibit narrow dispersive distributions, indicating that satisfactory uniformity can be obtained in different TaN/Ta/TaO$_x$/TaN devices.

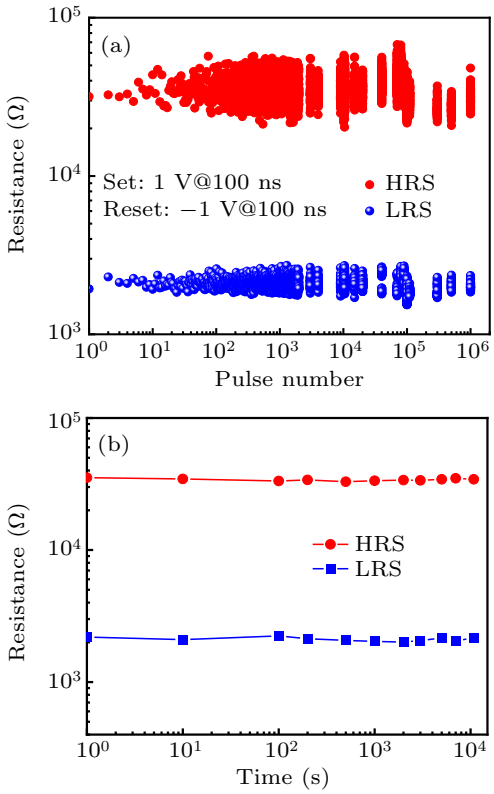


Fig. 4. (a) Endurance of the TaN/Ta/TaO$_x$/TaN device. Switching endurance over 10^6 cycles was achieved for the device under repetitive set (1 V) and reset (−1 V) pulse cycles with pulse width of 100 ns. (b) Retention characteristics of the TaN/Ta/TaO$_x$/TaN device.

Endurance testing was done by using a pulse generator to apply voltage pulse to the TaN/Ta/TaO$_x$/TaN device. Pulse of V_S and V_R were 1 V and −1 V at the pulse width of 100 ns for both set and reset. The typical endurance results of the device are presented in Fig. 4(a). The TaN/Ta/TaO$_x$/TaN device exhibits fairly stable HRS and LRS for over 10^6 switching cycles. Furthermore, the retention characteristics of the TaN/Ta/TaO$_x$/TaN device was also investigated. As can be seen from Fig. 4(b), the resistance values of both HRS and LRS exhibit little change over 10^4 seconds, indicating that the TaN/Ta/TaO$_x$/TaN device is potentially suitable for nonvolatile memory applications. Table 1 shows the comparison of resistive switching characteristics between our fabricated TaN/Ta/TaO$_x$/TaN structure devices and some previous reported tantalum oxide-based RRAM devices. Based on the experimental results shown in Table 1, our fabricated devices demonstrate satisfactory resistive switching characteristics, such as low operation voltages, low operation current, good endurance, reliable data retention, and low cost.

Table 1. Comparisons of resistive switching characteristics in this study with some previous studies.

Device structure	V_F (V)	V_S (V)	V_R (V)	I_C	Endurance cycles	Retention (s)	Cost	References
TaN/Ta/TaO_x/TaN	1.25	< 1	< -1	< 100 μA	$> 10^6$	$> 10^4$	low	this work
Pt/Ta_2O_{5-x}/TaO_{2-x}/Pt	−1.5 to −2.5	−1	2	< 30 μA	$> 10^{12}$	10 years	high	[13]
Ta/TaO_x/Pt	No	< 1	< -1	< 100 μA	$> 10^{10}$	NS	high	[14]
Pd/Ta_2O_{5-x}/TaO_y/Pd	−4 to −5	~ -0.9	1.1	> 1 mA	> 2000	> 3600 s	high	[15]
Ru/Al_2O_3/Ta_2O_5/ TaO_x/Al_2O_3/W	−4 V	~ -1.2	2	100 μA	$> 10^6$	$> 10^4$	low	[17]
W//Ir/Ta/TaO_x/TiN	2.5 V	0.9	−1.3	100 μA	NS	NS	low	[19]

NS = not specified, V_F = forming voltage, V_S = set voltage, V_R = reset voltage, I_C = compliance current

4. Conclusions

In conclusion, a TaO_x-based resistive switching memory device with excellent nonvolatile characteristics is proposed in TaN/Ta/TaO_x/TaN structure. As compared with the TaN/TaO_x/TaN structure device which cannot achieve a stable resistive switching, the TaN/Ta/TaO_x/TaN stacked structure device exhibits low operation power (< 0.1 mW), good endurance ($> 10^6$ cycles), satisfactory uniformity, and reliable data retention. Furthermore, the operation current can be further reduced by decreasing the value of compliance current during the set process. The excellent resistive switching characteristics together with the advanced CMOS compatibility of the TaN/Ta/TaO_x/TaN device promise its application in the next generation nonvolatile memory.

Acknowledgement

Project supported by the Key Research and Development Program of Gansu Province - Industrial Project (Grant No. 25YFGA005).

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