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Heterogeneous integration of silicon nitride photonics and CVD-grown WS_2 for second harmonic generation

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Silicon nitride photonics has emerged as a promising integrated optical platform due to its broad transparency window, low optical loss, and mature fabrication technology. However, the inherent centrosymmetric crystal structure of silicon nitride fundamentally restricts its applications in second-order nonlinear optical processes. Monolayer transition metal dichalcogenides, particularly tungsten disulfide (WS_2), exhibit strong second-order nonlinear responses, making them ideal candidates for nonlinear photonic applications. Herein, we demonstrate a heterogeneously integrated platform combining silicon nitride waveguides with chemical vapor deposition (CVD)-grown monolayer WS_2, enabling second harmonic generation. A specially designed silica cladding featuring gentle-slope profile on silicon nitride strip waveguides facilitates the integration of centimeter-scale WS_2 film with photonic circuits. This approach provides a robust solution for incorporating second-order nonlinearity into silicon nitride photonic systems. The demonstrated platform holds significant potential for advancing quantum networks, visible-light lasers, and integrated optical modulation/detection systems.

Keywords: silicon nitride photonics, monolayer WS_2, heterogeneous integration, second harmonic generation, integrated photonics

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1. Introduction

Second harmonic generation (SHG), a second-order nonlinear optical process in which photons interact with a nonlinear medium to generate coherent radiation at twice the fundamental frequency, plays a pivotal role in quantum networks,[1,2] integrated visible-light lasers,[3,4] and optical modulation/detection systems.[5–7] This frequency-doubling phenomenon typically requires the interaction of intense optical fields with non-centrosymmetric materials.[8]

While optical fibers enable low-loss transmission in free-space configurations, integrated photonic waveguides provide analogous functionality for on-chip light manipulation including emission, modulation, and detection.[9–11] Among various integrated platforms, silicon nitride (Si_3N_4) has become a mainstream choice due to its CMOS compatibility, broad transparency window, and ultralow propagation loss.[12–16] Nevertheless, the centrosymmetric crystal structure of Si_3N_4 fundamentally precludes second-order nonlinear interactions.

Transition metal dichalcogenides (TMDCs), particularly monolayer WS_2, offer an attractive solution with their broken inversion symmetry and large second-order susceptibility (χ^2).[17–20] The van der Waals nature of TMDCs enables damage-free heterointegration with Si_3N_4 photonic circuits, thereby introducing second-order nonlinearity to conventional dielectric platforms.[21–26]

In this work, we demonstrate a heterogeneously integrated Si_3N_4–WS_2 platform capable of SHG through evanescent-field coupling between waveguide modes and CVD-grown monolayer WS_2. Key to this integration is a gently sloping silica (SiO_2) cladding that enables damage-free transfer of centimeter-scale WS_2 film onto Si_3N_4 photonic waveguides. This scalable integration approach not only preserves material integrity but also establishes a manufacturable pathway for implementing second-order nonlinearity in Si_3N_4 photonic systems. The demonstrated platform opens new possibilities for chip-scale quantum light sources, visible-frequency combs, and nonlinear signal processing modules.

2. Results and discussion

2.1. Simulation analysis of the Si_3N_4–WS_2 heterogeneous waveguide

The optical mode characteristics of the Si_3N_4–WS_2 heterostructure waveguide were numerically analyzed via finite-element simulations. The Si_3N_4 waveguide dimensions were optimized to 1500 nm (width) ×150 nm (height), with t denot-

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ing the SiO_2 cladding layer thickness. Due to the centrosymmetric crystal structure of Si_3N_4, second-order nonlinearity is exclusively introduced by the monolayer WS_2. The second-order nonlinear polarization density $\boldsymbol{P}^{(2)}$ relates to the local electric field $\boldsymbol{E}$ through: $\boldsymbol{P}^{(2)} = \varepsilon_0 \chi^{(2)} : \boldsymbol{E}\boldsymbol{E}$, where ε_0 is the vacuum electric permittivity and $\chi^{(2)}$ represents the second-order nonlinear susceptibility. For a given ε_0 and $\chi^{(2)}$, $\boldsymbol{P}^{(2)}$ exhibits a quadratic dependence on $\boldsymbol{E}$. To quantify the light-matter interaction strength, we calculated the optical confinement factor Γ in the WS_2 layer[27,28]

$$\Gamma = \frac{\int_{WS_2} \varepsilon_{WS_2} \left|E_{\parallel}\right|^2 \mathrm{d}S}{\int_{Si_3N_4} \varepsilon_{Si_3N_4} \left|E_{\parallel}\right|^2 \mathrm{d}S + \int_{SiO_2} \varepsilon_{SiO_2} \left|E_{\parallel}\right|^2 \mathrm{d}S + \int_{air} \varepsilon_{air} \left|E_{\parallel}\right|^2 \mathrm{d}S + \int_{WS_2} \varepsilon_{WS_2} \left|E_{\parallel}\right|^2 \mathrm{d}S},$$

where ε denotes the position-dependent permittivity and $\left|E_{\parallel}\right|$ corresponds to the in-plane electric field component.

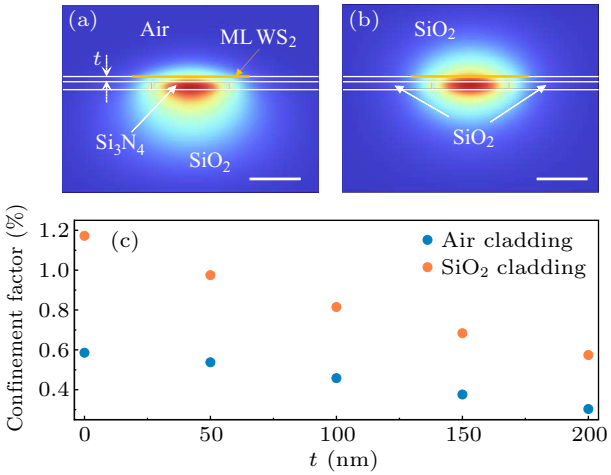


Fig. 1. Optical modes analysis in the Si_3N_4 WS_2 heterostructure waveguides. (a)–(b) Cross-sectional electric field profiles of the fundamental TE mode at 1580 nm with (a) air-clad and (b) SiO_2-clad configurations ($t = 100$ nm). (c) Optical confinement factor Γ in monolayer WS_2 versus t. Scale bars: 1 μm in panels (a) and (b).

In the simulation we do not consider the absorption of the material: the refractive index of Si_3N_4 is set to be 2.0, the refractive index of SiO_2 is set to be 1.44, the thickness of WS_2 is set to be 1 nm, and the refractive index is set to be 4.5.[29] Figures 1(a) and 1(b) show the simulated electric field profiles of the fundamental transverse electric (TE) mode at 1580-nm wavelength with different cladding configurations: (a) air-clad and (b) SiO_2-clad structures at $t = 100$ nm. Cross-sectional field distributions reveal enhanced optical confinement in the WS_2 layer under SiO_2 capping. Quantitative analysis of the confinement factor versus cladding thickness t (Fig. 1(c)) demonstrates that depositing an SiO_2 overlayer increases Γ by more $\sim 75\%$ compared to the air-clad configuration. This improved mode overlap directly enhances the second harmonic generation efficiency through quadratic dependence on $|E|$ at the WS_2-waveguide interface.

2.2. Heterogeneous integration scheme of Si_3N_4 photonics and CVD-grown WS_2

The schematic of the heterogeneous integration process involving Si_3N_4 photonics and CVD-grown monolayer WS_2 is illustrated in Fig. 2. This process can be categorized into three main steps: (i) the fabrication of Si_3N_4 photonic chips (Fig. 2(a)), (ii) the preparation of centimeter-sized monolayer WS_2 (Fig. 2(b)), and (iii) the heterogeneous integration of Si_3N_4 photonic chips with WS_2 (Fig. 2(c)).

The Si_3N_4 photonic chips were fabricated using a well-established silicon photonic chip processing technique. Initially, an Si_3N_4 thin film was deposited on an Si/SiO_2 wafer via low-pressure chemical vapor deposition (LPCVD). Subsequently, a photoresist layer was spin-coated onto the wafer, and the waveguide pattern was defined using photolithography. The Si_3N_4 layer was then etched through an inductively coupled plasma-reactive ion etching (ICP-RIE) process, followed by the removal of residual photoresist to obtain the desired Si_3N_4 waveguide. Figure 3 presents a scanning electron microscope (SEM) image of the cross-section of the bare Si_3N_4 waveguide, revealing a waveguide width of 1500 nm and a height of 150 nm, which aligns with the simulation parameters utilized in Fig. 1. To minimize scattering losses during light transmission, an SiO_2 layer of a specific thickness was deposited over the bare Si_3N_4 waveguide using plasma-enhanced chemical vapor deposition (PECVD). Finally, the Si_3N_4 chip was annealed at 1250 °C to smoothen the SiO_2 surface and form a gently sloping SiO_2 cladding around the Si_3N_4 waveguide.

For the synthesis of monolayer WS_2, centimeter-scale continuous WS_2 monolayers were first grown on a sapphire substrate using a chemical vapor deposition (CVD) method. Subsequently, a polymethylmethacrylate (PMMA) layer was spin-coated onto the WS_2/sapphire substrate, and a thermal release tape (TRT) was laminated onto the PMMA/WS_2/sapphire stack. The PMMA/WS_2 stack was then peeled off the sapphire substrate by immersing it in a KOH solution, as depicted in Fig. 2(b).

The TRT/PMMA/WS_2 stack was transferred onto the prefabricated Si_3N_4 photonic chip (from Fig. 2(a)), and the assembly was heated to 120 °C to release the TRT. The chip was subsequently treated with acetone and isopropanol to remove the PMMA layer, resulting in the final Si_3N_4–WS_2 heterogeneous photonic chip, as shown in Fig. 2(c).

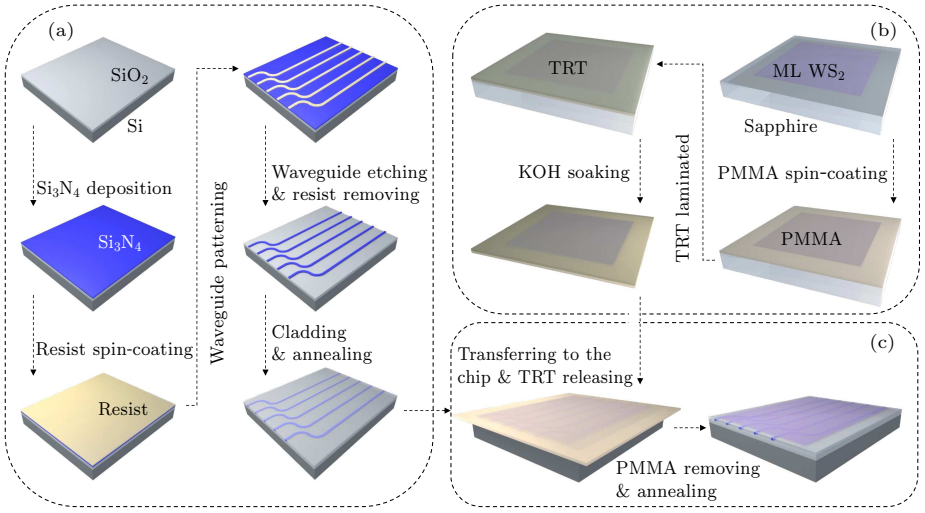


Fig. 2. Heterogeneous integration scheme of Si_3N_4 photonics and CVD-grown WS_2. (a) Fabrication of Si_3N_4 photonic chips: deposition of an Si_3N_4 film onto an Si/SiO_2 substrate, spin-coating of photoresist, definition of the Si_3N_4 waveguide pattern via photolithography, waveguide etching, removal of photoresist, deposition of an SiO_2 cladding layer, and annealing at 1250 °C. (b) Preparation of monolayer WS_2: growth of centimeter-scale monolayer WS_2 on a sapphire substrate using CVD, spin-coating of PMMA onto the WS_2/sapphire substrate, lamination of a TRT onto the PMMA/WS_2/sapphire stack, and subsequent peeling of the PMMA/WS_2 stack from the sapphire substrate by immersion in a KOH solution. (c) Heterogeneous integration of Si_3N_4 photonic chips and WS_2: transfer of the TRT/PMMA/WS_2 stack onto the pre-fabricated Si_3N_4 photonic chip, heating of the assembly to 120 °C to release the TRT, and removal of residual PMMA using acetone-isopropanol to obtain the final Si_3N_4–WS_2 heterogeneous photonic chip.

The SiO_2 cladding surrounding the Si_3N_4 strip waveguide serves to facilitate material transfer. However, as quantitatively validated in Fig. 1(c), its thickness results in a reduction in the optical confinement factor. The minimum thickness of the deposited SiO_2 must be sufficient to prevent damage to the 2D material after integration with the waveguide. In our experiments, the thickness of the SiO_2 cladding was approximately 100 nm, which can be precisely controlled by adjusting the process time of PECVD.

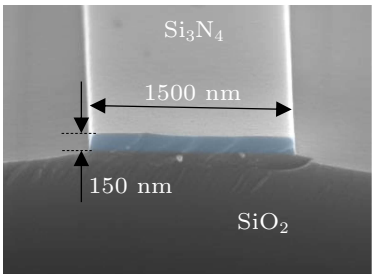


Fig. 3. The SEM image of the cross-section of the bare Si_3N_4 waveguide reveals a waveguide width of 1500 nm and a height of 150 nm.

During the subsequent annealing process, the temperature was maintained at 1250 °C, slightly above the glass transition temperature of SiO_2 (1202 °C),[30] for a duration of approximately 12 hours. This high-temperature annealing process enables self-smoothing of the SiO_2 cladding through surface tension, resulting in a gently sloping cladding on the surface of the Si_3N_4 waveguide. The atomic force microscopy (AFM) image of the waveguide cross-section (Fig. 4) clearly illustrates the gently sloping topography on the waveguide's top surface. It should be noted that, for modeling simplicity, the simulation in Fig. 1 assumes a flat SiO_2 cladding on the waveguide, which differs slightly from the actual fabricated device. However, this discrepancy does not affect the qualitative analysis of the problem.

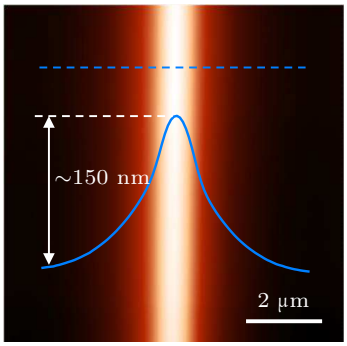


Fig. 4. The AFM image of the waveguide cross-section reveals the gently sloping topography on the top surface of the waveguide. The blue curve in the illustration represents the height variation along the dashed blue line, indicating a height difference of approximately 150 nm.

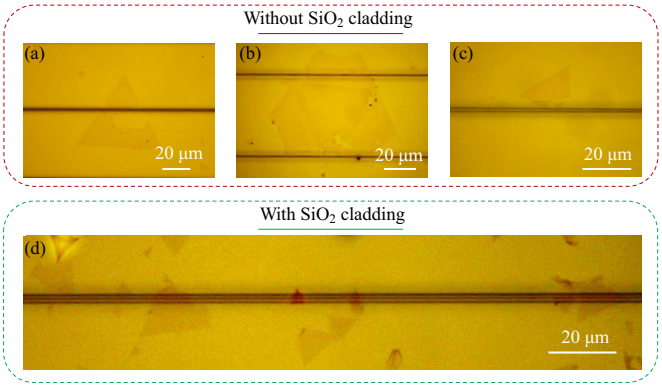


Fig. 5. Optical microscope images of Si_3N_4 waveguides without SiO_2 cladding (a)–(c) compared to those with a gently sloping SiO_2 cladding (d) after integration with WS_2. As shown in (a)–(c), the 150-nm rectangular step between the upper surface of the bare Si_3N_4 waveguide and the SiO_2 substrate layer causes wrinkling and damage to the layered WS_2 near the waveguide step during direct integration. Consequently, successful integration of WS_2 with the bare Si_3N_4 waveguide cannot be achieved under these conditions.

From Fig. 3, it can be observed that a 150 nm-height step exists between the upper surface of the Si_3N_4 waveguide and the SiO_2 substrate. Direct integration of layered WS_2 onto the bare Si_3N_4 waveguide would introduce significant stress at the step edge, leading to material fracture in the integrated 2D material (Figs. 5(a)–5(c)). To address this issue, we fabricated a gently sloping SiO_2 cladding on the Si_3N_4 waveguide using the aforementioned method. This modification effectively prevents mechanical damage to the two-dimensional (2D) material at both waveguide edges after integration (Fig. 5(d)), demonstrating the necessity of the preparation SiO_2 cladding layer.

2.3. Characterization of the Si_3N_4–WS_2 heterogeneous photonic chip

Figure 6(a) displays the fabricated Si_3N_4–WS_2 heterogeneous photonic chip, where the yellowish region to the left of the white dashed line represents the centimeter-scale continuous monolayer WS_2. A WS_2-covered area was selected for photoluminescence (PL) characterization, as shown in Fig. 6(b). The white dashed lines in Fig. 6(b) mark the positions of the Si_3N_4 waveguides. Monolayer WS_2, being a direct bandgap semiconductor, exhibits strong PL under excitation by a 405-nm semiconductor laser. Figure 6(c) presents the PL spectrum measured at the blue dot in Fig. 6(b), with a PL peak observed at approximately 630 nm, further confirming the monolayer nature of the integrated WS_2.[31]

Figure 6(d) shows a dark-field optical microscope image of a monolayer WS_2 region without an underlying waveguide pattern on the heterogeneous chip. Multiple oriented grain boundaries are visible within the continuous monolayer WS_2, indicating that the second harmonic signal collected from the Si_3N_4–WS_2 heterogeneous waveguide arises from the average orientation of WS_2 domains with varying crystal orientations.

Figures 6(e) and 6(f) present dark-field optical microscope and false SEM image of the Si_3N_4–WS_2 heterogeneous waveguides, respectively. The area below the red dashed line in Fig. 6(e) is the area covered by WS_2, and the purple area in Fig. 6(f) is the WS_2 area. The surface of the Si_3N_4 strip waveguides appears smooth, owing to the deposition of an SiO_2 layer and subsequent annealing at 1250 °C. This ensures robust adhesion of WS_2 to the waveguide surface without the breakage issues observed in Figs. 5(a)–5(c).

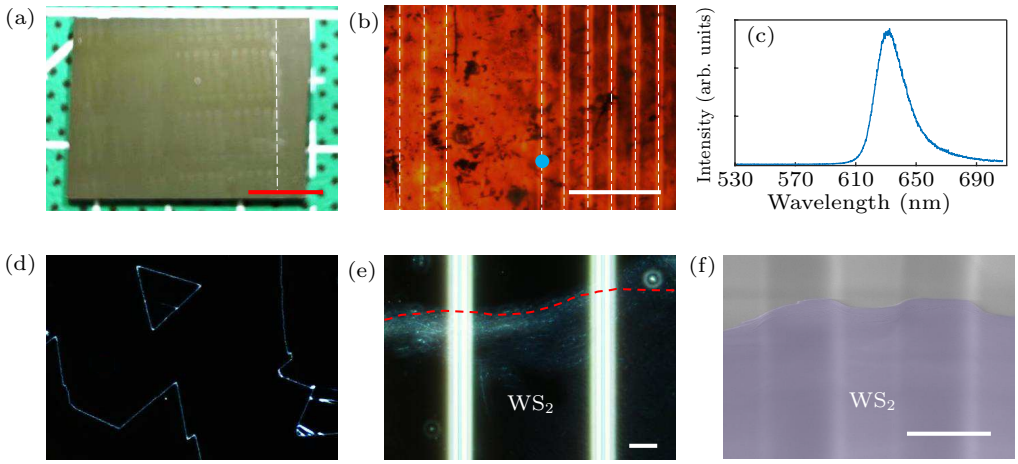


Fig. 6. Characterization of the Si_3N_4–WS_2 heterogeneous photonic chip. (a) Optical image of the Si_3N_4–WS_2 heterogeneous chip, showing centimeter-scale continuous monolayer WS_2 on the left side of the white dashed line. (b) PL image of a selected WS_2-covered region on the chip, with white dashed lines indicating the positions of the Si_3N_4 waveguides. (c) PL spectrum measured at the blue dot marked in panel (b), exhibiting a peak at approximately 630 nm, consistent with the characteristic PL spectrum of monolayer WS_2. (d) Dark-field optical microscopy image of a monolayer WS_2 region without an underlying waveguide pattern on the heterogeneous chip. (e)–(f) Dark-field optical microscopy image (e) and false SEM image (f) of the Si_3N_4–WS_2 heterogeneous waveguides. Scale bars: (a) 0.5 cm, (b) 100 μm, (d) 20 μm, (e) 10 μm, (f) 2 μm.

2.4. SHG in the Si_3N_4–WS_2 heterogeneous waveguide

The experimental setup for characterizing the Si_3N_4–WS_2 heterogeneous waveguide is illustrated in Fig. 7(a). A femtosecond (fs) laser pulse with a central wavelength of approximately 1580 nm (Fig. 7(b)) was served as the pump source, with a repetition rate of 100 MHz, a pulse width of 110 fs and an output power of 10 mW. The fs pulse was passed through a polarization controller (PC) and coupled into the Si_3N_4–WS_2 heterogeneous waveguide using a lensed fiber.[32] The coupling efficiency from the fiber to the waveguide was about 5%.[33] The output signal from the waveguide was collected by a single-mode fiber and analyzed using an optical spectrum analyzer (OSA) capable of detecting single photons. The relative position between the optical fiber and the chip was precisely controlled using a displacement stage to maximize the coupling efficiency under the given experimental conditions. Since 1580-nm light is not visible, a 650-nm red light was used as an auxiliary alignment tool during the coupling adjustment between the lensed fiber and the heterogeneous waveguide (Fig. 8).

Although previous studies have demonstrated second-harmonic generation (SHG) in Si_3N_4 waveguides through in-

terfacial effects[34] or intrinsic second-order nonlinearity,[35] no detectable SHG signal was observed in our experiments for an Si_3N_4 waveguide without WS_2 integration, as shown by the black curve in Fig. 7(c). In contrast, after integrating monolayer WS_2, the heterogeneous waveguide exhibited a pronounced SHG signal at approximately 790 nm under fs laser pumping (blue curve in Fig. 7(c)). In fact, the observed second harmonic signal originated from WS_2, and the Si_3N_4 waveguide provides an on-chip optical propagation platform.

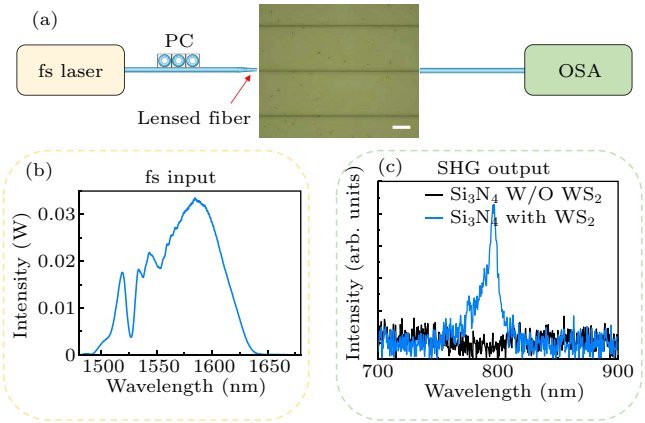


Fig. 7. SHG in the Si_3N_4–WS_2 heterogeneous waveguide. (a) Schematic diagram of the experimental setup for SHG testing of the Si_3N_4–WS_2 heterogeneous waveguide. A fs laser at 1580 nm serves as the pump source, which passes through a polarization controller (PC) and is coupled into the on-chip waveguide using a lensed fiber. The second-harmonic signal generated in the waveguide is coupled out through a single-mode fiber and detected by an optical spectrum analyzer (OSA). The scale bar in the waveguide optical microscope image is 20 μm. (b) Spectrum of the input fs laser pulse. (c) Spectra of the generated second-harmonic signal for an Si_3N_4 waveguide without WS_2 (black curve) and an Si_3N_4 waveguide integrated with WS_2 (blue curve).

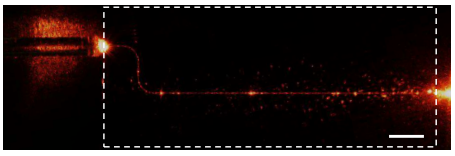


Fig. 8. Optical microscope image of the coupling between a lensed fiber and an Si_3N_4–WS_2 heterogeneous waveguide. Visible red light (650 nm) was employed for precise alignment, enabling optimized coupling efficiency at the fiber-waveguide interface. The white dashed box indicates the area covered with monolayer WS_2, while the red portion where the red light passes through represents the waveguide location. Scale bar: 200 μm.

3. Conclusions and perspectives

In summary, we have demonstrated a heterogeneous integration scheme combining Si_3N_4 photonics with CVD-grown monolayer WS_2, enabling the realization of SHG nonlinear optical processes on the Si_3N_4–WS_2 platform. By depositing SiO_2 and applying high-temperature annealing, a gently sloping and smooth SiO_2 cladding was formed on the surface of the bare Si_3N_4 strip waveguide. This approach facilitated the integration of centimeter-scale monolayer WS_2 with Si_3N_4 photonic chips without the need for expensive polishing equipment, providing a simple and practical solution for the heterogeneous integration of Si_3N_4 photonics and monolayer TMDCs.

While this work serves as a preliminary demonstration of second-order nonlinear optics on an Si_3N_4-TMDC platform, the device performance could be further optimized through inverse design methodologies,[36–39] thereby extending its application scope. Additionally, this integration scheme is scalable and applicable to other TMDCs, offering broad potential for applications in quantum networks, visible light lasers, optical modulation, and detection modules. The batch fabrication of Si_3N_4-based heterogeneously integrated platforms with second-order nonlinearity holds significant promise for advancing integrated photonics.

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