

RF detection of split-gate modes in Si-MOS quantum dots

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RF detection of split-gate modes in Si-MOS quantum dots

Ning Chu(楚凝)[1,2], Sheng-Kai Zhu(祝圣凯)[1,2], Ao-Ran Li(李傲然)[1,2], Chu Wang(王储)[1,2], Wei-Zhu Liao(廖伟筑)[1,2], Gang Cao(曹刚)[1,2,3], Hai-Ou Li(李海欧)[1,2,3,†], and Guo-Ping Guo(郭国平)[1,2,3,4]

[1] *CAS Key Laboratory of Quantum Information, University of Science and Technology of China (USTC), Hefei* 230026, *China*
[2] *CAS Center for Excellence in Quantum Information and Quantum Physics, University of Science and Technology of China, Hefei* 230026, *China*
[3] *Hefei National Laboratory, University of Science and Technology of China, Hefei* 230088, *China*
[4] *Origin Quantum Computing Company Limited, Hefei* 230088, *China*

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Radio frequency (RF) reflectometry is an effective and sensitive technique for detecting charge signal in semiconductor quantum dots, and its measurement bandwidth can reach the MHz level. However, in accumulation mode devices, the presence of parasitic capacitance makes RF reflectometry more difficult. The universal approach is relocating the ion implantation region approximately 10 μm from the center of the single-electron transistor (SET) and optimizing the design of the accumulation gates. But, this method puts forward more stringent requirements for micro-nano fabrication processing. Here, we propose a split-gate structure that enables RF reflectometry when the ion-implanted region and the ohmic contact are farther from the SET center. In Si-MOS devices, we employ a split-gate structure to achieve RF detection, with the ion-implanted region located 150 μm away from the center of the SET. Within an integration time of 140 nanoseconds, we achieved a readout fidelity exceeding 99.8% and a detection bandwidth of over 2 MHz. This is an alternative solution for micro-nano fabrication processing that cannot achieve ion implantation areas closer to the center of the chip, and is applicable to various silicon-based semiconductor systems.

Keywords: silicon-based quantum computing, Si-MOS, radio-frequency readout

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1. Introduction

Quantum computing holds the potential to surpass classical computing. Among the various systems capable of realizing quantum computing, the confinement of electron spin in semiconductor quantum dots presents an appealing platform for quantum information processing.[1–3] Specifically, spin qubits in silicon are regarded as strong contenders for realizing large-scale quantum processors due to their small qubit size, ability for local and global control,[4] CMOS compatibility,[5–8] long coherence times,[9] weak hyperfine interactions, and the possibility of operating above 1 K.[10,11] Recently, single-qubit gates with fidelity exceeding 99.9%[12] and two-qubit gates with fidelity up to 99%[13–15] have been demonstrated, marking significant progress in the implementation of quantum error correction protocols.[16,17]

In silicon-based semiconductor spin qubits, single electron transistor (SET) is crucial device for charge readout. DC detection[18–21] of SET is widely used because of its simple circuit, minimal impact on qubits, and ability to mitigate some high-frequency noise by its low-pass filter characteristic. However, the major drawback of DC detection lies in limited measurement bandwidth, typically only a few thousand hertz, attributed to the presence of hundreds of pF parasitic capacitance in the DC line, high input impedance of the amplifier and hundreds of kilohm resistance of the SET. This measurement rate is significantly slower compared to the single qubit manipulation rate, which operates at the nanoseconds level,[22,23] and the exchange coupling between qubits, which can reach tens of megahertz.

To enhance the readout bandwidth, the conventional low-bandwidth DC measurement has gradually been supplanted by RF reflection measurement,[14,24–29] where transient changes can be tracked using reflectometry. In order to match the impedance of the SET with the impedance in the transmission lines, a tank circuit consisting of an inductor and a parasitic capacitor is used to form a resonator. This tank circuit redirects the hundreds of pF parasitic capacitance of the DC lines, which limits the readout bandwidth, to the around 1-pF ground capacitance after the inductor. The bandwidth of the resonator is determined by the parasitic capacitance originating from the chip and printed circuit board (PCB), as well as the impedance of the SET. The RF reflectometry method enables a detection bandwidth of several MHz, which is three orders of magnitude higher than that of DC detection. Therefore, the radio-frequency reflectometry method is an ideal approach for rapid measurements and can effectively enhance readout fidelity.

In depletion-mode devices, there is no direct capacitive coupling between the two-dimensional electron gas (2DEG)

†Corresponding author. E-mail: haiouli@ustc.edu.cn

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and the gate, thus preventing leakage.[30,31] Consequently, RF readout possesses inherent advantages in depletion-mode devices. However, for accumulation mode devices like Si-MOS, Si/SiGe, when the RF circuit connects to the ohmic contact, named Ohmic approach,[28,32–34] the 2DEG beneath the electrode acts a leakage channel for the RF signal, as shown in Fig. 1(b). The capacitor between the lead and the 2DEG C_g enables the RF signal to pass through the low-impedance ground capacitance C_p and the line resistance on the PCB R_b,[34] rendering it challenging to effectively track the transient change in SET impedance. Hence, it is crucial to meticulously design the device structure to minimize the leakage of RF signals. In response to this problem, many research groups have made design improvements to the accumulation mode device. The most commonly used one is to extend the ion implantation region to a position 10 μm away from the center of the SET, reduce the overlap area between the ion implantation region and the lead, and shorten the length of the lead. These design modifications are intended to reduce signal leakage caused by parasitic capacitance and solve the dissipation loss caused by high impedance in the measurement circuit. However, this method has very high requirements for micro-nano fabrication processing, and it is prone to leakage current when the ion implantation region is located too close to the SET center.

In this study, we enhanced our structure by dividing the previous single-layer lead electrode into two layers: the lead gate and the splitting accumulation gate, named split-gate approach,[34,35] as shown in Fig. 1(c). The characteristic of this design is that it does not need to extend the ion implantation region to the center of the chip, which has a very positive significance for the large-scale expansion of qubits. We employed a split-gate structure in Si-MOS to achieve RF detection with the ion implantation region situated more than 150 μm from the SET. This approach allowed us to detect the charge stability diagram of quantum dots using RF-SET. When we adjust the tunneling of electrons between the quantum dot and the reservoir at a frequency of 145.7 kHz, we can measure this random telegraph signal (RTS) and achieve a charge readout fidelity of 99.86% within an integration time of 140 ns. Moreover, this structure can also be applied to the Ge/SiGe system.

2. Device

We fabricated a highly tunable double quantum dots device on a 70-nm ^{28}Si substrate using split-gate approach, with a residual ^{29}Si concentration of 60 ppm, as shown in Fig. 1(a). The chip is placed inside a dilution refrigerator with a base temperature of 20 mK, and its circuit layout is shown in Sup-Fig. S1 in supplementary note 1. Figure 1(b) is a schematic diagram of the RF reflection using the Ohmic approach when the gate structure of the sample is not optimized, which corresponds to the single quantum dot sample we measurement before. Its lead extends from the ion implantation region to the vicinity of the SET, and the tank circuit is connected to the source. It has been proven in experiments and simulations that the capacitance C_g between the lead and the 2DEG will cause the leakage of the RF signals in this approach. In this study, we propose a split-gate approach in Si-MOS as shown in Fig. 1(c), which divides the previous lead into two parts: the accumulation gate and the lead. The two gates are connected by a small contact area and a narrow contact width, and the RF signal is input from the accumulation gate. A minimal overlap area between the lead and the accumulation gate ensures that the RF signal does not leak through the C_{A-L} capacitive channel, as the value of C_{A-L} is proportional to the overlap area between these two gates. Additionally, since the voltage on the lead is kept off during RF measurements, RF leakage through the resistive channel R_{A-L} is effectively prevented. This can both initialize free electrons and suppress the leakage of RF signals. Figure 1(d) presents a cross-sectional view of the split-gate structure.

As shown in Fig. 1(a), we connect the RF circuit to the accumulation gate AL_1 of QD_1 as RF-SET to detect QD_2 below. The RF signal is transmitted to the quantum dot through the capacitance (C_g) between the accumulation gate and the 2DEG beneath it, with varying RF signal amplitudes reflected back according to the different states of the electrons in quantum dot. As shown in Figs. 1(b) and 1(c), in RF reflection circuit, C_m and C_t are voltage-controlled capacitors;[29,36] the former is used for impedance matching, and the latter is used as a tuning capacitor to adjust the resonant frequency and sensitivity of the circuit (supplementary note 2).

In both methods, capacitive coupling between the 2DEG and the leads constitutes the primary leakage channel. There are two pathways for RF signal leakage via the leads: one through the line resistance R_b to the input line of the gate voltage V_{lead} (serving as the RF ground), and the other through the parasitic capacitance C_p from all metal components on the sample side (including gates, bond wires, bond pads, and PCB traces) to ground. Therefore, in the split-gate approach, we employ two strategies to suppress leakage. The first is to increase the resistance R_{lead} between the lead and the accumulation gate. The second is to introduce an additional resistance R_s on the PCB in the line connected to the ohmic contacts, as illustrated in Fig. 1(c). For detailed gate structure morphology and manufacturing process, please see supplementary note 4.

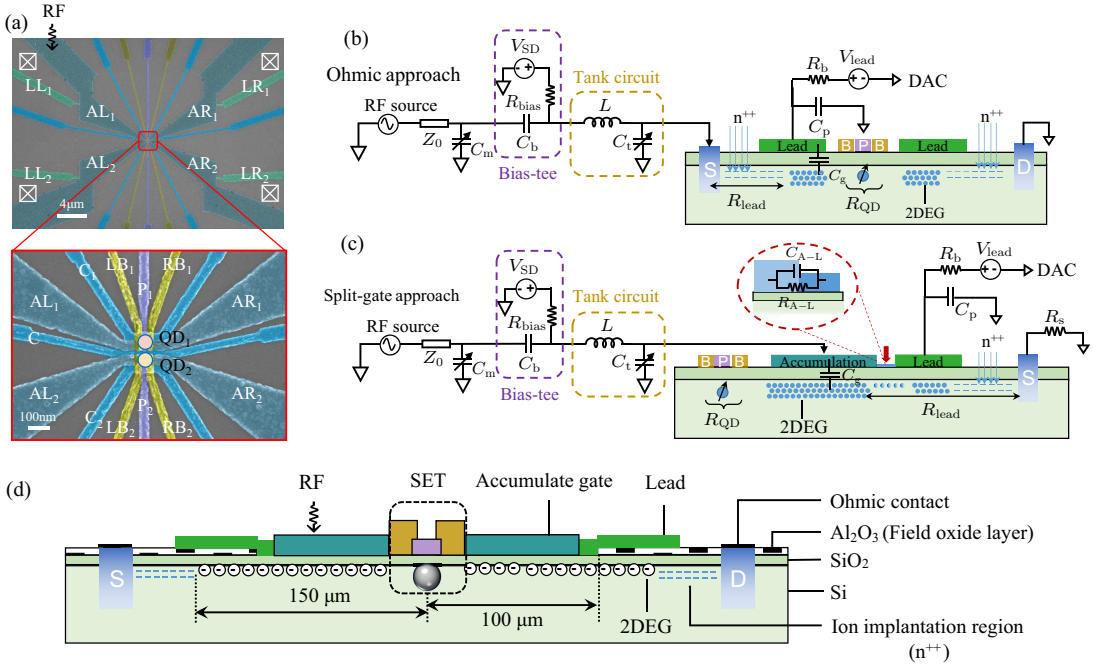


Fig. 1. (a) A false-colored SEM image of an Si-MOS device. In order to facilitate mutual detection, we made a symmetrical design. The subscripts 1 and 2 indicate that the upper and lower sides have exactly the same structure. The two quantum dots, QD_1 and QD_2, locate under gates P_1 and P_2 respectively (purple), and barriers are formed under the LB_1, LB_2, RB_1, and RB_2 gates (yellow). Confine gates C_1, C_2, and C are used to control the lateral size of quantum dot. Previous large lead gate is divided into two layers: lead gate (LL and LR) and splitting accumulation gate (AL and AR). In the test, we utilize the upper quantum dot as SET to detect the signal from the lower quantum dot, with the RF circuit connected to the AL_1 gate. (b) Ohmic approach. In the ohmic design, the bias tee (purple dashed line) and tank circuit (yellow dashed line) are implemented on the PCB. $R_{\rm lead}$ represents the resistance of the 2DEG accumulated beneath the lead gate, which dissipates the RF signal. And $C_{\rm g}$ represents the capacitance between the lead electrode and 2DEG, which causes the leakage of RF signal. $C_{\rm p}$ is the parasitic capacitance from the bonding wire and between the accumulation gate to the ground plane of PCB. $R_{\rm b}$ is a resistor on the PCB to prevent RF signals from leaking into the DC line. The matching capacitor $C_{\rm m}$ can match the RF circuit to the SET with high resistance. n^{++} is ion implantation region. (c) Split gate approach. The RF signal is applied to the accumulation gate. The lead and accumulation gates are divided into two parts, reducing their overlap to minimize the resistance $R_{\rm A-L}$ and capacitance $C_{\rm A-L}$. The overlap region has a length of 0.1 μm and a width of 0.3 μm. For convenience, $R_{\rm A-L}$ is included in the lead-to-Ohmic contact resistance $R_{\rm lead}$. (d) Cross-sectional view of the split-gate structure. The ion implantation region is located 150 μm from the center of the SET. The Al_2O_3 layer has a thickness of 30 nm, and the aluminum oxide in the central area of 100 μm by 100 μm of the chip has been etched away.

3. Simulation

In order to further illustrate the effect of the split-gate structure in RF reflection, we simulated the Ohmic approach and the split-gate approach, which can understand the improvement of this structure more intuitive and provide guidance for the design of specific parameters in samples. We estimate various parameters of the two structures and measurement circuits as inputs for our simulation model, including $R_{\rm b}$ (50 kΩ), $C_{\rm p}$ (0.2 pF), $C_{\rm b}$ (100 nF), $R_{\rm bias}$ (5.1 kΩ), $R_{\rm SET}$ (625 kΩ, 500 kΩ). Other values used in the simulations, as well as the parameter variation ranges, are provided in Table 1 of the supplementary. The most critical aspect of RF structure design is the impedance matching throughout the entire circuit; only by achieving this can the RF-SET exhibit the maximum variation in signal amplitude. Through circuit simulations of the Ohmic approach and the split-gate approach, we obtained the RF reflection signal S_{21} under different conditions. According to different parameter ranges, we can analyze the influence of various electronic components and chip structures on impedance matching. When impedance matching is achieved, the S_{21} at the resonance frequency will exhibit the minimum reflection signal. In the simulations, we need to account for the variation in the SET impedance caused by electron tunneling in the quantum dot. Since we employ Elzerman readout,[37] tunneling occurs when the electron is spin-up, whereas no tunneling occurs when the electron is spin-down. Based on the experimentally observed behavior in our sample, we define the SET resistance as 625 kΩ and 500 kΩ, corresponding to the spin-up and spin-down states of the electron in the quantum dot, respectively. These resistance values also correspond to the high and low levels of the RTS signal.[38,39] In the simulation, we define the difference in the SET reflection coefficients under impedances of 625 kΩ and 500 kΩ, $|\Delta S_{21}|$, as the signal amplitude. When impedance matching occurs, the magnitude of $|\Delta S_{21}|$ reaches its maximum. For specific simulation details, please refer to supplementary note 2.

We first model the circuit presented in Fig. 1(b). In the Ohmic approach, impedance matching is achieved only when the capacitance $C_{\rm g}$ between the leads and the 2DEG is zero. However, this represents an ideal scenario that necessitates the lead to have zero area. As the lead area increases, even a small capacitance $C_{\rm g}$ of 0.001 pF can cause a significant reduction in the depth of $|\Delta S_{21}|$ dip, resulting in impedance mismatch and decreased sensitivity, as shown in Fig. 2(a). Moreover, the offset caused by RF signal leakage is too large to be cor-

rected, even with the use of C_m and C_t. The roles of C_m and C_t are to compensate for impedance matching in the system, particularly in Si-MOS, where the over-coupled state is adjusted to achieve impedance matching. However, the leakage current caused by C_g cannot be compensated by adjusting the S_{21} matching. Therefore, it is crucial to optimize the design through the Ohmic method to minimize C_g within the circuit. The most critical point is to shorten the distance between ion implantation region and SET, which requires higher micro-nano fabrication technology. Some research groups have achieved RF reflection readout in the Si/SiGe system using this approach.[28,32,33]

For the split-gate approach, since we connect the RF reflection circuit to the accumulation gate AL_1, C_g no longer acts as a leakage channel but instead serves as a coupling channel. As illustrated in Fig. 2(b), the range of C_g allowing for impedance matching significantly expands, and C_g within the wide range of 0.1 pF to 5 pF no longer affects the depth of the resonance dip. Perfect impedance matching can be achieved through adjustments of C_m and C_t. Consequently, this split-gate approach does not require reducing C_g as is necessary in the Ohmic approach. However, this approach may lead to leakage from the lead, specifically through the capacitive channel C_{A-L} and the resistive channel R_{lead} between the lead and the accumulation gate, which need to be suppressed. Therefore, in addition to reducing the overlapping area between the lead and the accumulation gate, we can also avoid applying voltage to the lead during RF measurements to prevent the accumulation of 2DEG beneath the lead, thereby further suppressing leakage through the lead. In this design, the lead gate is solely utilized for DC measurement and the injection of free electrons.

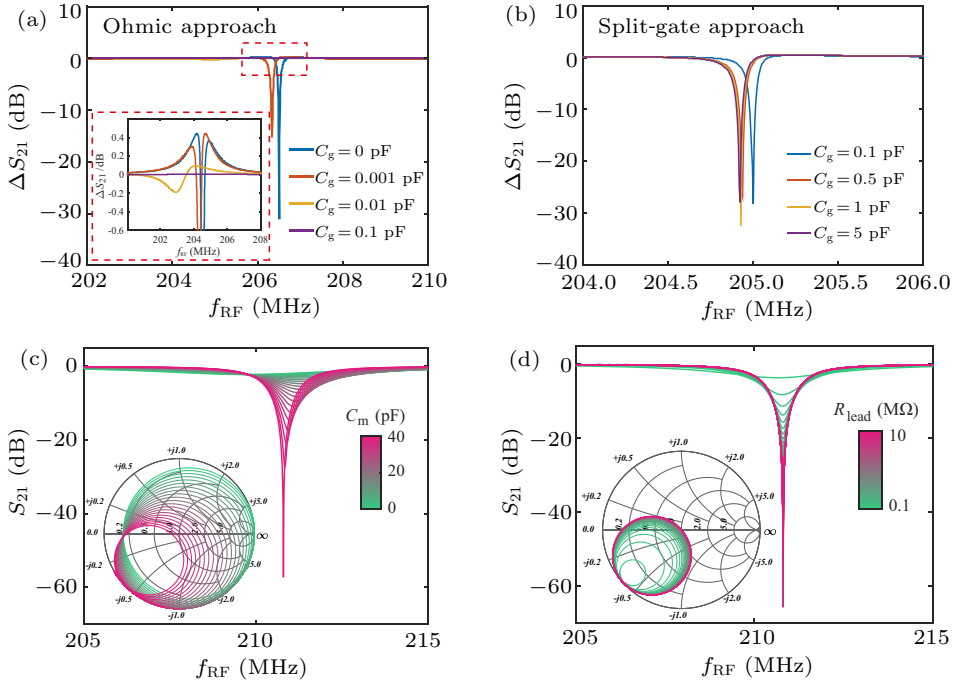


Fig. 2. (a) In the Ohmic approach, the signal amplitude measured is a function of RF frequency f_{RF}, with lines of different colors representing various C_g values. When C_g is 0 pF, the reflection signal exhibits a dip at a certain frequency, called resonant frequency f_{res}, indicating impedance matching at this point. As C_g increases, the dip rapidly disappears, suggesting that higher C_g values lead to signal leakage in this approach. (b) In the split-gate approach, C_g is a coupling channel rather than a leakage channel. And the impedance matching is very tolerant to the value of C_g, and the impedance matching can be achieved from 0.1 pF to 5 pF. (c) In the simulation of the split-gate structure, the adjustment of C_m for impedance matching is examined. Through linear adjustment of C_m, the system coupling can be transitioned from an over-coupled state (green) to impedance matching (pink). Inset: The corresponding Smith circle can be adjusted to pass through the origin by varying C_m. (d) In our simulation, we generated 121 logarithmically spaced data points for R_{lead} to explore the condition of impedance matching. Effective suppression of RF leakage from the lead direction occurs only when R_{lead} is sufficiently large ($R_{lead} > 10 \cdot R_{QD}$, $R_{QD} = 625$ kΩ). For detailed parameter ranges and the corresponding two-dimensional figures, please refer to supplementary note 2.

In Si-MOS, the resistance R_{QD} of the SET is relatively large, typically ranging from 0.5 MΩ to 1 MΩ.[40–42] This complicates direct impedance matching between the SET and the tank circuit, making it prone to over-coupling. To ensure optimal impedance matching and maximize sensitivity, we incorporated a matching capacitor C_m into the tank circuit.[36] The role of C_m, as illustrated in Fig. 2(c), is to gradually reduce the Smith chart in the over-coupling state until it passes through the origin, thereby achieving impedance matching. Consequently, the presence of C_m effectively compensates for the errors associated with over-coupling in the circuit. Even in the presence of significant parasitic capacitance within the system, perfect impedance matching can still be achieved by adjusting C_m, as detailed in supplementary note 2.

Similarly, we analyze the impedance adjustment of the system through the trend of simulating the Smith chart for R_{lead}. The role of R_{lead} is to suppress RF leakage; significant transmission of RF signals through the SET occurs only when

the impedance between accumulation gate and lead is much greater than R_{QD}. Otherwise, the RF signals will leak through the lead via ohmic contact. As shown in Fig. 2(d), when R_{lead} is insufficiently large, the corresponding Smith circle is very small, far from achieving impedance matching. However, as R_{lead} continues to increase, the dip in S_{21} becomes deeper, indicating improved impedance matching. Theoretically, when R_{lead} approaches infinity, leakage through the lead path will cease; however, C_{A-L} will still exist. Nevertheless, due to the very small overlapping area between the lead and accumulation gate, its effect can be considered negligible. Therefore, in this design, we optimize the structure related to R_{lead} and turn off the voltage on the lead during RF measurements. We use logarithmic units to plot the S_{21} resonance peak in Figs. 2(c) and 2(d). When the resonance peak has a deep dip, we define the detection bandwidth of the RF as the frequency width at the −3-dB position from the top.

4. Measurement

Now, we test samples prepared according to the split-gate approach. The DC transport current I_{SET} is measured by applying a bias voltage of $V_{SD} = 500$ μV to the DC port of the bias-tee, as shown in Fig. 1(c). Figure 3(a) shows a transport measurement of a Coulomb resonance of the SET as a function of the plunger gate voltage. We selected one of the Coulomb peaks of QD_1 to detect QD_2, when the electronic state in QD_2 changes, the impedance changes due to capacitive coupling with QD_1, which can be detected. We test the change of reflection parameter S_{21} at three locations of coulomb peak, as shown in Fig. 3(b), please refer to supplementary note 1 for the RF-SET measurement setup. Under the resonant condition of $f_{res} = 160.1$ MHz, the change in S_{21} between the peak and valley of the SET coulomb oscillations reaches up to 30 dB, as indicated by the blue and yellow signals in Fig. 3(b). Subsequently, we measured the charge stability diagram using a combination of an RF reflectometer and pulse scanning, as illustrated in Fig. 3(c), where data from over 10^4 points can be collected within a time frame of 1 second. We then scanned the gate voltage of QD_2, using the Coulomb peaks selected in Fig. 3(a) to probe the distribution of electron numbers within QD_2, as shown in Fig. 3(d). This method enables sensitive charge sensing through RF reflection measurements. From these results, we confirmed that the split-gate structure can achieve RF reflection measurement.

Next, we continue to use QD_1 as the SET to probe the opposite QD_2. In selecting the detection position of the SET with higher conductivity, we evaluate the tunneling between the first electron of QD_2 and the reservoir, specifically the RTS between $N = 0$ and $N = 1$, as shown in Fig. 4(a). The sampling rate is set to 9 MSa, resulting in a signal-to-noise ratio (SNR) of 5.72 over an integration time of 140 ns. Notably, the detected charge fidelity reached an impressive 99.86%.

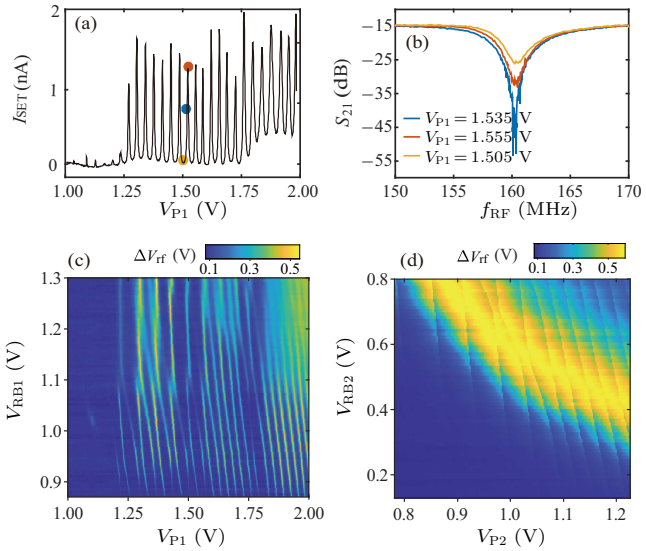


Fig. 3. (a) Schematic plot of the DC current I_{SET} through the SET as a function of gate voltage V_{P1}. A DC bias voltage of 500 μV is imposed to one Ohmic contact, while the other Ohmic contact is connected to a voltmeter through an amplifier. Meanwhile, both Ohmic contacts of the probed quantum dot (QD_2) are grounded. The transport current of SET depends on the voltage of plunger gate V_{P1} and bias voltage. (b) Reflected signals are observed at the positions of the three circles of different colors in panel (a). The reflection coefficient S_{21} of the SET demonstrates variations with changing plunger voltages. Sensitivity is maximized when impedance matching is achieved (indicated in blue). The −15-dB background reflects the attenuation from the directional coupler's coupled port to the input port, with additional circuit attenuations accounted for. (c) Charge stability diagram of QD_1 measured by RF reflectometer, and the figure shows the demodulated voltage signal. (d) QD_1 is used as a detector to measure the signal of QD_2. The jagged signal indicates the transition of electrons. The yellow background indicates the coulomb peak in panel (a).

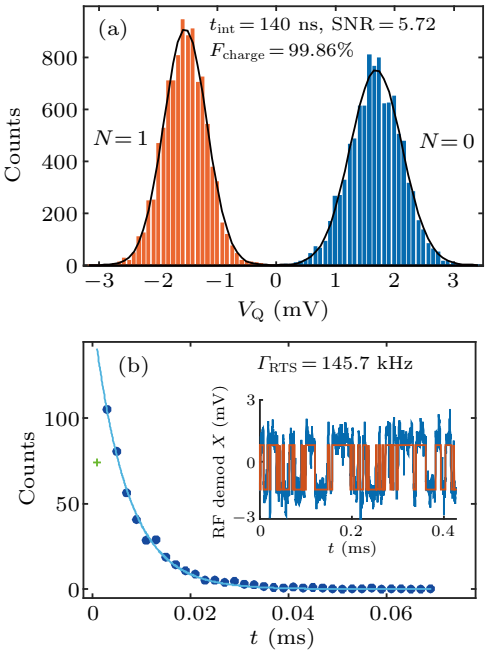


Fig. 4. (a) Distribution of the X component of the demodulated reflected signal at an integration time of $t_{int} = 140$ ns. The black curve is a fit with a sum of two Gaussian distributions. From the fit we obtain an SNR of 5.72. The blue and yellow bars illustrate the V_I voltage distributions reflected by the SET for cases when the number of electrons in the detected quantum dots QD_2 is 0 and 1, respectively. (b) Probability density of the times obtained from the time trace shown in the inserted images, an average RTS tuning rate up to 145.7 kHz is obtained by RF detection.

Figure 4(b) presents a statistical analysis of the RTS signals, with the tested RTS frequency reaching up to 145.7 kHz, enabling rapid readout. In supplementary note 3, we also conducted bandwidth measurement on the sample, with results indicating no attenuation within a bandwidth of 2 MHz. This demonstrates that the RF structure can facilitate rapid, high-fidelity readout. In the RF measurement, we minimize the impact of the RF signal on the properties of the detected electrons by using an RF switch to turn off the RF signal during the non-reading periods of each cycle.

5. Conclusion

In this paper, we proposed a split-gate approach suitable for RF measurements in accumulation mode devices, which can replace the previous Ohmic approach for RF measurements and has relaxed distance requirements for the ion implantation region relative to the center position of the SET. We achieved high bandwidth and high-fidelity readout at a distance of 150 μm from the SET center in the ion implantation region. This method achieves performance comparable to the optimized Ohmic method, while allowing the ion implantation region to be placed further away.

The split-gate structure features the division of the original lead into two parts, where the accumulation gate is used to apply the RF signal, and the new lead serves to inject free electrons into the MOS structure and measure the transport current. To suppress signal leakage during RF measurements, we impose strict limitations on the overlapping area and contact width of these two components. Additionally, during RF measurements, it is necessary to adjust the voltage on the lead to mitigate leakage caused by the capacitance between the lead and the 2DEG. This method ensures accurate measurements with minimal interference. To address signal dissipation, we increased the area of the accumulation gate. Specifically, we rapidly widened the electrode width as it extends outward from the nanostructure of the accumulation gate near the SET. This ensures sufficiently low impedance, reducing RF signal dissipation in this region. Furthermore, we conducted impedance matching and bandwidth calculation simulations using various structural and reflection network parameters to evaluate the effectiveness of this design.

In actual measurement results, we measured over 99% charge readout fidelity within an integration time of 140 ns, with an SNR of 5.72 and an RTS frequency of 145.7 kHz. We also recorded a measurement bandwidth exceeding 2 MHz at the optimal position during testing. All these findings were validated through simulations. This split-gate approach facilitates rapid and high-fidelity readout while expanding the valuable central region of the chip, making it suitable for the large-scale integration of quantum dots.

Acknowledgements

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