

Gate leakage mechanisms in Al_2O_3/SiN/AlN/GaN MIS-HEMTs on Si substrates

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Gate leakage mechanisms in Al_2O_3/SiN/AlN/GaN MIS-HEMTs on Si substrates

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This study investigates the gate leakage mechanisms of AlN/GaN metal–insulator–semiconductor high-electron-mobility transistors (MIS-HEMTs) fabricated on silicon substrate with Al_2O_3/SiN as stacked gate dielectrics, analyzing behaviors across high and low temperature conditions. In the high-temperature reverse bias region ($T > 275$ K, $V_G < 0$ V), Poole–Frenkel emission (PFE) dominates at low electric fields, while trap-assisted tunneling (TAT) is the primary mechanism at medium to high electric fields. The shift from PFE to TAT as the dominant conduction mechanism is due to the increased tunneling effect of electrons as the electric field strength rises. Additionally, TAT is found to be the main gate leakage mechanism under low-temperature reverse bias ($T < 275$ K, $V_G < 0$ V). At lower temperatures, the reduction in electron energy causes the emission process to rely more on electric field forces. Furthermore, under forward bias conditions at both high and low temperatures (225 K $< T <$ 375 K, $V_G > 0$ V), conduction is primarily dominated by defect-assisted tunneling (DAT).

Keywords: AlN/GaN, MIS-HEMTs, gate leakage mechanism, trap-assisted tunneling (TAT)

PACS: 71.55.Eq, 73.40.Qv, 73.40.–c, 73.43.Jn

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1. Introduction

AlN/GaN high-electron-mobility transistors (HEMTs) with ultra-thin AlN barriers offer the advantages of high current density[1] and high frequency performance,[2] showing promising potential in the radio frequency (RF) and high-power electronics applications.[3–5] However, the traditional AlN/GaN HEMT with a Schottky gate (SG) suffers from significant gate leakage current.[6,7] Moreover, the presence of an ultra-thin AlN barrier layer in AlN/GaN SG-HEMTs creates a strong vertical electric field, which limits the breakdown voltage of the device.[8,9] To solve these issues, the insertion of a gate insulator in the access region is adopted, forming the AlN/GaN metal–insulator–semiconductor high-electron-mobility transistors (MIS-HEMTs). Compared with the SG-HEMTs, MIS-HEMTs effectively improve gate leakage current and breakdown voltage.[10]

Further exploration of the gate leakage mechanisms in AlN/GaN MIS-HEMTs is essential for enhancing the reliability of high-frequency devices. There has been considerable research on the leakage currents associated with AlGaN/GaN HEMTs or MIS-HEMTs.[11–19] In contrast, studies on AlN/GaN devices tend to emphasize materials and processes, with little attention on leakage mechanisms. It is worth mentioning that Qin *et al.*[20] have already analyzed the leakage mechanisms of AlN/GaN SG-HEMTs and demonstrated that Poole–Frenkel emission (PFE) and thermionic emission (TE) are the dominant leakage mechanisms under reverse and forward bias, respectively. However, reports on the leakage currents in AlN/GaN MIS-HEMTs are limited. Therefore, it is necessary to address this issue.

In this paper, the conduction mechanisms of both forward and reverse bias gate leakage currents in AlN/GaN MIS-HEMTs with atomic layer deposition (ALD)-Al_2O_3 and *in-situ* SiN as stacked gate dielectric have been analyzed in detail. This paper is arranged as follows: In Section 2, the fabrication structure of AlN/GaN MIS-HEMTs and several important processes are demonstrated. In Section 3, a detailed examination of the current–voltage (I_G–V_G) characteristics across different biases and temperatures is conducted, and corresponding parameters are extracted.

2. Experimental set up

Figure 1(a) shows the schematic diagram of the Al_2O_3/*in-situ* SiN/AlN/GaN MIS-HEMTs in this work. An epitaxial layer of *in-situ* SiN/AlN/GaN (3.5 nm/4 nm/1.5 μm) was grown on a 6-inch (1 inch = 2.54 cm) Si substrate by metal–organic chemical vapor deposition (MOCVD). The room-temperature Hall measurement exhibited the sheet resistance of 249 Ω/□, the electron concentration of 1.75×10^{13} cm^{-2}, and the electron mobility of 1450 cm^{-2}/V·s, respectively. Ti/Al/Ni/Au ohmic contacts were deposited and followed by rapid thermal annealing at 850 °C for 60 seconds. Subse-

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quently, a 3-nm Al_2O_3 dielectric layer was then grown using ALD at 300 °C, and a 120-nm SiN passivation layer was deposited over the entire wafer surface using plasma-enhanced chemical vapor deposition (PECVD). Next, the excess SiN beneath the gate foot region was removed by atomic layer etching. Because of the etching selectivity between ALD-Al_2O_3 and PECVD-SiN, both of the Al_2O_3 and *in-situ* SiN were retained. Finally, Ni/Au/Ti gate metals and interconnection metals were deposited to complete the structure.

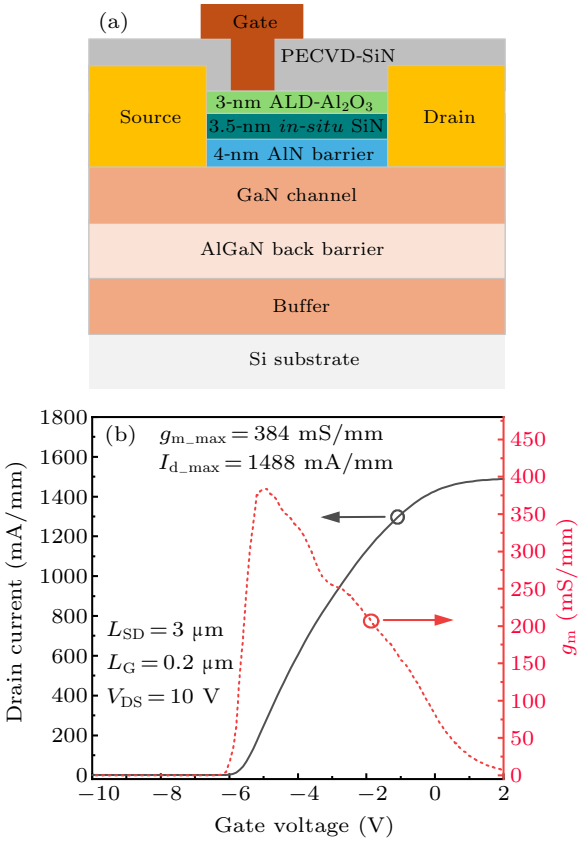


Fig. 1. (a) Schematic cross section of the MIS-HEMTs, (b) transfer characteristic curve of the MIS-HEMTs at $V_{DS} = 10$ V.

As shown in Fig. 1(b), the transfer characteristics of MIS-HEMTs with gate length of 0.2 μm and source-drain spacing of 3 μm exhibit a maximum drain current of 1488 mA/mm and a peak transconductance of 384 mS/mm at $V_{DS} = 10$ V. To further investigate the gate leakage mechanism in this structure, we fabricated FAT-FETs on the same wafer to measure the leakage current, which can ensure the uniformity of the measured current density (J_G).[21] The gate length and gate width of the FAT-FETs are 50 μm and 100 μm. The Agilent B1500 was used to measure the J_G–V_G characteristics of the FAT-FETs at temperatures ranging from 225 K to 375 K in steps of 15 K.

3. Results and discussion

Figure 2(a) illustrates the transfer curve (I_D–V_G) at $V_{DS} = 4$ V for different temperatures. According to the inset of Fig. 2(a), as the temperature increases, the threshold voltage (V_{TH}) shifts positively by less than 0.1 V, which is an insignificant drift. As shown in Fig. 2(b), characteristics of the FAT-FETs were measured at 225 K–375 K. A monotonic increase in gate leakage current density with temperature was observed, indicating that trap-related or defect-related mechanisms dominate current transport in this structure.[23] To eliminate the effect of electric stress on leakage current, the drain current was measured again after the device recovered from 375 K, as shown in the inset of Fig. 2(b). The result indicated that the variation of gate leakage current with temperature is primarily attributable to thermal stress, and that this variation is recoverable.[24]

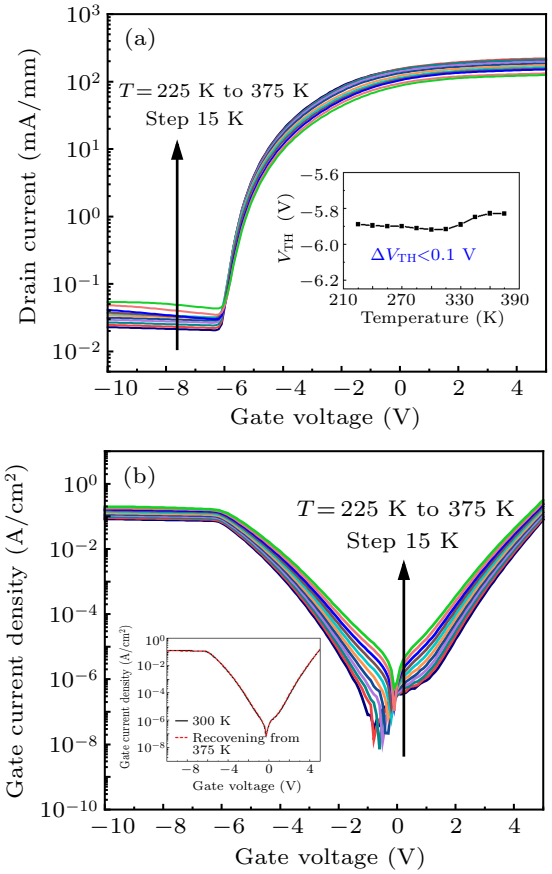


Fig. 2. (a) Temperature dependence of transfer characteristics of the FAT-FETs at $V_{DS} = 4$ V. The inset shows the variation of threshold voltage with temperature. (b) Gate current density versus gate voltage characteristics of the FAT-FETs measured at different temperatures. The inset shows the leakage current at 300 K (solid line) and after recovering from 375 K to 300 K (dashed line).

To investigate the gate leakage mechanisms of AlN/GaN MIS-HEMTs with stacked gate dielectrics, various leakage current transport models were compared with the measured data. It was found that, the leakage mechanisms of this structure are influenced by both electric field and temperature. This research will conduct a detailed analysis of the leakage mechanisms in the high-temperature reverse bias region, low-temperature reverse bias region and forward bias region.

3.1. Reverse gate leakage mechanisms under high temperature

Figure 3(a) shows the reverse J_G–V_G characteristics under high temperature ($T > 275$ K, $V_G < 0$ V). To explore the leakage mechanisms, various models are compared, and two current transport mechanisms are identified, with the dominant operating regions labeled on the plot. The procedure for modeling and the relevant extracted parameters for each current transport mechanism are discussed in detail.

Under moderate electric fields at room temperature or higher, PFE serves as the predominant mechanism.[25] PFE achieves thermal emission by thermally activating electrons from trap levels near the metal Fermi level to the continuous states present in the stacked dielectric and barrier layers.[14] The region where the PFE model is applied is labeled region I in Fig. 3(a). The energy band diagram illustrating the PFE mechanism is presented in Fig. 3(c). Consequently, PFE is influenced by both temperature and electric field strength. The vertical electric field (E) across the stacked dielectric and barrier layers are given by[12]

$$E = \frac{q(\sigma_b - n_{2DEG})}{\varepsilon_r \varepsilon_0}, \tag{1}$$

$$\frac{d}{\varepsilon_r} = \frac{d_{Al_2O_3}}{\varepsilon_{Al_2O_3}} + \frac{d_{SiN}}{\varepsilon_{SiN}}, \tag{2}$$

$$n_{2DEG} = \int_{V_{TH}}^{V} \frac{C}{qA} \mathrm{d}V, \tag{3}$$

where $q = 1.6 \times 10^{-19}$ C is the elementary charge, $\sigma_b = 2.5 \times 10^{13}$ cm^{-2} is the density of polarization charge at AlN/GaN heterointerface, calculated from the self-consistent solution of Schrödinger equation and Poisson's equation. The theoretical dielectric constant ($\varepsilon_r = 7.8$) of the Al_2O_3/SiN stacked layer is calculated using Eq. (2), where $d_{Al_2O_3}$ and d_{SiN} are the thickness of the Al_2O_3 and SiN layer, $d = d_{Al_2O_3} + d_{SiN}$, and $\varepsilon_{Al_2O_3}$ and ε_{SiN} are the dielectric constant of Al_2O_3 and SiN. The n_{2DEG} is the density of 2DEG obtained from integration of the C–V curve, expressed by Eq. (3). Since the change in V_{TH} with temperature is negligible, the E–V distribution can be considered the same at different temperatures, as illustrated in Fig. 3(b).

The current density of PFE (J_{PFE}) is given by[26]

$$\ln\left(\frac{J_{PFE}}{E}\right) = m(T)\sqrt{E} + c(T), \tag{4}$$

$$m(T) = \frac{q}{k_b T}\sqrt{\frac{q}{\pi \varepsilon_i}}, \tag{5}$$

$$c(T) = -\frac{q\phi_t}{k_b T} + \ln(C_{PF}), \tag{6}$$

where k_b is the Boltzmann constant, ε_i is the high-frequency dielectric constant of the gate dielectric layer and the barrier layer, which can be calculated from the measured C–V curve, with an experimental value of 5.85, ϕ_t is the barrier height for the electron emission from the trap states for PFE, and C_{PF} is a constant associated with PFE.

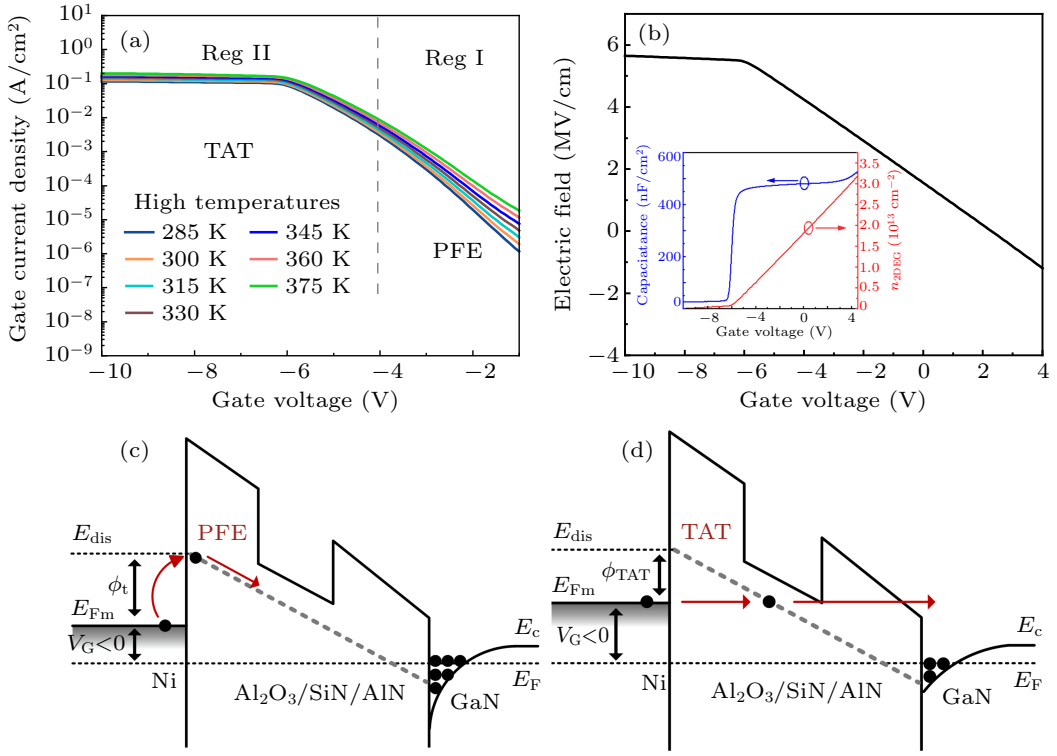


Fig. 3. (a) Reverse J_G–V_G characteristics under high temperatures, with dominant leakage mechanisms and their associated regions labeled; (b) calculated electric field as a function of voltage (E–V) plot. Capacitance–voltage (C–V) experimental data and the calculated 2DEG density are displayed in the inset; (c)–(d) conduction band edge diagrams of Poole–Frenkel emission (PFE) and trap-assisted tunneling (TAT).

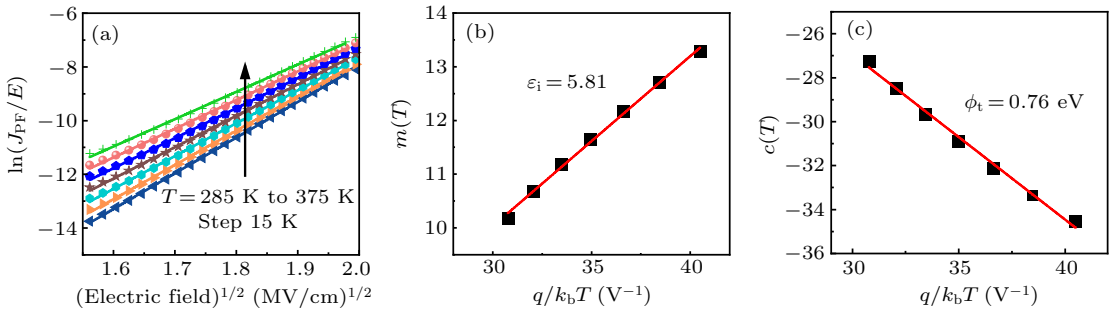


Fig. 4. (a) Characteristics of $\ln(J_{PFE}/E)$ versus $\sqrt{E}$ and the linear fits, (b)–(c) dependence of experimental $m(T)$ and $c(T)$ on q/k_bT and the extracted values of ε_i and ϕ_t.

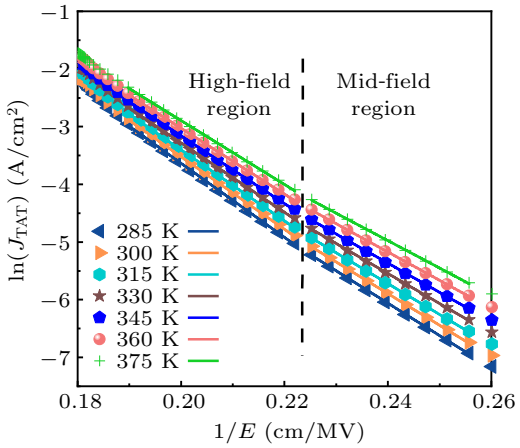


Fig. 5. Characteristics of $\ln(J_{TAT})$ versus $1/E$ in region II, fitted into high-field and mid-field regions.

Table 1. The extracted TAT energy levels at high temperatures.

Temperature (K)	Mid-field ϕ_{TAT} (eV)	High-field ϕ_{TAT} (eV)
285	1.31	1.43
375	1.17	1.30

Figure 4(a) illustrates the $\ln(J_{PFE}/E)$–$\sqrt{E}$ relationship within the temperature range of 285 K to 375 K, demonstrating a strong linear correlation. Using Eq. (4), $m(T)$ and $c(T)$ are extracted from the linear fits. Figures 4(b) and 4(c) display $m(T)$ and $c(T)$ versus q/k_BT. From Eq. (5), the extracted value of ε_i is 5.81, closely approximating the experimental value of 5.85. Additionally, ϕ_t is extracted by Eq. (6), with a result of 0.76 eV, which is close to the reported values.[27]

At higher reverse bias, the electric field strength across the gate dielectric layer increases, making it easier for carriers to pass through the triangular barrier.[28] Thus, another leakage mechanism known as trap-assisted tunneling (TAT) is expected to occur. The bias range where TAT dominates is labeled region II in Fig. 3(a). The energy band diagram depicting TAT is shown in Fig. 3(d). The current density for TAT is given by Dutta *et al.*[14]

$$\ln(J_{TAT}) = \ln(C_1) - \frac{C_2}{E}, \tag{7}$$

$$C_2 = \frac{8\pi\sqrt{2qm_n^*}}{3h}\phi_{TAT}^{3/2}, \tag{8}$$

where C_1 is a constant, $h = 6.626 \times 10^{-34}$ J·s is Planck's constant, m_n^* is the effective mass of electrons in gate dielectric layer, and ϕ_{TAT} is the effective barrier height for TAT.

Figure 5 shows the characteristics of $\ln(J_{TAT})$ versus $1/E$ at temperatures range of 285 K to 375 K. The TAT plot is divided into two linear regions, mid-field and high-field, based on the electric field strength. The extracted ϕ_{TAT} values are listed in Table 1, and it can be observed that the trap energy levels decrease with increasing temperature, due to the narrowing of the bandgap as temperature rises.[29]

In the high-temperature reverse bias, two current transport mechanisms were identified: Poole–Frenkel emission at low reverse bias and trap-assisted tunneling at medium to high reverse bias. As the electric field strengthens, the emission of electrons from the gate metal to the channel gradually transitions from thermal excitation to tunneling.

3.2. Reverse gate leakage mechanisms under low-temperature

The reverse J_G–V_G characteristics under low-temperature ($T < 275$ K, $V_G < 0$ V) are shown in Fig. 6(a). At this region, J_G exhibits a weak temperature-dependence, indicating that tunneling mechanism primarily governs the current transport. It was found that the current conduction in this region is still dominated by the TAT mechanism. Figure 6(b) presents the experimental measurements of $\ln(J_{TAT})$ versus $1/E$, fitted into the low-field and high-field regions, which demonstrate a good linear relationship. The ϕ_{TAT} can be extracted from the slope of the TAT plot, as shown in Table 2. The variation of ϕ_{TAT} with electric field and temperature is consistent with the previously mentioned results, and the values of 1.30 eV–1.46 eV also match the reported research.[29]

When comparing the leakage mechanisms under high-temperature reverse bias and low-temperature reverse bias, certain phenomena can be observed. At low reverse bias voltages, PFE occurs at high temperatures, while TAT is observed at low temperatures. Jiang *et al.*[17] have studied the behavior of leakage current and found that its deviation from the PFE process occurs at low temperatures. The turning point aligns with the temperature at which the frozen-trap effect becomes

significant. Therefore, at low temperatures, the emission of frozen electrons from the trap states primarily depends on the force of the electric field. This clarifies that within the same voltage range, two different conduction mechanisms occur at different temperature ranges.

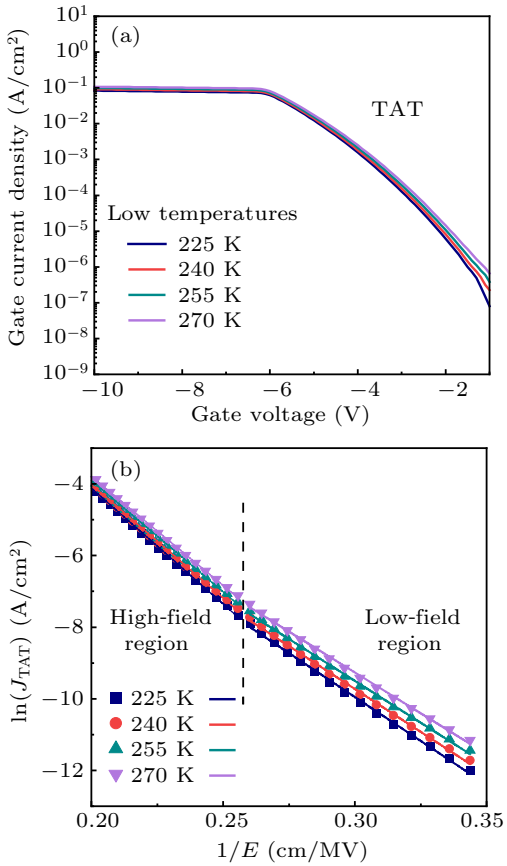


Fig. 6. (a) Reverse J_G–V_G characteristics under low temperature, with dominant leakage mechanism labeled; (b) characteristics of $\ln(J_{TAT})$ versus $1/E$, fitted into high-field and low-field regions.

Table 2. The extracted TAT energy levels at low temperatures.

Temperature (K)	Low-field ϕ_{TAT} (eV)	High-field ϕ_{TAT} (eV)
225	1.44	1.46
270	1.38	1.4

3.3. Forward gate leakage mechanisms

The forward J_G–V_G characteristics from 225 K to 375 K are shown in Fig. 7. Due to the significant lattice mismatch in the AlN/GaN heterojunction, there is a high dislocation density at the heterojunction interface. Additionally, the stacked gate dielectric layer introduces some of defects. Therefore, we considered the defect-assisted tunneling (DAT) mechanism, with the energy band diagram illustrated in the inset of Fig. 7. The DAT current density (J_{DAT}) is provided by[12]

$$J_{DAT} = J_{DAT0}\left\{\exp\left(\frac{V_G}{\eta_{DAT}V_T}\right) - 1\right\}, \tag{9}$$

where J_{DAT0} is the reverse saturation current density for DAT, η_{DAT} is the ideal factor, and $V_T = k_bT/q$. V_G is much greater than V_T, so equation (9) can be rewritten as

$$\ln(J_{DAT}) = k_{DAT}V_G + B, \tag{10}$$

$$k_{DAT} = \frac{1}{\eta_{DAT}V_T}, \tag{11}$$

where B is a constant. From Eq. (10), if the gate leakage current is caused by DAT, then the curves of $\ln(J_{DAT})$ versus V_G will exhibit a linear relationship.

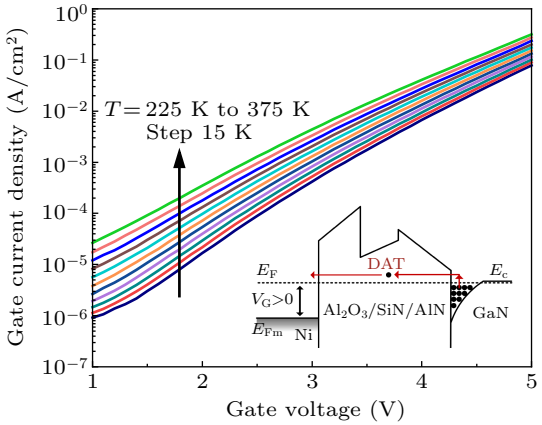


Fig. 7. Forward J_G–V_G characteristics from 225 K to 375 K. The inset shows the schematic diagram of DAT mechanism.

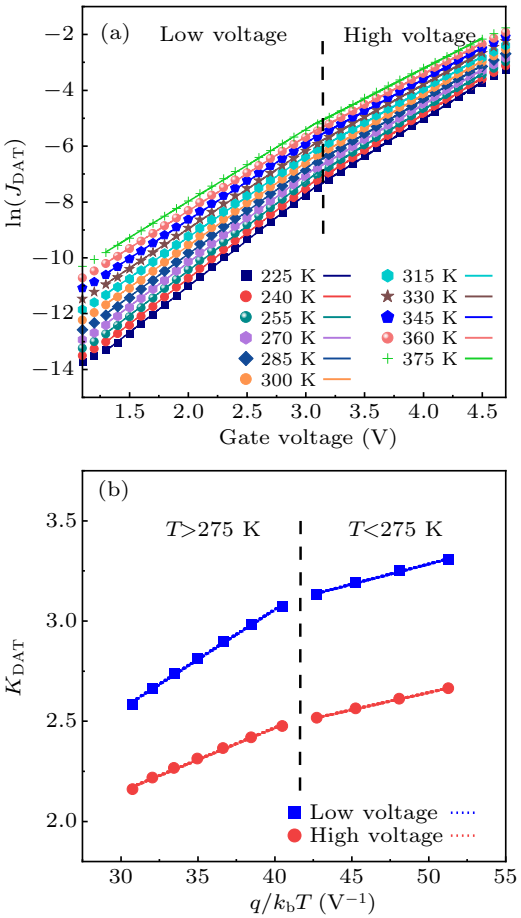


Fig. 8. (a) Characteristics of $\ln(J_{DAT})$ versus V_G plot, (b) slope extracted from the DAT plot (k_{DAT}) versus q/k_bT plots.

Figure 8(a) shows the experimental measurement curves of $\ln(J_{DAT})$ versus V_G, which are divided into low and high

voltage regions. It is clearly observed that the measured data still fits the straight line well. Subsequently, k_{DAT} was extracted from the DAT plot by Eq. (11), as shown in Fig. 8(b). The ideal factor of 19.1 was extracted from the TAT plot, which is very close to the reported value.[30] This confirms that DAT dominates gate leakage under forward bias.

The primary leakage mechanisms of AlN/GaN MIS-HEMTs differ from those of AlN/GaN SG-HEMTs or AlGaN/GaN HEMTs. Specifically, the key distinction between AlN/GaN MIS-HEMTs and AlN/GaN SG-HEMTs is the introduction of a dielectric layer, which effectively suppresses thermionic emission and alters the leakage paths of the device. Meanwhile, the difference compared to traditional AlGaN/GaN HEMTs lies in the lattice mismatch between AlN and GaN, introducing some dislocation defects that affect the leakage behavior. Moreover, research indicates that in MIS-HEMTs, gate leakage is primarily influenced by the properties of the dielectric layer, including its thickness, material quality, and interface characteristics.[14] Therefore, these factors result in the leakage current in this structure being primarily dominated by TAT, PFE, and DAT.

4. Conclusion

To conclude, we investigated the gate leakage current mechanisms in Al_2O_3/*in-situ* SiN/AlN/GaN MIS-HEMTs on a 6-inch silicon substrate at both high and low temperatures. In the high-temperature reverse bias region, PFE is the primary leakage mechanism at low fields, while TAT becomes the dominant mechanism at medium to high fields. As the electric field strength increases, electrons more easily tunnel from the gate metal to the channel, leading to a shift in the leakage mechanisms. Besides, when the temperature decreases, the energy of the electrons is reduced, causing the emission process to rely mainly on electric field forces. As a result, gate leakage is predominantly governed by the TAT mechanism at low-temperature reverse bias. And conduction in forward bias is dominated by DAT.

Acknowledgement

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