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RAPID COMMUNICATION

Ultrafast reconfigurable direct charge trapping devices based on few-layer MoS_2

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Charge trapping devices incorporating 2D materials and high-κ dielectrics have emerged as promising candidates for compact, multifunctional memory devices compatible with silicon-based manufacturing processes. However, traditional charge trapping devices encounter bottlenecks including complex device structure and low operation speed. Here, we demonstrate an ultrafast reconfigurable direct charge trapping device utilizing only a 30 nm-thick Al_2O_3 trapping layer with a MoS_2 channel, where charge traps reside within the Al_2O_3 bulk confirmed by transfer curves with different gate-voltage sweeping rates and photoluminescence (PL) spectra. The direct charging tapping device shows exceptional memory performance in both three-terminal and two-terminal operation modes characterized by ultrafast three-terminal operation speed (∼300 ns), an extremely low OFF current of 10^{-14} A, a high ON/OFF current ratio of up to 10^7, and stable retention and endurance properties. Furthermore, the device with a simple symmetrical structure exhibits V_D polarity-dependent reverse rectification behavior in the high resistance state (HRS), with a rectification ratio of 10^5. Additionally, utilizing the synergistic modulation of the conductance of the MoS_2 channel by V_D and V_G, it achieves gate-tunable reverse rectifier and ternary logic capabilities.

Keywords: charge trapping memory, two-dimensional materials, reconfigurable device, reverse rectification

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1. Introduction

With the development of the Internet of things and artificial intelligence, there is an urgent demand for compact, efficient, and multifunctional memory devices compatible with silicon-based manufacturing processes.[1,2] As dimensional scaling, constrained by dielectric layer point defects[3] and capacitively coupled interference between adjacent units,[4,5] charge trapping memories[6] are replacing floating gate memories[7] as the mainstream silicon-based nonvolatile memory, but still encounter bottlenecks including leakage,[8,9] short-channel effects,[10,11] complex fabrication processes involving three layers for tunneling, trapping, and blocking dielectrics[12–15] and low operation speed. Owing to the ultra-thin thickness, free of dangling bonds and excellent gate electrostatic control,[10,16–20] two-dimensional (2D) materials have emerged as promising materials for high-performance electronic devices, notably for their superior immunity to short-channel effects[10,21] when used as channels. However, most 2D materials-based charge trapping memories still exhibit low operation speed.[14,15,22–27] Previously, by integrating atomically flat h-BN as tunneling layer into traditional three-layer charge trapping devices, atomically sharp interface is formed between the MoS_2 channel and h-BN tunnel layer, enabling the high-efficiency program/erase operation with a speed of 20–30 ns.[28] By using MoS_2 and graphdiyne (GDY) for the channel and trapping layer, respectively, extremely fast write speeds (8 ns) and low operating voltages (30 mV) are achieved, while the erase speed is still at ∼100 μs.[29] Specifically, unlike traditional three-layer charge trapping devices, direct charge trapping memory with GDY/MoS_2 Van der Waals heterostructure features a simple structure with only the channel and the trapping layer,[23] offering great opportunities to improve the operation speed of direct charge trapping memories by selecting appropriate charge trapping layers. ALD-grown high-k dielectrics, such as Al_2O_3 and HfO_2, often possess rich defect states that can serve as charge trapping centers.[27,30–35] Moreover, due to their strong electrostatic modulation capabilities on the channel, the control of trapped charges can be greatly enhanced,[36–38] suggesting that they can function as an efficient charging trapping layer to improve the operation speed of direct charge trapping memories.

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Here, we demonstrate an ultrafast reconfigurable direct charge trapping device featuring a simple structure with only a 2D MoS_2 channel and a 30 nm-thick Al_2O_3 trapping layer. The charge trapping primarily occurs in the defect states within Al_2O_3, confirmed by dual-sweeping transfer curves with different gate-voltage sweeping rates and photoluminescence (PL) spectra. Our device demonstrates exceptional memory properties under both three-terminal and two-terminal operation modes. The device shows ultrafast three-terminal operation speed (∼300 ns), an incredibly low off-state current of 10^{-14} A, a high ON/OFF current ratio of up to 10^7 and stable retention and endurance properties. Unlike traditional rectification methods relying on PN junctions[39–41] or Schottky junctions,[42] our device demonstrates V_D polarity-dependent reverse current rectifying behavior in the high resistance state (HRS) in a simple symmetrical structure, with a rectification ratio of 10^5. This shows the synergistic modulation of the conductance of the MoS_2 channel by V_D and V_G. Additionally, by serially connecting a resistor to the device, it achieves gate-tunable voltage rectification and ternary logic capabilities. Our device demonstrates its potential as a viable candidate for next-generation electronic devices with enhanced efficiency, versatility, and scalability.

2. Results

2.1. Device structure and operating principle of the direct charge trapping device

Figure 1(a) shows the 3D schematic view of the direct charge trapping device, in which few-layer MoS_2, 30 nm Al_2O_3, and bottom Cr/Au are employed as the channel material, trapping layer and control gate electrode, respectively. Cr/Au (5 nm/50 nm) control gate and contact electrodes were patterned by standard e-beam lithography followed by e-beam deposition and a lift-off process. 30 nm Al_2O_3 was grown via atomic layer deposition (ALD) at 150 °C. Few-layer MoS_2 was mechanically exfoliated and transferred onto the Al_2O_3 by a dry transfer method. The detailed device fabrication processes are described in Appendix A. The measurement configuration under traditional three-terminal operation mode is also shown, in which the current of the MoS_2 channel is read at a fixed V_D with source electrode grounded after program/erase the device by applying positive/negative control gate voltage pulses ($V_{G,\mathrm{pulse}}$) between the control gate and the source electrode side. Figure 1(b) depicts the optical image of a typical direct charge trapping device. The dual-sweeping transfer characteristics were recorded to probe the memory functionality of the direct charge trapping device. As shown in Fig. 1(c), with $V_D = 0.1$ V, when dually sweeping V_G at different $V_{G,\mathrm{AMX}}$ ranges (5 V, 10 V, and 15 V), apparent memory windows due to the offset of the threshold voltage at the current level of $\sim 10^{-10}$ A are observed. The memory window (ΔV) increases as the $V_{G,\mathrm{MAX}}$ increases from 5 V to 15 V, with a maximum memory window of 20 V observed when $V_{G,\mathrm{MAX}} = 15$ V. To exclude the effect of interfacial trapped charges between MoS_2 and Al_2O_3 on the presence of the memory windows,[43] we measured the dual-sweeping transfer curves of the device under varying gate-voltage sweeping rates at $V_D = 0.1$ V. As shown in Fig. 1(d), with increasing gate-voltage scan rates from 0.2 V/s to 20 V/s, the memory windows of the device are reduced. However, even at a very high scan rate of 20 V/s, a significant memory window can still be observed, indicating that the interfacial trapped charges between the MoS_2 channel and the Al_2O_3 are not the main factor for the presence of the large memory window.[23,44,45] Furthermore, to reveal the effect of adsorbents from air on the MoS_2 channel, such as oxygen and water,[43,46–48] we measured the effect of gate-voltage scan rates on the memory window of the direct charge trapping device that was encapsulated with poly(methyl methacrylate) (PMMA) in a glove box under Ar gas atmosphere (supplementary Fig. S1). Compared with that of exposed in ambient air (Fig. 1(d)), the encapsulated device shows a nearly-constant memory window with increasing scanning rates, suggesting that adsorbents from ambient air indeed have some effect on the memory window.

Intrinsic defects, including oxygen vacancies and interstitial oxygen atoms, are inevitably formed in ALD-grown Al_2O_3 dielectrics, which gives rise to defect energy levels in the bandgap of Al_2O_3.[49] To determine these defect energy levels in Al_2O_3, photoluminescence (PL) spectra were collected from different regions of the device, including bare 285 nm SiO_2/Si substrate, 30 nm Al_2O_3 film on SiO_2/Si substrate, and few-layer MoS_2 on Al_2O_3/SiO_2/Si substrate. As shown in Fig. 1(e), by identifying the peaks at ∼2.45 eV for the defect level of bare SiO_2[50] and ∼1.82 eV for the energy gap of MoS_2,[51,52] the PL peaks at 1.97 eV, 2.18 eV, 2.38 eV, and 3.29 eV coming from multiple defect levels in the Al_2O_3 film grown by ALD are revealed. These defect states provide deep enough potential wells for charge storage.[53] As shown in Fig. 1(f), when a positive V_G applied, electrons can be pulled from the MoS_2 channel and trapped by the defect states of Al_2O_3 layer, forming a high-resistance program state. Oppositely, when a negative V_G is applied, electrons can be pushed back from Al_2O_3 layer to the MoS_2 channel, forming a low-resistance erase state. The large memory windows presented in Figs. 1(c) and 1(d) indicate the high trapping efficiency of the defect levels in Al_2O_3 layers, encouraging us to construct high-performance non-volatile charge trapping memories.

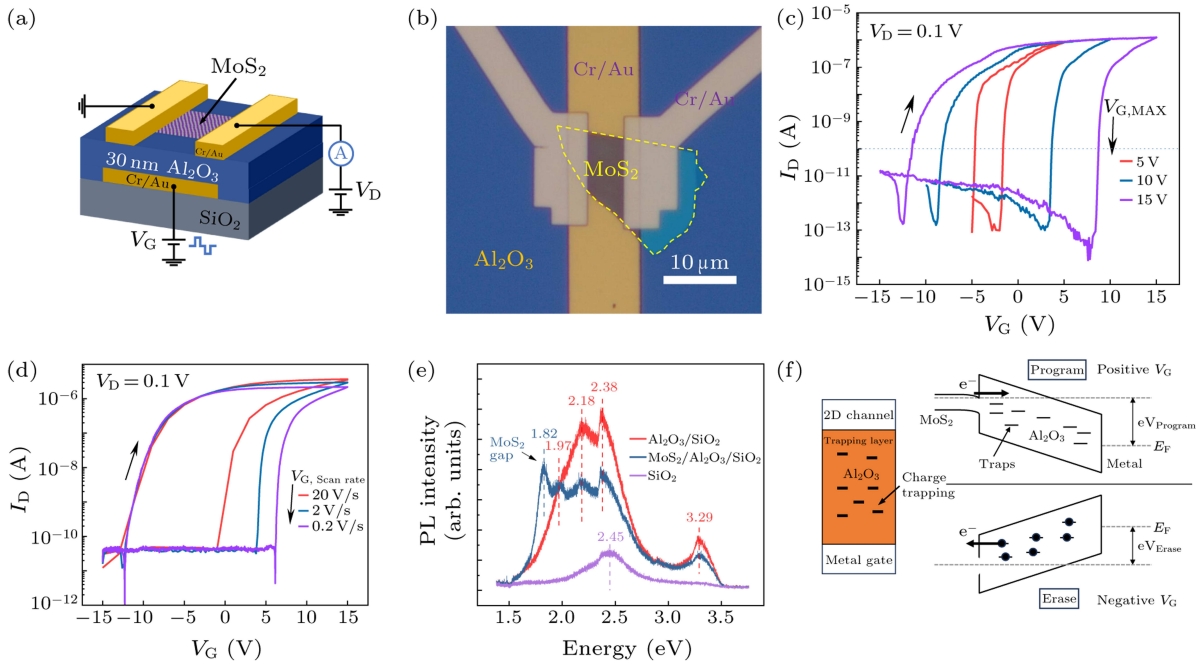


Fig. 1. Device structure and operating principle of the direct charge trapping device based on few-layer MoS_2. (a) The 3D schematic view of the direct charge trapping device with a 30 nm Al_2O_3 serving as the trapping layer. The measurement configuration under traditional three-terminal operation mode with pulse applied to the gate (V_G) is also shown. (b) Optical image of a typical direct charge trapping device. (c) Dual-sweeping transfer curves of the direct charge trapping device at $V_D = 0.1$ V with different V_G sweep ranges. The arrows show the sweep directions of V_G. (d), Dual-sweeping transfer curves of the direct charge trapping device with varying sweep rates of V_G at $V_D = 0.1$ V within a 15 V $V_{G,MAX}$ sweep range. (e) Photoluminescence spectra of bare 285 nm SiO_2/Si substrate, 30 nm Al_2O_3 film on SiO_2/Si substrate, and few-layer MoS_2 on Al_2O_3/SiO_2/Si substrate, revealing multiple defect states in the Al_2O_3 film grown by ALD. (f) Schematic of the operating principle of the direct charge trapping device. For the program operation, a positive V_G pulse pulls electrons to the Al_2O_3 layer from the MoS_2 channel. While for the erase operation, a negative V_G pulse pushes electrons back from the Al_2O_3 layer to the MoS_2 channel.

2.2. Ultrafast direct charge trapping memories under three-terminal operation mode

To evaluate the practical application of the direct charge trapping device as memory, retention and endurance characteristics, including their program/erase speeds, were investigated. Figure 2(a) illustrates the retention characteristics of the direct charge trapping device. In the program process, when a +26 V gate voltage pulse ($V_{G,pulse}$) with a full width at half maximum (FWHM) of 300 ns (shown in Fig. S2) is applied, electrons tunnel from the MoS_2 channel into the Al_2O_3 charge trapping layer. After positive $V_{G,pulse}$ is removed, electrons are stored in the trap states of Al_2O_3, inducing a depleted state exhibiting high resistance state (HRS) characteristics (blue curve). The accumulated charge in the trap states of Al_2O_3 can be well retained after withdrawing the $V_{G,pulse}$ because of high barrier heights between the defect states and the conduction/valence band edges of Al_2O_3. On the contrary, in the erase process, when a −20 V $V_{G,pulse}$ with a FWHM of 300 ns (shown in Fig. S2) is applied, the stored electrons tunnel from the Al_2O_3 back to the MoS_2 channel, resulting in a low resistance state (LRS) (red curve). The currents were measured under a fixed V_D of 0.1 V. The current of LRS can be stably maintained for more than 1000 s, while that of HRS slowly increases from $\sim 10^{-15}$ A to $\sim 10^{-13}$ A. After 1000 s, the ON/OFF ratio still exceeds 10^6, indicating a low back-tunneling probability and more stable retention characteristics even without extra blocking layers that are used in traditional three-layer (for tunneling, trapping, and blocking dielectrics) charge trapping memories.[14,15] It is found that the presence of defect-assisted tunneling[54,55] will greatly degrade the retention capability of charge trapping memories. To improve the retention performance, defect-free blocking layers are necessary in traditional three-layer charge trapping memories. However, to ensure sufficient program/erase efficiency, larger operation voltages need to be applied. The successful ultrafast program/erase operations of our direct charge trapping device can be attributed to the high program/erase efficiency ensured by direct and ultrafast trapping/de-trapping electrons in the trap states of the Al_2O_3 layer.[31,45] We have also fabricated charge trapping memory devices using 8 nm HfO_2/30 nm Al_2O_3 stack and 8 nm HfO_2 as charge trapping layer, selecting MoS_2 with the same optical contrast on polydimethylsiloxane (PDMS) as the channel for both. As shown in supplementary Fig. S3, for charge trapping memories using HfO_2/Al_2O_3 stack as trapping layer, the current ON/OFF ratio for erase and program operations can reach $\sim 10^6$, but under a much slower operation speed of 1 ms for erase and 1 s for program operations. However, for charge trapping memories using HfO_2 as trapping layer, a much lower current ON/OFF ratio of $\sim 10^4$ is achieved under similar program/erase operations. The effect

of the MoS_2 thickness on the window and switch ratio were also investigated, as shown in supplementary Fig. S4. Despite the noticeable contrast differences on the same substrate, the switch ratio and window size remained largely the same, while the thicker MoS_2 exhibited a smaller subthreshold swing (SS). These results suggest that the various trap states presented in the Al_2O_3 trapping layer play an important role in the ultrafast operation of the direct charge trapping device.

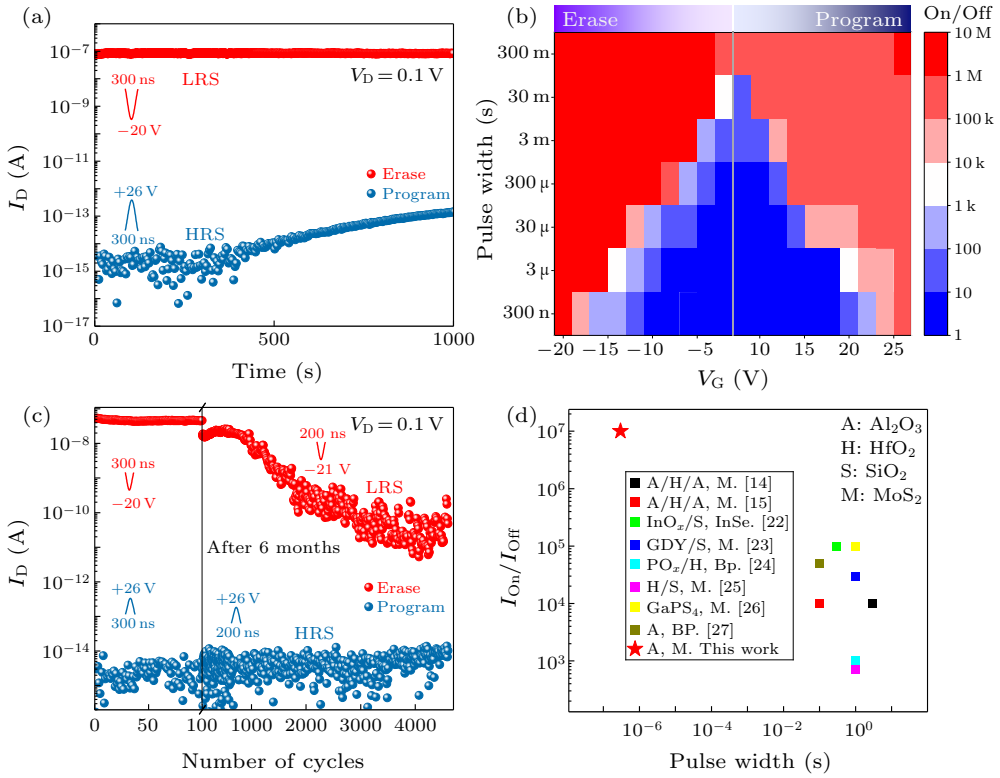


Fig. 2. Memory performance of the direct charge trapping device based on few-layer MoS_2 under three-terminal operation mode. (a) Retention characteristics of the direct charge trapping device at $V_D = 0.1$ V executed with V_G pulses of +26 V/−20 V with a FWHM of 300 ns for program/erase operations, respectively. Program operation sets the device to a high-resistance state (HRS), while erase operation sets the device to a low-resistance state (LRS). (b) Heatmap of the attained ON/OFF ratio of memory under different voltage pulse conditions with varying both the amplitude and pulse width. (c) Endurance characteristics of the direct charge trapping device. The first 100-cycle endurance test was conducted using V_G pulses of +26 V/−20 V for program/erase operations, with an FWHM of 300 ns (the same pulses as in the previous retention test). After six months from the initial 100-cycle test, a subsequent endurance test of 4500 cycles was conducted, using V_G pulses of +26 V/−21 V with a narrower FWHM of 200 ns for program/erase operations. The currents were all measured at $V_D = 0.1$ V. (d) Comparison of the proposed device with other charge trapping devices in ON/OFF ratio and operation speed (pulse width).

To further investigate the minimum voltages required for erase and program operations for various pulse widths, we measured the current ON/OFF ratios as a function of gate voltage pulse amplitudes and widths after program/erase operations, as shown in Fig. 2(b). The channel currents were measured under a fixed V_D of 0.1 V. In erase operation, the device was initially set to a reference HRS using a +26 V V_G pulse with a width of 300 ms, resulting in an initial current of $\sim 10^{-14}$ A, as shown in supplementary Fig. S5(a). The applied erase voltage amplitudes spanned from −20 V to −2 V with a step of 2 V with the pulse width varied from 300 ns to 300 ms. In program operation, the device was initially set to a reference LRS using a −20 V V_G pulse with a width of 300 ms, resulting in an initial current of $\sim 10^{-7}$ A, as shown in supplementary Fig. S5(b). The applied program voltage amplitudes ranged from +6 V to +26 V with a step of 2 V with the pulse width varied from 300 ns to 300 ms. From the heatmap of the ON/OFF ratios, it can be seen that for erase operations with a gate voltage of −20 V, the device can be erased to LRS for any pulse width. While for program operations, only when the voltage amplitude is increased to +26 V, the device can be programmed to HRS with a high current ON/OFF ratio for any pulse width. The asymmetric voltage amplitudes required for program/erase operations come from the asymmetric tunnel barriers for electrons and holes, as schematically shown in the energy band diagram in supplementary Fig. S6. The barrier height for electrons to tunnel from MoS_2 into Al_2O_3 equals to $\phi_e = \chi_M - \chi_A = 2.6$ eV, while the barrier height for holes equals to $\phi_h = \chi_A + E_{gA} - \chi_M - E_{gM} = 2.1$ eV. Therefore, it is easier for holes to tunnel through the barrier. On the other hand, according to the previously reported energy level of defect states in Al_2O_3,[56,57] the potential barriers ϕ_1, ϕ_2 and ϕ_3 between the three main defect states and the bottom of the conduction band of Al_2O_3 are 1.97 eV, 2.18 eV and 2.38 eV (Fig. 1(e)), respectively, which are all lower than ϕ_e. Consequently, trapped electrons in the defect states after program

operations are easier to tunnel back into the channel under applied erase gate voltages.

The endurance characteristics of this device is shown in Fig. 2(c). Firstly, repeated program/erase operations of 100 cycles were performed on the device using V_G pulses of +26 V/−20 V with an FWHM of 300 ns (the same pulses as in the previous retention test). The HRS and LRS currents remained unchanged throughout the 100-cycle endurance test. After six months, we conducted additional 4500-cycle endurance test on it using V_G pulses of +26 V/−21 V with a narrower FWHM of 200 ns for program/erase operations. The HRS current still kept constant during the 4500-cycle test. The LRS current, however, began to exhibit noticeable fluctuations and degradation after the first 1000 cycles. By the end of 4500 cycles, the LRS current had decreased by three orders of magnitude with current fluctuations reaching up to one order of magnitude. Nevertheless, the device still exhibited an ON/OFF ratio of $\sim 10^3$ and the decay of the LRS current gradually slowed down, indicating the excellent endurance characteristics of the device. The degradation and fluctuation of the LRS current are closely related to the movement of defects and the generation of new defects in Al_2O_3 due to bias stress during endurance tests.[58–62] The movement of defects and the generation of new defects cause fluctuations in the spatial distribution of charges stored in Al_2O_3, which subsequently affects their modulation to the channel and ultimately results in fluctuation in the channel current. At the same time, the variation of defects also reduces the erase efficiency of the device, leading to a decrease in LRS current.[63] By increasing the amplitude of the erase voltage pulse from −21 V to −22 V (keeping the pulse width constant), as shown in supplementary Fig. S7, the device was erased back to the original LRS current level observed at the beginning of the 4500-cycle test, but the LRS current still slowly decreased as the number of cycles increased.

We compare the ON/OFF ratio and operation speed (pulse width) of our ultrafast direct charge trapping device with those of other charge trapping devices, as shown in Fig. 2(d). In traditional three-layer ($Al_2O_3/HfO_2/Al_2O_3$) charge trapping memories using MoS_2 as the channel material,[14,15] the typical operation speed is above 100 ms with an ON/OFF ratio of $\sim 10^4$. As for two-layer charge trapping memories, whether direct charge trapping with a blocking layer[22–24] or two oxide layers (HfO_2/SiO_2),[25] the typical operation speed is also above 100 ms with an ON/OFF ratio of $\sim 10^3$–10^5. For one-layer direct charge trapping device,[26,27] the operation speed is also above 100 ms with an ON/OFF ratio of below 10^5. Using one-layer Al_2O_3 as the charge trapping layer, our direct charge trapping device achieves an ultrafast operation speed of ∼300 ns with a greatly enhanced ON/OFF ratio of $\sim 10^7$. Previously, by replacing atomically flat h-BN for Al_2O_3 as tunneling layer in traditional three-layer charge trapping devices, atomically sharp interface is formed between the MoS_2 channel and h-BN tunnel layer, enabling the high-efficiency program/erase operation with a speed of 20–30 ns.[28] The high ON/OFF ratio of $\sim 10^7$ in our charge trapping memory device makes it possible to realize multi-bit data storage and suitable for both memory and synaptic applications (supplementary Fig. S8), enriching the diversity of device functionalities.

2.3. Direct charge trapping memories under two-terminal operation mode

Previous studies indicate that the charge trapping memories can be operated in two-terminal mode,[15,64,65] in which trapping and de-trapping processes are conducted by controlling the drain voltage instead of the gate voltage. The measurement configuration for two-terminal operation of our direct charge trapping device is depicted in Fig. 3(a). The gate was either left floating or grounded for leakage currents (I_G) measurement. Figure 3(b) illustrates the I_D–V_D curves of the direct charge trapping device by dually sweeping the drain voltage with different $V_{D,MAX}$. The sweeping directions are marked by the black arrows. Under a 15 V $V_{D,MAX}$ dual sweep range, large counterclockwise memory windows are observed. The memory window is 6.5 V (−6.5 V to 0 V) on the negative voltage side and 3.3 V (0 V to 3.3 V) on the positive voltage side due to the offset of the threshold voltage at the current level of $\sim 10^{-9}$ A. The device also exhibits a high ON/OFF ratio of $\sim 10^8$, showing the potential for commendable memory capability. The leakage currents are at the level of $\sim 10^{-14}$ A, demonstrating that no electrons enter the bottom electrode.

To evaluate the practical application of the device as memory, retention and endurance characteristics of the device under two-terminal operation mode were investigated. Figure 3(c) illustrates the retention characteristics of the direct charge trapping device. In the program process, when a −26 V drain voltage pulse ($V_{D,pulse}$) with a width of 1 s is applied, electrons tunnel from the MoS_2 channel into traps in Al_2O_3 by the potential difference between the drain electrode and the Al_2O_3 layer (supplementary Fig. S9).[15,64] After the negative $V_{D,pulse}$ is removed, electrons are stored in the trap states of Al_2O_3, inducing a depleted state (high resistance state, HRS) (blue curve). The accumulated electrons in the trap states in Al_2O_3 can be well retained after withdrawing the $V_{D,pulse}$ because of high barrier heights between the defect states and the conduction/valence band edges of Al_2O_3 (supplementary Fig. S6). On the contrary, in the erase process, when a +26 $V_{D,pulse}$ with a width of 1 s is applied, the stored electrons can tunnel from the Al_2O_3 back to the MoS_2 channel (supplementary Fig. S9), inducing a low resistance state (LRS) (red curve). The currents were measured under a fixed V_D of 0.1 V.

The current of LRS can be stably maintained for more than 1000 s, while that of HRS slowly increases from $\sim 10^{-14}$ A to $\sim 10^{-13}$ A. After 1000 s, the ON/OFF ratio still exceeds 10^5. The current ON/OFF ratios as a function of gate pulse amplitudes and widths after program/erase operations are shown in supplementary Fig. S10. From the heatmap of the attained ON/OFF ratios, it can be seen that, compared to the three-terminal mode, achieving the same effective ON/OFF ratio requires wider pulse widths and larger pulse voltages in the two-terminal mode, suggesting that charge trapping and de-trapping are less efficient in the two-terminal mode. To explore the memory mechanisms of the device operating in the two-terminal mode, we conducted a control experiment in a direct charge trapping device without a bottom electrode, as shown in supplementary Fig. S11, there is no memory window in dual-sweeping I_D–V_D curves of the device without a bottom electrode, even when $V_{D,MAX}$ is increased to 15 V. It is speculated that the existence of the bottom electrode facilitates the vertical component of the electric field generated by V_D, inducing a potential difference between the drain electrode and the Al_2O_3 layer, thereby enabling the electron tunneling into/out Al_2O_3.[64] Dual-sweeping I_D–V_D curves at varying V_D sweeping rates were also measured. The memory window shows almost no change between the scan rates of 0.2 V/s and 2 V/s (supplementary Fig. S12), indicating that charges are trapped within the defects in Al_2O_3 rather than at the MoS_2/Al_2O_3 interface. Figure 3(d) shows the endurance characteristics of the direct charge trapping device executed with alternate V_D pulses of +18 V/−18 V with a width of 1 s for program/erase operations, respectively. After 100 cycles of program and erase operations, the current level of the two states remains unchanged, and the ON/OFF ratio retains a high value of $\sim 10^5$ without obvious degradation, indicating robust endurance performance.

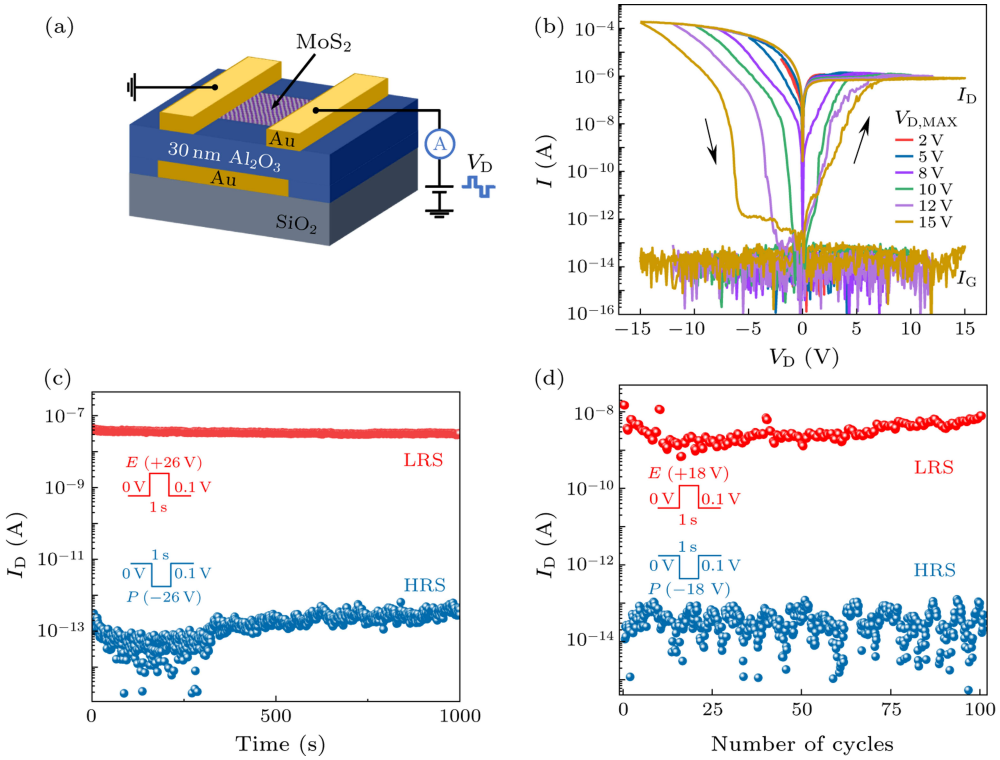


Fig. 3. Memory performance of the direct charge trapping device under two-terminal operation mode. (a) The 3D schematic of the direct charge trapping device under two-terminal operation mode. The voltage pulse is applied to the drain. The gate is floated or grounded for leakage currents (I_G) measurement. (b) The I_D–V_D curves of the direct charge trapping device under different V_D dual sweep range. The corresponding leakage currents are also shown. The sweeping directions are marked by the black arrows. (c) Retention characteristics of the direct charge trapping device at $V_D = 0.1$ V executed with V_D pulses of +26 V/−26 V with a width of 1 s for program/erase operations, respectively. Program and erase operations set the device to HRS and LRS, respectively. (d) Endurance performance test of the direct charge trapping device at $V_D = 0.1$ V executed with alternate V_D pulses of +18 V/−18 V with a width of 1 s for program/erase operations, respectively.

2.4. Gate-tunable reverse rectifier and ternary logic

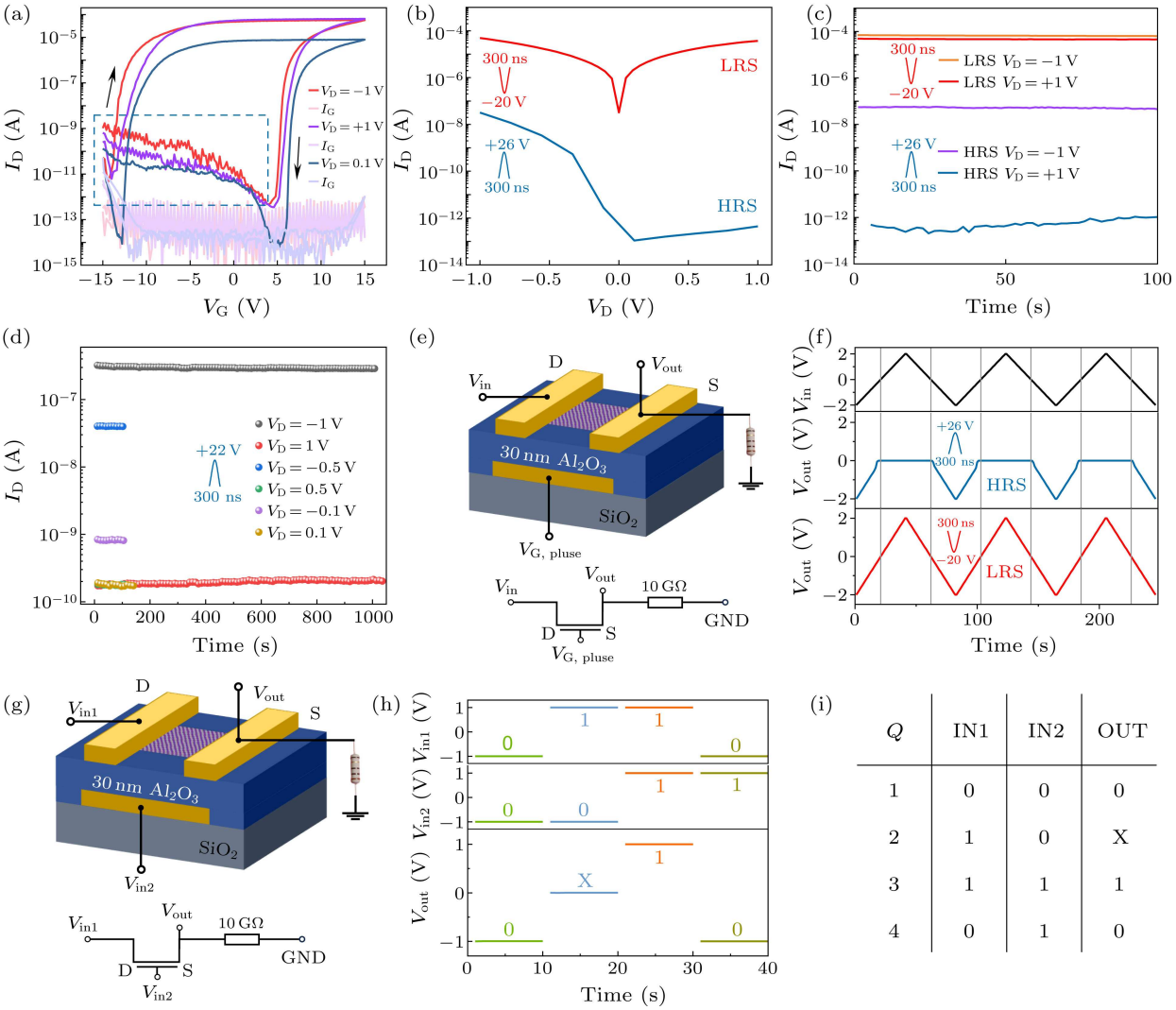
In the two-terminal operation mode, we found that the channel current of our direct charge trapping device is strongly dependent on the polarities and amplitudes of the drain voltage. To further uncover this effect, we measured dual-sweeping transfer characteristics of the direct charge trapping device at $V_D = -1$ V, +1 V, and +0.1 V within a 15 V $V_{G,MAX}$ sweep range, as shown in Fig. 4(a). It is observed that under the gate modulation, in the lower current segment of the curves (indicated by the dashed rectangular box), the current at $V_D = -1$ V surpasses that at $V_D = +1$ V. The output characteristics of the device were measured by setting it to LRS and

HRS through applying −20 V and +26 V V_G pulses with an FWHM of 300 ns, respectively. As shown in Fig. 4(b), when sweeping V_D from −1 V to +1 V, LRS shows symmetric behavior for negative and positive polarity of V_D. While for HRS, the output curve is asymmetric, demonstrating V_D polarity-dependent reverse rectification behavior, where a current flows under negative V_D but not under positive V_D. The I_D–V_D curves remain almost unchanged after changing the roles of the two electrodes (as drain or source), as shown in supplementary Fig. S13. The corresponding changes of resistance in HRS and LRS are shown in supplementary Fig. S14. The rectifying output characteristics of the device are attributed to two almost symmetric back-to-back Schottky barriers, where the highest current arises from image force barrier lowering at the electrically forced junction (under negative V_D, the Schottky junction at the drain is reverse biased), while the reverse current is due to Schottky barrier-limited injection at the grounded junction (under positive V_D, the Schottky junction at the source is reverse biased). The electrons trapped in the Al_2O_3 deplete the channel (shifting the channel bands upward), making the rectification effect more pronounced.[66] To characterize the stability of the LRS and HRS under constant V_D with different polarities, we measured the time evolution of the I_D across the MoS_2 in HRS and LRS at $V_D = \pm 1$ V after setting by 300 ns +26 V and −20 V V_G pulses, respectively. As shown in Fig. 4(c), all four states remain stable after 100 s, indicating that changing the polarities of V_D does not affect the charge stored in the device. In HRS, the current level for $V_D = -1$ V and +1 V is $\sim 10^{-8}$ A and $\sim 10^{-13}$ A, respectively, suggesting a current rectification ratio over 10^5. The higher current at negative V_D indicates the reverse current rectification. We have also measured the time evolution of the I_D across the MoS_2 in HRS for different voltage amplitudes of V_D with positive and negative polarities after setting the device by a 300 ns +22 V V_G pulse. As shown in Fig. 4(d), for positive V_D with different amplitudes ($V_D = +0.1$ V, +0.5 V, and +1 V), the current remains at the level of $\sim 10^{-10}$ A. While for negative V_D ($V_D = -0.1$ V, −0.5 V, and −1 V), the current level is strongly dependent on the voltage amplitude, which is consistent with that shown in Fig. 4(b). Moreover, under $V_D = \pm 1$ V, the current remains unchanged even after 1000 s, further revealing that these states are stable with time. These results suggest that the current rectification ratio can be effectively tuned by varying the amplitudes of V_D. Within a certain range, a larger V_D amplitude corresponds to a higher ON/OFF ratio. On the other hand, the rectification ratio at $V_D = \pm 1$ V is $\sim 10^3$ after setting the device by a 300 ns +22 V $V_{G,pulse}$, while after setting the device by a 300 ns +26 V $V_{G,pulse}$, the rectification ratio at $V_D = \pm 1$ V increases to $\sim 10^5$ (Fig. 4(c)). This indicates that rectification ratios can also be regulated by varying the amplitudes of positive $V_{G,pulse}$, which essentially varies the amount of electrons trapped in Al_2O_3, resulting in varying degrees of depletion in the channel. The rectification ratios can also be regulated by altering negative $V_{D,pulse}$ to change the amount of electrons trapped in Al_2O_3 in the two-terminal operation mode.

Based on the current rectification capability of our direct charge trapping device, we further exploit it to function as gate-tunable rectifiers.[40–42,67] The 3D schematic of the circuit and the effective circuit diagram are shown in Fig. 4(e), in which a loading resistor of 10 GΩ is connected to the direct charge trapping device. The drain and source electrodes serve as the input (V_{in}) and output (V_{out}), respectively. The gate electrode functions as the control electrode, regulating rectification ratios by varying the $V_{G,pulse}$. As an example, we used a 300 ns +26 V $V_{G,pulse}$ to set the device to HRS. As shown in Fig. 4(f), under the input alternative triangular V_D wave with an amplitude of 2 V (V_{in}) (upper panel), only the negative input voltage can pass through (middle panel). When V_{in} is positive, $V_{out} = 0$ V, suggesting the successful reverse rectification behavior for the input alternative signal. While for the LRS set by applying a 300 ns −20 V V_G pulse, the output signal is identical to that of the input signal (lower panel), indicating the absence of rectification capability in LRS, which is consistent with the above results (Fig. 4(b)). As such, by applying specific positive and negative gate pulses, the rectifying behavior of the rectifier can be switched ON and OFF, thus creating what are known as gate-tunable rectifiers. However, in HRS, when the amplitude of the negative input voltage is smaller than 0.5 V, the output voltage becomes distorted, with an amplitude lower than the input value (supplementary Fig. S15). This is because, under smaller amplitude negative V_D, the decrease in resistance of the device is too small to be significantly lower than the series resistance.

Inspired by the synergistic modulation of the conductance of the MoS_2 channel by varying the polarity of V_D and V_G, we have constructed a ternary logic[40,68–70] device, as schematically shown in Fig. 4(g), in which the drain, gate, and source electrodes serve as the input 1 (IN1, V_{in1}), input 2 (IN2, V_{in2}), and output (OUT, V_{out}), respectively. A loading resistor of 10 GΩ is connected to the source electrode. An equivalent circuit diagram is shown in the lower panel. Figure 4(h) shows the time traces of the ternary logic device, in which −1 V represents logic "0", +1 V represents logic "1", and 0 V represents logic "X", the intermediate logical state. The OUT depends on the voltage distribution between the effective resistance of the device and the 10 GΩ series resistance. As long as the MoS_2 channel is switched ON by applying negative V_D ($V_{in1} = -1$ V, IN1 = 0), regardless of the logic state of the V_G ($V_{in2} = -1$ V or +1 V, IN2 = 0 or 1), the output follows the voltage of V_{in1}, resulting in $V_{out} = -1$ V (OUT = 0).

When applying positive V_D ($V_{in1} = +1$ V, IN1 = 1), the conductance of the MoS_2 channel is modulated by V_G (V_{in2}). For $V_{in2} = +1$ V, the MoS_2 channel is switched ON, the output still follows that of V_{in1}, resulting in $V_{out} = +1$ V (OUT = 1). While for $V_{in2} = -1$ V, the MoS_2 channel is switched OFF, $V_{out} = 0$ V (OUT = X). The truth table of the ternary logic is shown in Fig. 4(i). Apparently, it can be observed that this ternary logic behaves similarly to AND logic where the output is "1" only if both inputs are "1". The difference lies in that when IN1 = 1 and IN2 = 0, the output shows an intermediate logic state X. The ability of ternary logic to handle more states per logic gate and provide intermediate logic states opens up new possibilities for innovation and efficiency in various technological fields. This feature enables more sophisticated processing and decision-making in a range of applications, from AI systems to embedded devices.[71]



Q	IN1	IN2	OUT
1	0	0	0
2	1	0	X
3	1	1	1
4	0	1	0

Fig. 4. Gate-tunable reverse rectifiers and ternary logic devices based on direct charge trapping devices. (a) Dual-sweeping transfer curves of the direct charge trapping device at $V_D = -1$ V, +1 V and 0.1 V within the 15 V $V_{G,MAX}$ sweeping range. The arrows show the sweeping directions of V_G. The leakage currents (I_G) under different drain biases are also shown. (b) The I_D–V_D curves of the direct charge trapping device in HRS and LRS after applying 300 ns V_G positive and negative pulses, respectively. A reverse current rectification behavior, where a current flows under negative V_D but not under positive V_D, is observed in HRS, while it is absent in LRS which allows current to flow in both directions without rectification. (c) Time evolution of the I_D across the MoS_2 in HRS and LRS at V_D of ±1 V after applying 300 ns +26 V and −20 V V_G pulses. (d) Time evolution of the I_D across the MoS_2 in HRS at V_D of ±0.1 V, ±0.5 V and ±1 V after applying a 300 ns +22 V V_G pulse, indicating V_D-amplitude-dependent reverse current rectification. (e) The upper panel shows the 3D schematic of the reverse current rectifier circuit. A loading resistor of 10 GΩ is connected to the direct charge trapping device. The drain and source electrodes serve as the input (V_{in}) and output (V_{out}), respectively. The gate electrode functions as the control electrode, regulating rectification ratios by varying the $V_{G,pulse}$. The lower panel shows the equivalent circuit diagram of the rectifier. (f) Output rectifying characteristics (V_{out}) of the direct charge trapping device in HRS and LRS set by 300 ns positive and negative V_G pulses, respectively. The input alternative triangular wave with an amplitude of 2 V (V_{in}) is also shown. (g) The upper panel shows the 3D schematic of the circuit of the dual-input ternary logic device. A loading resistor of 10 GΩ is connected to the direct charge trapping device. The drain, control gate and source electrodes serve as the input1 (IN1, V_{in1}), input2 (IN2, V_{in2}) and output (OUT, V_{out}), respectively. The lower panel shows the equivalent circuit diagram of the ternary logic device. (h) Time traces of the ternary logic device. Here, −1 V represents logic 0, +1 V represents logic 1, and 0 V represents logic X. (i) The truth table of the dual-input ternary logic.

3. Conclusion

In summary, we have demonstrated an ultrafast reconfigurable direct charge trapping device based on few-layer MoS_2 for memory, rectifier and ternary logic. The direct charge trapping device features a simple structure with only the MoS_2 channel and the Al_2O_3 trapping layer. Confirmed by dual-sweeping transfer curves with different gate-voltage sweeping rates and photoluminescence (PL) spectra, the rich defect states within Al_2O_3 can directly trap charges to modulate the MoS_2 channel. The direct charge trapping device shows exceptional performance in both three-terminal and two-terminal operation modes, which is characterized by an ultrafast three-terminal operation speed ($\sim$300 ns), an extremely low OFF current of 10^{-14} A, a high ON/OFF current ratio of up to 10^7, and stable retention and endurance properties. Furthermore, the device with a simple symmetrical structure exhibits V_D polarity-dependent reverse rectification behavior in HRS, where negative V_D significantly increases the current of MoS_2. The reverse current rectification ratio can be tuned by both the number of electrons trapped in Al_2O_3 and the amplitude of V_D. With V_D at $\pm$1 V, the rectification ratio reaches $\sim 10^5$ after setting the device by a 300 ns $+$26 V $V_{G,pulse}$. Leveraging this rectification behavior, a gate-tunable reverse rectifier is implemented with a series 10 GΩ loading resistor. Treating the V_D and V_G of the rectifier as inputs and V_S as the output, a ternary logic resembling AND logic gate can be achieved through the synergistic modulation of the MoS_2 channel by V_D and V_G. The simplicity of this device structure, its compatibility with silicon-based manufacturing technologies, and its diverse functionalities make it a promising contender for future electronic devices.

Appendix A: Experimental details

Device fabrication The bottom gate was patterned using e-beam lithography (EBL) and a 5 nm/50 nm Cr/Au stack was deposited using e-beam evaporation on the silicon substrate with a 300 nm-thick SiO_2 thermal oxide film. A 30 nm Al_2O_3 trapping layer was grown by Cambridge NanoTech Savannah 100 Atomic Layer Deposition System (ALD). During the ALD process, trimethylaluminum (TMA) reacted with water at 150 °C to form Al_2O_3. Then mechanically exfoliated few-layer MoS_2 was transferred to the Al_2O_3 trapping layer using a dry-transfer approach with PDMS as the transfer medium. Next, drain–source contacts were patterned by EBL and a 5 nm/50 nm thick Cr/Au stack was deposited using e-beam evaporation. Finally, the device was immersed in acetone for the lift-off process.

Materials characterization PL spectroscopies were mainly performed by a HORIBA LabRAM HR Evolution Raman microscope. The signals were excited using the 325 nm laser focused by a 75$\times$ microscope objective. The laser power was set to 5 mW. AFM height measurements were conducted using an Asylum Research Cypher S AFM in tapping mode.

Electrical tests All electrical characterization was conducted at room temperature in air under dark conditions in a probe station connected to a semiconductor device parameter analyzer (Keithley 4200A-SCS).

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