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A physical memristor model for Pavlovian associative memory

Jiale Lu(卢家乐)[†], Haofeng Ran(冉皓丰), Dirui Xie(谢頔睿), Guangdong Zhou(周广东)[‡], and Xiaofang Hu(胡小方)[§]

College of Artificial Intelligence, Southwest University, Chongqing 400712, *China*

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Brain-inspired intelligence is considered to be a computational model with the most promising potential to overcome the shortcomings of the von Neumann architecture, making it a current research hotspot. Due to advantages such as nonvolatility, high density, low power consumption, and high response ratio, memristors are regarded as devices with promising applications in brain-inspired intelligence. This paper proposes a physical Ag/HfO_x/FeO_x/Pt memristor model. The Ag/HfO_x/FeO_x/Pt memristor is first fabricated using magnetron sputtering, and its internal principles and characteristics are then thoroughly analyzed. Furthermore, we construct a corresponding physical memristor model which achieves a simulation accuracy of up to 99.72% for the physical memristor. We design a fully functional Pavlovian associative memory circuit, realizing functions including generalization, primary differentiation, secondary differentiation, and forgetting. Finally, the circuit is validated through PSPICE simulation and analysis.

Keywords: memristor model, Pavlovian associative memory circuit, secondary differentiation

PACS: 87.19.lv, 84.30.Bv, 84.30.–r

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1. Introduction

With the continuous increase in computing demands and the development of emerging technologies, the issues with the von Neumann architecture have become more prominent, especially in memory bottleneck, energy consumption, heat dissipation, and the lack of intelligence and adaptability.[1–3] In order to overcome the limitations of the von Neumann architecture, researchers have begun to explore and research new computing models and system architectures. Brain-inspired intelligence is a computational model that mimics the structure and function of the human brain. Compared to the traditional von Neumann architecture, it has advantages such as low power consumption, parallel processing, adaptive learning, and pattern recognition.[4–7] However, the neural network structure of the human brain is complex, containing billions or even trillions of neurons and trillions of synapse connections. Therefore, finding suitable devices to simulate human brain synapses is crucial.

Memristors possess many advantages, including resistance switching, low power consumption, high density, high response ratio, and nanoscale capabilities, making them ideal devices for simulating human brain synapses.[8,9] Since the first experimentally verified memristor was manufactured by researchers at HP Labs in 2008, various types of memristors have been fabricated.[10,11] Among them, memristors with metal–oxide–metal (MIM) structures have been widely studied for their high response ratio, low power consumption, high density, and stability.[12] In 2013, Muhammad *et al*. fabricated an Ag/ZnO/Cu memristor with a maximum switching ratio of up to 10^3, demonstrating good durability and stability.[13] In 2021, a novel memristor based on WS_2/MoS_2 2D semiconductor heterostructures was proposed, with a maximum switching ratio of up to 10^4, exhibiting advantages of low power consumption and durability, with the potential to realize large-scale memristor crossbar arrays.[14] In 2023, Li *et al*. proposed a strategy for the electron beam irradiation treatment of the complete lattice structure of h-BN memristors, fabricating memristors with a switching ratio of 10^8 and a good resistance switching curve, which provides a new approach for researchers to fabricate memristors with excellent performance.[15] However, the above-mentioned memristors suffer from poor synaptic plasticity, low accuracy, and poor durability. The Ag/HfO_x/FeO_x/Pt memristor fabricated in this work exhibits analog resistive-switching (RS) storage behavior, with high switching ratio ($> 10^4$), outstanding durability ($> 10^4$ cycles), high accuracy (> 6 bits), and excellent synaptic plasticity, which can simulate human brain synapses well.

However, due to the drawbacks of complex fabrication processes, high production costs, and instability, memristors cannot be widely deployed for large-scale applications. Memristor modeling is based on the internal principles of physical memristors to simulate real devices. Therefore, most applied research is conducted based on memristor models.[16] In 2009, a linear ion drift model was proposed in reference,[17] but it failed to effectively simulate the non-linear behavior of memristors. Furthermore, Biolek *et al*. introduced a nonlinear ion

[†]Corresponding author. E-mail: krislu_111@163.com
[‡]Corresponding author. E-mail: zhougd@swu.edu.cn
[§]Corresponding author. E-mail: huxf@swu.edu.cn

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drift model that could better simulate the non-linear behavior of memristors, although it lacked precision.[18] Subsequently, a more accurate Simmons tunneling model was proposed, but it was complex and computationally inefficient.[19] Inspired by Ref. [18], the TEAM and VTEAM models were successively proposed, known for their simplicity, efficiency, and accuracy. However, they still could not precisely simulate the complex non-linear behavior in some memristors.[20,21] Yakopcic *et al*. proposed an accurate, comprehensive, and automated memristor modeling method that could precisely simulate various MIM memristors.[22] References [23–25] achieved accurate simulation of real physical memristors based on the space charge-limited current mechanism (SCLC).[26] Reference [27] designed a memristive spiking neural network based on an ideal memristor model to realize a fully functional Pavlov experiment, which possesses learning, correcting, and forgetting capabilities. However, there is limited research on modeling based on the Frenkel–Poole (F-P) tunneling physical mechanism of MIM memristors.[28] In this paper, we construct a physical Ag/HfO_x/FeO_x/Pt memristor model based on the F-P tunneling physical mechanism. Our main contributions are summarized as follows.

1) The Ag/HfO_x/FeO_x/Pt memristor is fabricated using direct current sputtering and alternating current sputtering methods. Detailed electrochemical analysis and internal principle analysis are conducted on this memristor, which is characterized by high switching ratio, durability, high precision, and synaptic plasticity.

2) Based on the principle analysis in (1), the modeling of the Ag/HfO_x/FeO_x/Pt memristor is completed, and this model can effectively simulate the real physical device. Subsequently, a simulation analysis is conducted to validate the accuracy of the model.

3) Utilizing the advantages of the Ag/HfO_x/FeO_x/Pt memristor model, we design a fully functional Pavlov associative memory circuit, which possesses learning, generalization, primary differentiation, secondary differentiation, and forgetting functions.

2. Fabrication process

A silicon dioxide substrate is subjected to sequential ultrasonic cleaning using Decon 90, deionized water, acetone, and ethanol. The bottom electrode, switch functional layer, and top electrode are fabricated using high-purity (greater than 99%) Pt, Fe_2O_3, HfO_2, and Ag target materials, respectively. Deposition of the silver electrode is carried out under 0.9 Pa Ar using the direct current sputtering mode at a power of 15 W, completing the process within 30 s. Subsequently, utilizing the direct current sputtering mode at 0.9 Pa Ar and 20 W, the deposition of the Pt electrode is accomplished within 50 s. The switch functional layer of FeO_x is deposited using the radio-frequency sputtering mode under 1.0 Pa Ar, with a power of 100 W and a deposition time of 120 min. Meanwhile, the deposition of the switch functional layer of HfO_x is conducted under 1.0 Pa Ar, utilizing a radio-frequency sputtering mode at a power of 60 W, with a deposition time of 80 min. All sputtering processes are conducted under a background vacuum pressure of 5.0×10^4 Pa.

3. Memristor model

3.1. Principle analysis

After the fabrication of the memristor, the performance of Ag/HfO_x/FeO_x/Pt is tested (Fig. 1). It can be observed from the figure that the memristor exhibits a high switching ratio, favorable threshold characteristics, and strong non-linearity, making it well-suited for practical circuit applications. Based on the working principles of the internal structure of the memristor, we establish an energy band structure for the Ag/HfO_x/FeO_x/Pt memristor to explain the observed self-rectifying resistance switching (RS) memory behavior. This self-rectifying phenomenon is attributed to the natural barriers formed between Ag/HfO_x, HfO_x/FeO_x, and FeO_x/Pt. Each stage is described in detail below.

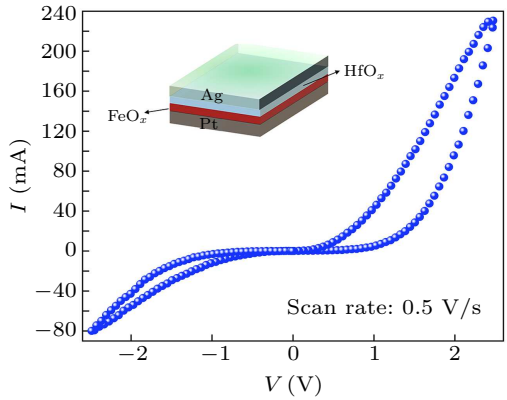


Fig. 1. Performance testing of the Ag/HfO_x/FeO_x/Pt memristor. The scanning voltage amplitude is 2.5 V and the frequency is 0.5 V/s.

First stage (Fig. 2(a)): At low electric fields, electrons lack sufficient kinetic energy to overcome the barrier produced by Ag/HfO_x. Consequently, in the rectification region (E_{rectify}), the Ag/HfO_x/FeO_x/Pt memristor exhibits a high-resistance state (HRS).

Second stage (Fig. 2(b)): At relatively high electric fields, some injected electrons overcome the barrier and are either trapped in the traps or enter the metal electrode, leading to an increase in current ($E > E_{\text{rectify}}$). This indicates that the injected electrons have enough energy to overcome the barrier.

Third stage (Fig. 2(c)): Most traps are filled, forming a path based on electron conduction. Therefore, at high electric field intensities, the memristor enters a low-resistance state (LRS) ($E \gg E_{\text{rectify}}$).

Fourth stage (Fig. 2(d)): When applying a reverse electric field, the memristor exhibits a high current value due to nearly free electron transmission and contributions from electrons escaping shallow traps. In this case, the recovery of shallow trap sites results in an increased resistance, while the contribution of escaping electrons leads to an increase in current. Before entering the rectification region, the contribution of escaping electrons exceeds the number of recovered trap sites.

Fifth stage (Fig. 2(e)): Due to the recovery of a large number of trap sites formed in the fourth stage, the barrier gap between Ag and HfO_x layers widens. Therefore, when entering the rectification region, injected electrons do not have enough energy to overcome the barrier, causing the majority of trap sites to be recovered and resulting in an extremely high resistance value for the memristor.

Sixth stage (Fig. 2(f)): Electrons injected from the Pt electrode successfully overcome the barrier between Pt and FeO_x (1.43 eV), enter the conduction band, and some are trapped in traps under low negative electric fields. It is noteworthy that the barrier between HfO_x and FeO_x layers exceeds 2.02 eV and does not form a path based on electron conduction in the negative rectification region, resulting in an extremely high resistance value.

Seventh stage (Fig. 2(g)): Injected electrons gradually fill trap sites, raising the Fermi level, thereby reducing the barrier width between HfO_x and FeO_x layers. In this situation, injected electrons can freely transmit between the two electrodes.

Eighth stage (Fig. 2(h)): Similarly, electrons in shallow traps that can easily transition to the conduction band increase the current under a high reverse electric field. Therefore, despite the recovery of shallow trap sites to an empty state, high current values are still observed.

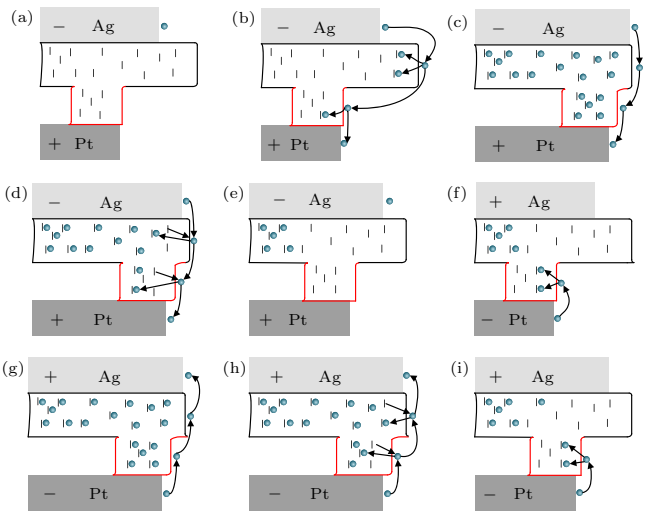


Fig. 2. Schematic diagram of the physical mechanism of the Ag/HfO_x/FeO_x/Pt memristor. The small blue circles represent electrons, the silver parts represent the Ag electrode, and the gray-black part represents the Pt electrode.

Ninth stage (Fig. 2(i)): As the electric field strength decreases and the number of empty trap sites increases, injected electrons are strictly restricted by the barrier potential between HfO_x and FeO_x layers, and the memristor remains in HRS.

Based on the above analysis, the Ag/HfO_x/FeO_x/Pt memristor satisfies F-P tunneling,[26] which is the process where electrons conduct through defect energy levels in the oxide insulating layer under the influence of an electric field, with the tunneling current density satisfying

$$J_{\mathrm{FP}} = \sigma E \exp\left(\frac{\beta_{\mathrm{FP}}}{k_{\mathrm{B}}T}E^{\frac{1}{2}} - \frac{q\phi_{\mathrm{P}}}{k_{\mathrm{B}}T}\right). \tag{1}$$

In the equation, $\beta_{\mathrm{FP}} = \sqrt{\frac{q^3}{\pi\varepsilon_{\mathrm{r}}\varepsilon_0}}$, where σ, k_{B}, T, E, ϕ_{P} , ε_{r} and ε_0 represent the conductivity coefficient, Boltzmann constant, temperature, electric field strength, trap energy level barrier, electron mass, thin film relative dielectric constant, vacuum dielectric constant, and electron charge, respectively. Taking the logarithm on both sides, it can be known that the equation satisfies the relationship $\ln(J) \propto E$.

3.2. Model construction

Based on the above principle analysis, this paper completes the construction of the physical model of the Ag/HfO_x/FeO_x/Pt memristor by improving the current–voltage relationship and window function in Ref. [21]. The current–voltage relationship can be described as

$$I(t) = \begin{cases} a_1 x(t)\sinh(b_1 V(t)), & V(t) \geq 0, \\ a_2 x(t)\sinh(b_2 V(t)), & V(t) < 0, \end{cases} \tag{2}$$

where $x(t)$ represents the state variable, $I(t)$ denotes the current flowing through the memristor, $V(t)$ represents the voltage applied at both ends of the memristor, a_1, a_2, b_1, and b_2 are model fitting parameters. The parameters a_1 and a_2 are used to control the amplitude of the input voltage, and b_1 and b_2 are used to control the conductivity and the strength of the threshold function related to the voltage magnitude.

The derivative equation of the state variable is as follows:

$$\frac{\mathrm{d}(x(t))}{\mathrm{d}t} = g(V(t))f(x(t)), \tag{3}$$

where the function $g(V(t))$ is used to control the threshold voltage, and the window function $f(x(t))$ is used to control the state variable within the range of [0,1]. The equation for $g(V(t))$ can be described as

$$g(V(t)) = \begin{cases} A_{\mathrm{p}}(\mathrm{e}^{V(t)} - \mathrm{e}^{V_{\mathrm{off}}}), & V(t) > V_{\mathrm{off}}, \\ 0, & -V_{\mathrm{on}} \leq v \leq V_{\mathrm{off}}, \\ -A_{\mathrm{n}}(\mathrm{e}^{-V(t)} - \mathrm{e}^{V_{\mathrm{on}}}), & V(t) < -V_{\mathrm{on}}, \end{cases} \tag{4}$$

where V_{off} and V_{on} represent the positive and negative threshold voltages, respectively. A_{p} and A_{n} are fitting parameters

used to control the rate of change of the state variable. The window function $f(x(t))$ is represented by

$$f(x(t)) = \begin{cases} f_{\text{off}}(x) = \exp\left[-\exp\left(\dfrac{x - a_{\text{off}}}{x_{\text{c}}}\right)\right], & V(t) > V_{\text{off}}, \\ f_{\text{on}}(x) = \exp\left[-\exp\left(\dfrac{a_{\text{on}} - x}{x_{\text{c}}}\right)\right], & V(t) \le -V_{\text{on}}, \end{cases} \tag{5}$$

where a_{off} , a_{on}, and x_{c} are the fitting parameters.

3.3. Simulation verification

In order to make the established memristor model better simulate real devices, this work uses the stochastic gradient descent method to minimize the relative error function. The relative root mean square error (RRMSE) is chosen as the error function:

$$E_{\text{RMS}} = \sqrt{\frac{1}{N} \cdot \left(\frac{\sum_{i=1}^{N} (V_{\text{model},i} - V_{\text{ref},i})^2}{\overline{V}_{\text{ref}}^2} + \frac{\sum_{i=1}^{N} (I_{\text{model},i} - I_{\text{ref},i})^2}{\overline{I}_{\text{ref}}^2} \right)}, \tag{6}$$

where N represents the number of samples, $V_{\text{model},i}$ and $I_{\text{model},i}$ represent the voltage and current data fitted by the model, $V_{\text{ref},i}$ and $I_{\text{ref},i}$ represent the voltage and current data of the measured real device, and $\overline{V}_{\text{ref}}$ and $\overline{I}_{\text{ref}}$ represent the Euclidean norm of the voltage and current in the measured data.

The fitting parameters of the model are shown in Table 1, and the fitting curve is shown in Fig. 3. It can be observed from the figure that the constructed memristor model can simulate the real physical device well, with an RRMSE of 0.28% and a high on-off ratio of 10^4.

Table 1. Model fitting parameters.

Parameter	R_{on}	R_{off}	V_{on}	V_{off}	a_1	a_2	b_1	b_2	a_{on}	a_{off}	A_{n}	A_{p}	x_{c}	E_{RMS}
Value	10 Ω	10 kΩ	0.1 V	0.5 V	0.2693	0.0591	1.1598	1.3692	–0.9501	1.1362	0.0022	20.4649	–0.4843	0.28%

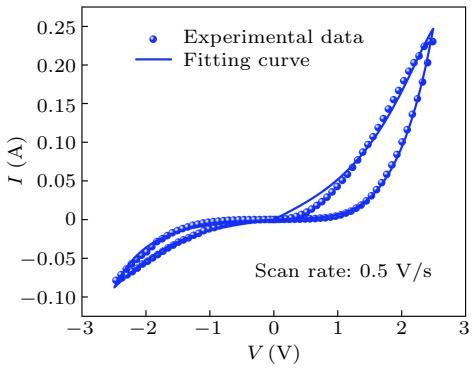


Fig. 3. Model fitting curve.

Table 2 provides a comparison summary of different memristor models. The linear ion drift model[16] and the nonlinear ion drift model[17] are the simplest but have lower accuracy and do not consider issues such as boundary effects. The Simmons tunneling model[18] has higher accuracy but is the most complex and not conducive to calculation. The TEAM[19] and VTEAM[20] models are simple and efficient, but the physical mechanism is unclear and the accuracy is not high enough, and they cannot simulate complex nonlinear behaviors. The memristor model proposed in Ref. [21] based on the SCLC mechanism has a threshold effect and solves the boundary problem, but the model's accuracy is moderate. Furthermore, this paper proposes an Ag/HfO$_x$/FeO$_x$/Pt memristor model based on the F-P tunneling mechanism, which has threshold characteristics and higher nonlinearity, and alleviates the boundary effect. While maintaining model simplicity, it improves accuracy, with an RRMSE of 0.28%. Compared to other models, this model can simulate physical memristors better.

Table 2. Comparison summary of different memristor models: IMT represents ion migration theory; QTT represents quantum tunneling theory; SCLC represents space charge limited current mechanism; F-P represents trap level tunneling physical mechanism.

Reference	[16]	[17]	[18]	[19]	[20]	[21]	Ours
State variable	$0 \le x \le D$	$0 \le x \le 1$	$a_{\text{off}} \le x \le a_{\text{on}}$	$a_{\text{off}} \le x \le a_{\text{on}}$	$a_{\text{off}} \le x \le a_{\text{on}}$	$0 \le x \le 1$	$0 \le x \le 1$
Physical mechanism	IMT	IMT	QTT	ambiguous	ambiguous	SCLC	F-P
Control mechanism	current	voltage	current	current	voltage	voltage	voltage
I–*V* relationship	explicit	explicit	ambiguous	explicit	explicit	explicit	explicit
Threshold effect	no	no	yes	yes	yes	yes	yes
Boundary effect	unsolved	solved	solved	solved	solved	solved	solved
Model complexity	easy	medium	complex	medium	medium	medium	medium
Model accuracy	lowest	low	highest	medium	medium	medium	high

4. Pavlov associative memory circuit based on Ag/HfO$_x$/FeO$_x$/Pt memristor

4.1. Memristor neural network structure

The memristor neural network structure designed in this paper is shown in Fig. 4, where N_1, N_2, N_3 and N_4 are input neurons, N_5 is the output neuron, and w_{15}, w_{25}, w_{35}, and w_{45} are the synaptic weights between them. N_1, N_2, N_3 and N_4 can only be activated by these specific stimuli, namely, food, 600 Hz bell, 600 Hz buzzer, and 400 Hz bell. If N_5 is activated, salivation response will occur. The relationship between

food and salivation response is inherent, so w_{15} is set to a high weight, represented by resistor R_1. In the initial state, since the bell and buzzer will not cause salivation response, w_{25}, w_{35}, and w_{45} are set to high weights, represented by memristors M_1, M_2, and M_3, respectively. After some training, the bell (500 Hz, 400 Hz) and the buzzer (500 Hz) will activate N_5, causing salivation response, which is the generalization process. Primary differentiation refers to further distinguishing the bell (600 Hz, 400 Hz) and the buzzer (600 Hz) based on generalization. After further training, the bell (500 Hz) and the bell (400 Hz) are distinguished, and only the bell (600 Hz) will cause salivation response, which is secondary differentiation. Then, the forgetting function is implemented. After inputting the bell (600 Hz) alone for a certain number of times, N_5 is no longer activated and no salivation response occurs.

Figure 5 illustrates the five processes of Pavlov associative memory, including testing, generalization, primary differentiation, secondary differentiation, and forgetting. Figure 5(a) is the testing process. Under the initial condition, when stimulated by food, neuron N1 is activated. Since w_{15} is a high weight, neuron N_5 is activated, and the dog instinctively produces a salivation response, which is an unconditional reflex, so food is an unconditional stimulus. When stimulated by the bell (600 Hz, 400 Hz) and the buzzer (600 Hz), neurons N_2, N_3 and N_4 are activated, respectively, but w_{25}, w_{35}, and w_{45} are low weights, neuron N_5 is not activated, and the dog does not produce a salivation response. Therefore, the bell and buzzer are neutral stimuli at this time.

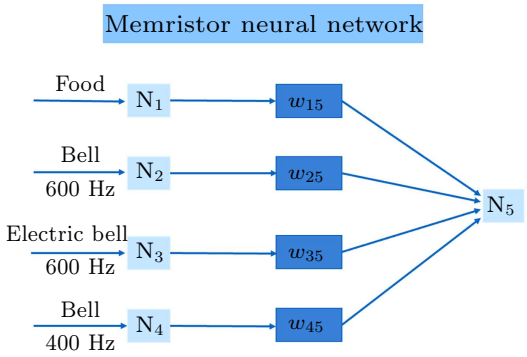


Fig. 4. Diagram of the memristor neural network structure.

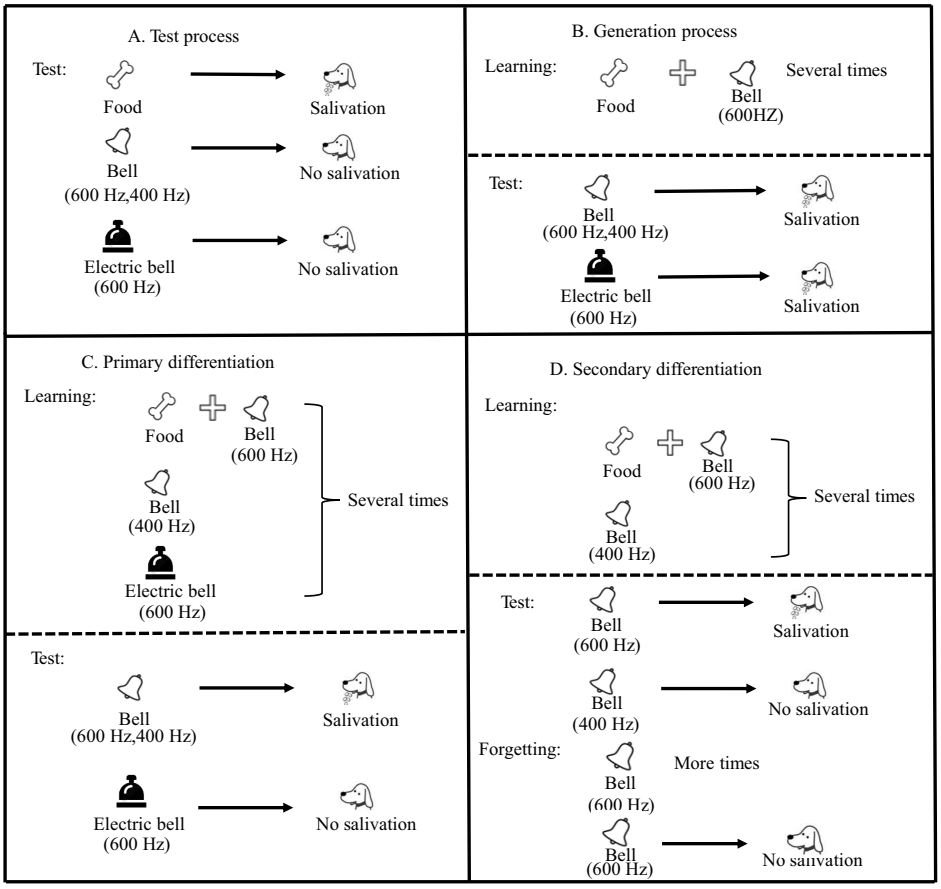


Fig. 5. Diagram of the memristor neural network structure.

As shown in Fig. 5(b), process B introduces the generalization process. When the dog is stimulated by food and bell (600 Hz) at the same time, neuron N_1 and neuron N_2 are activated, w_{25}, w_{35}, and w_{45} increase, and neuron N_5 is always activated, and the dog produces a salivation response, which is the learning process of classical conditioning. After a certain amount of learning, when the dog is only stimulated by the bell (600 Hz), neuron N_2 is activated. At this time, w_{25} is a high weight, neuron N_5 is activated, and the dog produces a salivation response. This indicates that classical conditioning has

been formed and the bell (600 Hz) has become a conditional stimulus. Similarly, when the dog is separately stimulated by the bell (600 Hz) and the buzzer (400 Hz), w_{35} and w_{45} are high weights, and neuron N_5 will also be activated, producing a salivation response.

Figure 5(c) introduces the primary differentiation process in detail based on achieving generalization. First, food and bell (600 Hz) stimuli are applied simultaneously to the dog. Neurons N_1 and N_2 are activated, w_{25}, w_{35}, and w_{45} continue to increase, and the connections between neurons N_2, N_3, N_4 and N_5 are strengthened. Then, the electric bell (600 Hz) stimulation is applied separately. Neuron N_3 is activated. w_{35} decreases and the synaptic connection between neurons N_3 and N_5 is weakened. Repeat the above experimental process a few times. Then, w_{35} becomes lower, while w_{25} and w_{45} are still high weights. The test results show that when the dog is only stimulated by the buzzer (600 Hz), neuron N_5 will not be activated, and the dog will not produce a salivation response. Since the tone of the bell (400 Hz) is similar to the bell (600 Hz), when the dog is stimulated by the bell (400 Hz), neuron N_5 will still be activated, producing a salivation response. Primary differentiation distinguishes different timbre based on generalization without separating the bells of the same timbre but different pitches.

The secondary differentiation and forgetting processes are illustrated in Fig. 5(d), which serves to further differentiate between bells of the same timbre but different pitches. During the learning process, both food and bell (600 Hz) stimuli are simultaneously presented to the dog, and the synaptic weight change process mirrors that of the generalization process depicted in Fig. 5(c). Subsequently, when the bell (400 Hz) stimulus is exclusively used on the dog, neuron N_4 becomes activated, leading to a decrease in w_{35} and w_{45}, as well as a weakening of the connection between neuron N_4 and N_5. After several repetitions of this training, w_{45} reaches a low weight. Test results demonstrate that when the dog is exposed to the bell (600 Hz) stimulus, neuron N_5 consistently activates, eliciting a salivation response. However, when presented with the bell (400 Hz) stimulus, neuron N_5 remains inactive, resulting in no salivation response. Consequently, the distinction between bells of the same timbre but different pitches is achieved, marking the realization of secondary differentiation. The forgetting process is further implemented, building on this foundation. Through continuous exposure to the bell (600 Hz) stimulus alone, w_{25} decreases and the connection between N_2 and N_5 weakens. After several cycles, w_{25} reaches a low weight. Upon subsequent exposure to the bell (600 Hz), neuron N_5 fails to activate, and the dog does not exhibit a salivation response.

4.2. Circuit implementation

(1) Complete circuit design: Based on the multi-mode generalization and differentiation associative memory memristor neural network and experimental process introduced in Subsection 4.2, a full-function Pavlov associative memory circuit has been designed, as shown in Fig. 6. The entire circuit consists of a control module, a synapse module, and an output module. The voltage control module integrates logic gates, NMOS transistors, PMOS transistors, and other components, which are responsible for regulating and controlling the input voltage. The synaptic module is mainly composed of an amplifier and a memristor, whose function is to simulate the learning and forgetting mechanism of biological synapses, thus realizing the Pavlovian associative memory function. Finally, the output module completes the signal output through the contingency gate circuit. Detailed descriptions of the design and workflow of each module will be provided in (2) and (3). U_1–U_4 are all logic gates in the circuit, where U_1 and U_3 are two-input AND gates (model: 74LS08), U_2 is a NOT gate (model: 74LS04), and U_4 is an OR gate (model: 74LS02). The initial values of memristors M_1, M_2, and M_3 are all set to HRS (9999 Ω). All devices in the entire circuit are from the PSPICE library and are simulated and analyzed in the PSPICE software.

(2) Voltage control module: The voltage control module is shown in Fig. 7. Here, N_1, N_2, N_3 and N_4 represent the input signals for food, bell (600 Hz), electric bell (600 Hz), and bell (400 Hz), respectively. The comparator COMP1 functions to compare thresholds and is implemented using NMOS and PMOS. The NMOS used is the M2N7000 model from the PWRMOS library (with a threshold voltage of approximately 1.73 V), while the PMOS used is the IRF9140 model from the PWRMOS library (with a threshold voltage of about −3.67 V). COMP2, COMP3, and COMP4 are all implemented using NMOS transistors, utilizing the M2SK530 model from the JPWRMOS library (with a threshold voltage of approximately 2.3 V). The threshold voltage for COMP1 is 0.73 V, with the source–drain voltage for NMOS and PMOS being −1 V and 3 V, respectively. The output voltage is represented by

$$V_{\mathrm{COMP1}} = \begin{cases} 0\ \mathrm{V}, & 0 \le V_{\mathrm{IN1}} \le 0.73\ \mathrm{V}, \\ 3\ \mathrm{V}, & V_{\mathrm{IN1}} > 0.73\ \mathrm{V}. \end{cases} \tag{7}$$

When the input voltage V_{IN1} is less than 0.73 V, $V_{\mathrm{IN1}} - (-1\ \mathrm{V}) \le 1.73$ V, which is less than the output threshold of the NMOS transistors, so the NMOS transistors outputs 0 V. and when 0 V is input to the PMOS transistors, $-3\ \mathrm{V} - (0\ \mathrm{V}) > -3.67$ V, which is greater than the threshold value of the PMOS transistors −3.67 V, so the COMP1 outputs 0 V. When the input voltage V_{IN1} is greater than 0.73 V, $V_{\mathrm{IN1}} - (-1\ \mathrm{V}) > 1.73$ V, while the NMOS transistors outputs −1 V. When −1 V is input to the PMOS transistors, $-3\ \mathrm{V} - (-1\ \mathrm{V}) > -3.67$ V, which is less than the threshold value of the PMOS transistors −3.67 V, and COMP1 outputs −3 V.

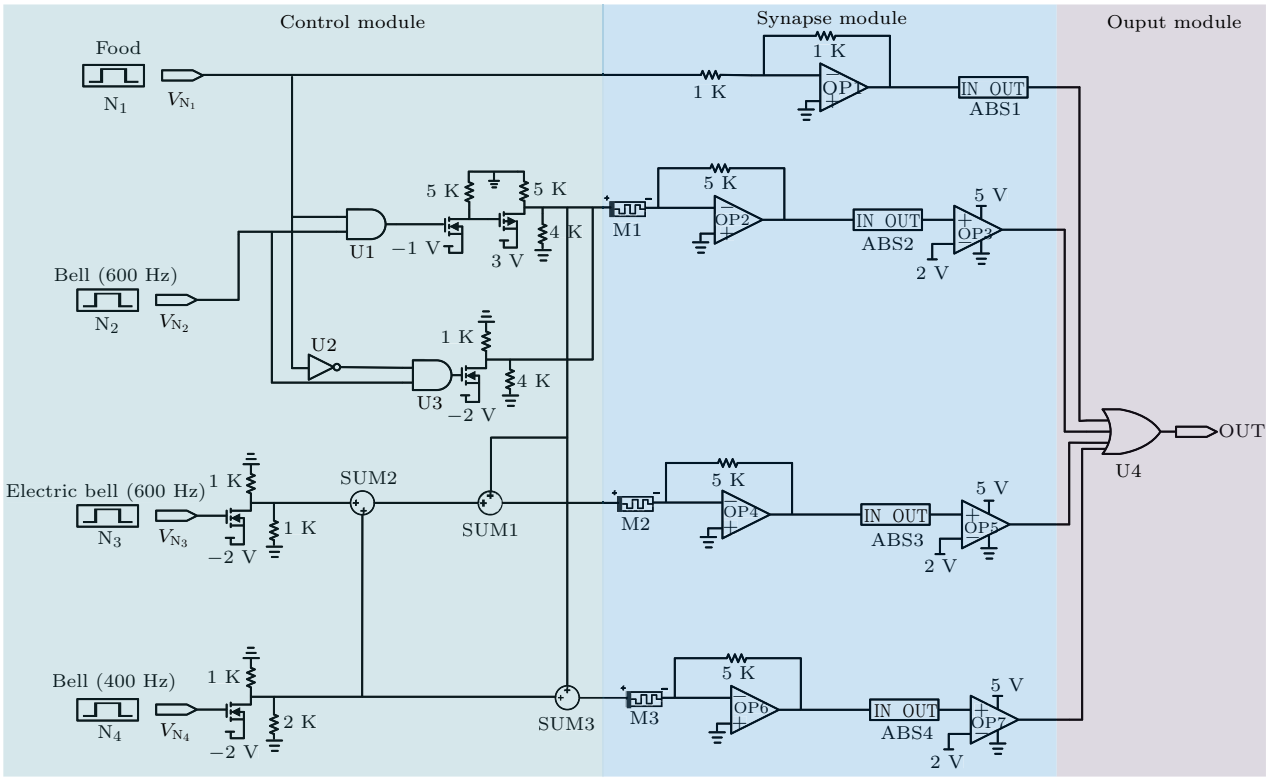


Fig. 6. Complete circuit structure.

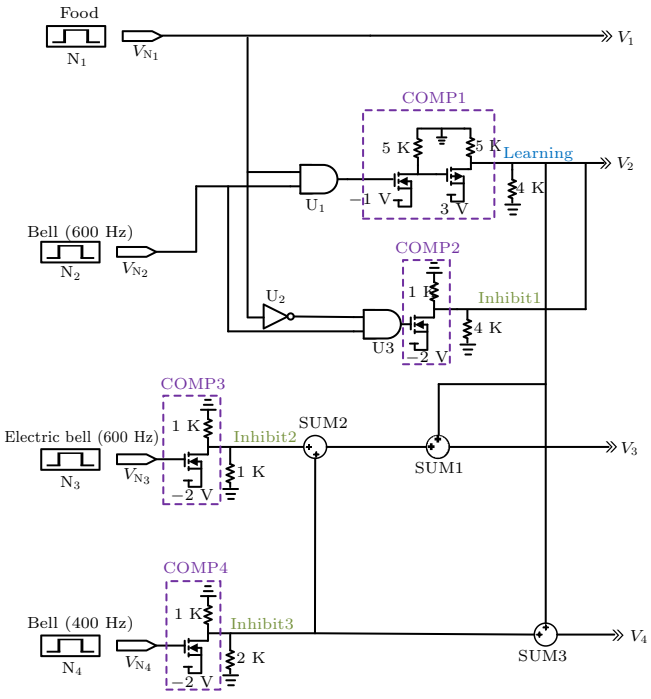


Fig. 7. Diagram of voltage control module circuit.

The threshold voltages of COMP2, COMP3, and COMP4 are all 0.3 V, where the source–drain voltage of the NMOS transistor is −2 V. Their output voltages are represented by

$$V_{\mathrm{COMP2}} = \begin{cases} 0\ \mathrm{V}, & 0 \le V_{\mathrm{IN2}} \le 0.3\ \mathrm{V}, \\ -2\ \mathrm{V}, & V_{\mathrm{IN2}} > 0.3\ \mathrm{V}. \end{cases} \tag{8}$$

When the input voltage $V_{\mathrm{IN2}} \le 0.3$ V, $V_{\mathrm{IN2}} - (-2)\ \mathrm{V} \le 2.3$ V, which is less than the threshold voltage of the NMOS tube, so the output is 0 V. When the input voltage $V_{\mathrm{IN2}} > 0.3$ V, the voltage $V_{\mathrm{IN2}} - (-2)\ \mathrm{V} > 2.3$ V, and output is −2 V. The operational workflow of the voltage control module mainly comprises the following five cases, which are detailed as follows:

1. When only the food signal is input, neuron N_1 is activated, and the input voltage V_{N_1} is 3 V, at which point the voltage V_1 is also 3 V. V_{N_2}, V_{N_3} and V_{N_4} are all 0 V with no other signals input. As a result, logic gates U_1 and U_3 output a low level. COMP1, COMP2, COMP3, and COMP4 are all closed, and the voltages V_2, V_3 and V_4 are all 0 V.

2. When only the bell (600 Hz) signal is input, neuron N_2 is activated, and the input voltage V_{N_2} is 3 V, while V_{N_1}, V_{N_3} and V_{N_4} are all 0 V. Consequently, logic gate U_1 outputs a low level, and COMP1 closes. Logic gate U_2 outputs a high level, and logic gate U_3 outputs a high level. Comparator COMP2 conducts and outputs −2 V. As V_{N_3} and V_{N_4} are both 0 V, COMP3 and COMP4 are closed. At this point, $V_2 = 0$ V, $V_2 = -2$ V, $V_3 = 0$ V, and $V_4 = 0$ V.

3. When only the electric bell (600 Hz) signal is input, neuron N_3 is activated, and the input voltage V_{N_3} is 3 V, while V_{N_1}, V_{N_2} and V_{N_4} are all 0 V. Logic gates U_1 and U_3 output a low level, and COMP1 and COMP2 close. COMP3 conducts and outputs −2 V, generating an inhibitory signal, while COMP4 closes. At this point, $V_1 = 0$ V, $V_2 = 0$ V, $V_3 = -2$ V and $V_4 = 0$ V.

4. When only the bell (400 Hz) signal is input, neuron N_4 is activated, and the input voltage V_{N_4} is 3 V, while V_{N_1}, V_{N_2}, and V_{N_3} are all 0 V. COMP1, COMP2, and COMP3 are

closed, and COMP4 conducts, outputting −2 V. At this point, the voltage values for V_1, V_2, V_3 and V_4 are 0 V, 0 V, −2 V, and −2 V, respectively.

5. When the food signal and the bell (600 Hz) signal are input simultaneously, neurons N_1 and N_2 are activated, resulting in $V_{N_1} = V_{N_2} = 3$ V and $V_{N_3} = V_{N_4} = 0$ V. Logic gate U_1 outputs a high level, COMP1 conducts and outputs 3 V, prompting associative learning and generating a learning signal, which is summed via an adder to V_3 and V_4. Logic gate U_3 outputs a low level, and COMP3 closes. Since $V_{N_3} = V_{N_4} = 0$ V, COMP4 and COMP5 also close. At this point, $V_1 = V_2 = V_3 = V_4 = 3$ V.

(3) Synapse module: The synapse module is shown in Fig. 8. The synapse is a critical component that connects input neurons and output neurons, and the magnitude of the synaptic weights determines the strength of the connections between neurons. V_1 represents the voltage generated by the input food signal, and V_2 represents the voltage generated after COMP1 is turned on. OP1 and OP2 are inverters. ABS1 and ABS2 are absolute value elements. Since the food and salivation response is innate, the food is considered an unconditioned stimulus. Therefore, the synaptic weight between the food and salivation response is set to a high value. In Fig. 8, the synaptic weight between the food and salivation response is represented by 1 kΩ. When a food signal is input, the output voltage of the inverter $V_{OP1} = -(1\text{ K}/1\text{ K}) \times 3\text{ V} = -3$ V. After passing through the absolute value component ABS1, the output voltage $V_{OUT1} = 3$ V. Based on Subsection 4.2, the bell (600 Hz, 400 Hz) and electric bell (600 Hz) are neutral stimuli, and the synapse weights between neurons N_2, N_3, N_4 and N_5 are low weight values and will change. Moreover, the memristor is an excellent device for simulating biological synapses. Therefore, memristors M_1, M_2, and M_3 represent the synapse weights between neurons N_2, N_3, N_4 and N_5, respectively. The initial resistance values of M_1, M_2, and M_3 are all set to 9999 Ω. When food and bell (600 Hz) signals occur simultaneously, associative learning occurs between the bell (600 Hz) and the food, resulting in the voltage value of V_2 becoming 3 V, causing the memristance value of memristor M_1 to decrease continuously. At this point, the output voltage of the inverter OP2 is $V_{OP2} = -(5\text{ K}/M_1) \times 3$ V. After passing through the absolute value element ABS2, $V_{ABS2} = -V_{OP2}$. The voltage value of V_{ABS2} increases as the memristance value of memristor M_1 decreases, which means that the synapse weight w_{25} between neurons N_2 and N_5 increases continuously. The connection between neurons N_2 and N_5 is continuously strengthened. When only Bell (600 Hz) signal is input, neuron N_2 is activated, the voltage value of V_2 becomes −2 V, the memristance value of memristor M_1 continuously increases, and the voltage value of V_{ABS2} decreases as the memristance value of M_1 increases. Subsequently, V_{ABS2} is input to the comparator COMP5, and its output voltage is represented by

$$V_{COMP5} = \begin{cases} 0\text{ V}, & 0 \le V_{ABS2} \le 2\text{ V}, \\ 5\text{ V}, & V_{IN2} > 2\text{ V}. \end{cases} \tag{9}$$

If the voltage value of V_{ABS2} is greater than 2 V, the comparator COMP5 is turned on and outputs 5 V, neuron N_5 is activated, and saliva secretion reaction occurs. If the voltage value of V_{ABS2} is less than 2 V, the comparator COMP5 is closed and outputs 0 V. The synapse modules between neurons N_2, N_3, N_4 and N_5 are the same, so they are not repeated.

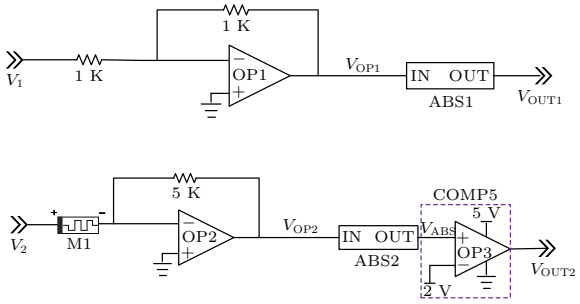


Fig. 8. Illustration of synaptic module circuits. The upper part shows the synaptic connection between neurons N_1 and N_5, and the lower part shows the synaptic connection between neurons N_2 and N_5.

4.3. Circuit simulation and validation

The associative memory circuit simulation experiments based on Ag/HfO$_x$/FeO$_x$/Pt memristors are conducted using PSPICE software. The voltage and resistance changes during the simulation experiment are shown in Table 3. V_{N_1}, V_{N_2}, V_{N_3}, V_{N_4}, and V_{N_5}, respectively, represent the output voltages of neurons N_1, N_2, N_3, N_4, and N_5, all generating 3 V pulses with a width of 0.5 s. M_1, M_2, and M_3 represent the resistance values of the corresponding memristors. A high-level output voltage V_{N_5} of 3 V indicates a salivation response, while a low-level output of 0 V indicates no response. The symbols "↑", "↓", and "\", respectively, represent an increase, decrease, and no change in the memristor resistance values.

(1) Test: The simulation results of the testing process are shown in Fig. 9. From 0 s to 5 s, when only the food signal is input, neuron N_1 is activated, generating the pulse voltage V_{N_1}, and output neuron N_5 is activated, resulting in a high level output voltage of 3V and a salivation response. From 5 s to 10 s, when only the bell (600 Hz) signal is input, neuron N_2 is activated, producing the pulse voltage V_{N_2}. At this point, output neuron N_5 is not activated, resulting in a low-level output voltage V_{N_5} of 0 V and no salivation response. From 10 s to 15 s, when only the electric bell (600 Hz) signal is input, neuron N_3 generates the pulse voltage V_{N_3}, and output neuron N_5 is not activated, leading to no salivation response. From 15 s to 20 s, when only the bell (400 Hz) signal is input, neuron N_4 is activated, producing a 3 V pulse voltage, and neuron N_5 is not activated, resulting in no salivation response. The resistance values of M_1, M_2, and M_3 remain unchanged.

Table 3. Input and output voltage values and resistance changes.

Experimental process	V_{N_1} (V)	V_{N_2} (V)	V_{N_3} (V)	V_{N_4} (V)	V_{N_5} (V)	M_1 (kΩ)	M_2 (kΩ)	M_3 (kΩ)
Test	3	0	0	0	3	\	\	\
	0	3	0	0	0	\	\	\
	0	0	3	3	0	\	\	\
	0	0	0	3	0	\	\	\
Learning	3	3	0	0	3	↓	↓	↓
Generation	0	3	0	0	3	↑	\	\
	0	0	3	0	3	\	↑	\
	0	0	0	3	3	\	↑	↑
Primary differentiation	3	3	0	0	3	↓	↓	↓
	0	0	3	0	3	\	↑	\
	3	3	0	0	3	↓	↓	↓
	0	0	3	0	3	\	↑	\
	0	3	0	0	3	↑	\	\
	0	0	3	0	0	\	↑	\
	0	0	0	3	3	\	↑	↑
Secondary differentiation	3	3	0	0	3	↓	↓	↓
	0	0	0	3	3	\	↑	↑
	3	3	0	0	3	↓	↓	↓
	0	0	0	3	3	\	↑	↑
	0	3	0	0	3	↑	\	\
	0	0	3	0	0	\	↑	\
	0	0	0	3	0	\	↑	↑
Forgetting	0	3	0	0	3	↑	\	\
	0	3	0	0	0	↑	\	\

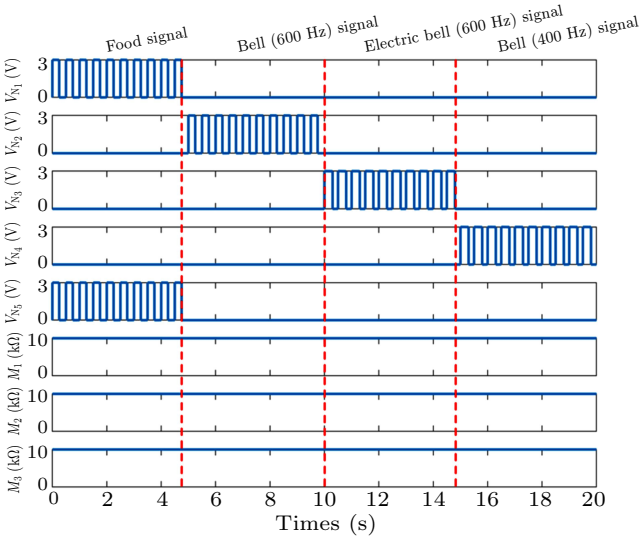


Fig. 9. Test process.

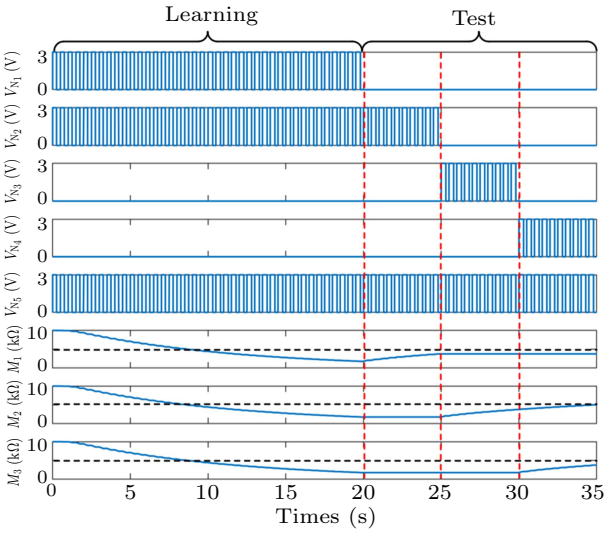


Fig. 10. Generalization process.

(2) Generalization: The generalization process is shown in Fig. 10. In 0 s–20 s, food stimulus and bell (600 Hz) stimulus are generated simultaneously, neurons N_1 and N_2 are activated simultaneously, generating pulse voltage V_{N_1} and V_{N_2}, and associative learning is performed. During the learning process, as the memristance values of M_1, M_2, and M_3 decrease, the synaptic weights w_{25}, w_{35}, and w_{45} increase, and the connections between neurons N_2, N_3, N_4, and N_5 are continuously strengthened. In the generalization test phase of the 20 s–35 s, when the bell (600 Hz), buzzer (600 Hz), and bell (400 Hz) stimuli are applied separately, neuron N_5 is activated, causing a salivation response.

(3) Primary differentiation: Primary differentiation is to distinguish the bells of different timbres based on generalization, that is, to distinguish the bell (600 Hz) from the buzzer (600 Hz), and the simulation process is shown in Fig. 11. In the first training cycle of 35 s–40 s, food stimulus and bell (600 Hz) stimulus are generated simultaneously, neurons N_1 and N_2 are activated simultaneously, M_1, M_2, and M_3 memristance values decrease, synaptic weights w_{25}, w_{35}, and w_{45} increase. In the 40 s–47 s, only a buzzer (600 Hz) stimulus is applied, neuron N_3 is activated, and as the memristance value of M_2 increases, the synaptic weight w_{35} decreases. After repeating the training for two cycles, the memristance value of

M_2 increases to more than 5 K. In the test phase of 65 s–80 s, when neurons N_2, N_3, and N_4 are activated separately, only when neuron N_3 is activated alone does neuron N_5 remain inactive, and no salivation response occurs. Therefore, the bell (600 Hz, 400 Hz) and the buzzer (400 Hz) are successfully distinguished.

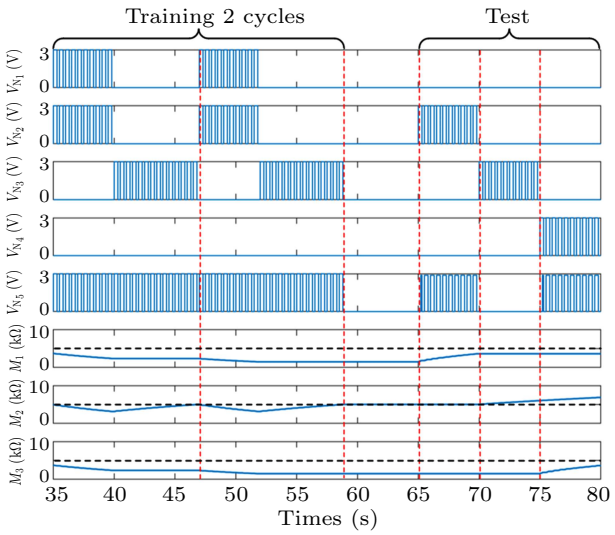


Fig. 11. Primary differentiation.

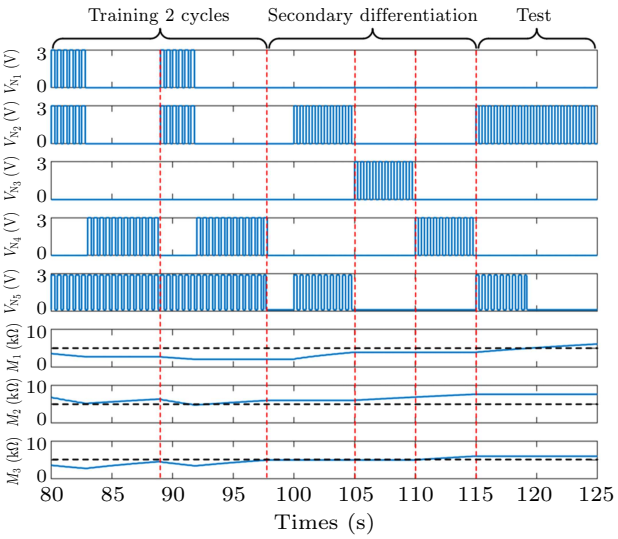


Fig. 12. Secondary differentiation and forgetting.

(4) Secondary differentiation and forgetting: The secondary differentiation further distinguishes between bells of the same timbre but different pitches, explicitly differentiating between the bell (600 Hz) and the bell (400 Hz). The process of secondary differentiation and forgetting is shown in Fig. 12. During the 80 s–98 s secondary differentiation training phase, from 80 s to 83 s, when both the food and the bell (600 Hz) signals are input, neurons N_1 and N_2 are simultaneously activated, and the resistance values of memristors M_1, M_2, and M_3 decrease. From 83 s to 89 s, when the bell (400 Hz) signal is input alone, neuron N_4 is activated, and the resistance value of memristor M_3 continues to decrease. After repeating the training several times, when the bell (400 Hz) signal is input alone, neuron N_5 is not activated, whereas when the bell (600 Hz) signal is input alone, neuron N_5 is still activated. At this point, the bells (600 Hz) and (400 Hz) are distinguished, and the process of secondary differentiation is completed. From 115 s to 125 s, forgetting is achieved based on the secondary differentiation. After applying the bell (600 Hz) stimulus alone several times, the resistance value of memristor M_2 increases to above 5 kΩ, and neuron N_5 is no longer activated, resulting in no salivation response.

4.4. Comparison with previous memristor-based Pavlov associative memory circuits

Table 4 compares different Pavlov associative memory circuits based on memristors, highlighting their individual drawbacks. The circuit structures presented in Refs. [29,30] are indeed simple, yet they are limited to achieving only the primary function of associative memory. In contrast, Refs. [28,31,32] have advanced to implement generalization and differentiation through learning and forgetting mechanisms, yet they fall short of achieving the function of secondary differentiation. While Ref. [33] does achieve secondary differentiation, it lacks physical support and boasts a complex circuit design. Building upon Ag/HfO_x/FeO_x/Pt memristors, the Pavlov associative memory circuit introduced in this paper stands out, offering comprehensive functionality including learning, forgetting, generalization, differentiation, and secondary differentiation. In comparison to existing works, the proposed circuit design is not only simpler but also boasts more extensive functionality, physical support, and a hardware-friendly implementation.

Table 4. Comparison with different memristor-based Pavlovian associative memory circuits.

Work	[29]	[30]	[28,31]	[32]	[33]	Ours
Physical support	×	√	×	√	×	√
Learning	√	√	√	√	√	√
Forgetting	×	√	√	√	√	√
Generalization	×	×	√	√	√	√
Primary differentiation	×	×	√	√	√	√
Secondary differentiation	×	×	×	×	√	√
Circuit complexity	easy	easy	medium	medium	complex	medium

5. Conclusion

This study proposes a memristor model exhibiting RS memory behavior. The Ag/HfO_x/FeO_x/Pt memristor is meticulously fabricated utilizing DC and AC sputtering methods, and a thorough analysis of its physical mechanism is conducted. Subsequently, a corresponding physical memristor model is constructed, grounded in the F-P tunneling physical mechanism, which accurately reflects the physical characteristics of the device and is validated through rigorous simulation experiments. Leveraging this Ag/HfO_x/FeO_x/Pt memristor, a Pavlov associative memory circuit is designed, boasting low power consumption, high on/off ratio, superior response ratio,

and exceptional synaptic plasticity. This circuit enables generalization, primary differentiation, secondary differentiation, and forgetting functions, all of which are verified, simulated, and analyzed using PSPICE software. This circuit represents a significant extension of the primary Pavlov associative memory circuit, characterized by its simplicity and remarkable ability to mimic the memory and forgetting behaviors of the human brain. Ultimately, this work contributes to the advancement of biologically inspired computing systems.

Acknowledgements

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