

M^2CS: A microwave measurement and control system for large-scale superconducting quantum processors

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M^2CS: A microwave measurement and control system for large-scale superconducting quantum processors

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As superconducting quantum computing continues to advance at an unprecedented pace, there is a compelling demand for the innovation of specialized electronic instruments that act as crucial conduits between quantum processors and host computers. Here, we introduce a microwave measurement and control system (M^2CS) dedicated to large-scale superconducting quantum processors. M^2CS features a compact modular design that balances overall performance, scalability and flexibility. Electronic tests of M^2CS show key metrics comparable to commercial instruments. Benchmark tests on transmon superconducting qubits further show qubit coherence and gate fidelities comparable to state-of-the-art results, confirming M^2CS's capability to meet the stringent requirements of quantum experiments running on intermediate-scale quantum processors. The compact and scalable nature of our design holds the potential to support over 1000 qubits after upgrade in stability and integration. The M^2CS architecture may also be adopted to a wider range of scenarios, including other quantum computing platforms such as trapped ions and silicon quantum dots, as well as more traditional applications like microwave kinetic inductance detectors and phased array radar systems.

Keywords: superconducting quantum computation, superconducting qubit, arbitrary waveform generator (AWG), data acquisition board (DAQ)

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1. Introduction

Quantum computing holds the potential to solve some hard problems that are otherwise intractable with classical computers, such as large number factorization.[1,2] Superconducting qubits, one of the most promising platforms for large-scale, fault-tolerant quantum computers, have made tremendous progresses in recent years.[3–5] Both the quality and quantity of qubits in superconducting quantum processors have been rapidly improved,[6–10] breaking through the 1000 qubits barrier on a single superconducting quantum chip recently.[11] Concurrently, to achieve logical qubits and, ultimately, fault-tolerant quantum computing, some progress has been made in qubit error correction.[12–16] Such rapid progress poses new challenges for electronic instruments used to control and measure superconducting quantum processors.

Electronic instruments are crucial for precise control of superconducting qubits and high-fidelity measurement of their states. Taking the widely used transmon superconducting qubits as an example,[17,18] electronic instruments must be able to perform the following functions at a minimum:[19,20] (1) output high-precision intermediate-frequency (IF) signals for qubit Z bias and adjust couplers between qubits; (2) output radio-frequency (RF) microwave signals (typically within the C band frequency range of 4–8 GHz) finely tuned for qubit XY operation and state detection; (3) sample RF microwave signals returned from the quantum processor, demodulate the signals to discriminate the qubit states.

Driven by increasing demand in this field, commercial products have been developed to fulfill these requirements, however, their closed-source hardware and digital logic hinder custom optimization, and their high cost limits affordability. Laboratory-based electronic instruments have also been developed, some of which utilize a combination of customized RF hardware and commercial high-performance field programmable gate array (FPGA) evaluation boards with their FPGA logic being open-sourced.[21–24] Others employ entirely customized FPGA-based hardware to enhance scalability further.[25–30]

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Here, we introduce an FPGA-based electronic instrument dedicated to large-scale superconducting quantum processors, which we call the microwave measurement and control system (M^2CS). The M^2CS adopts a modular architecture for scalability and flexibility, where the hardware is housed within a 6U compactPCI chassis. Each chassis comprises one backplane and 14 slots which can accommodate arbitrary waveform generator (AWG) and data acquisition (DAQ) modules. Each AWG module features four digital-to-analog (DAC) channels that can generate IF pulses with a sampling rate of 2 Gsps and a vertical resolution of 14 bits. To generate RF microwave pulses for qubit *XY* control and state detection, some AWG modules are equipped with two surface-mounted in-phase and quadrature (IQ) mixers that up-convert the IF pulses to RF pulses in the GHz range. To avoid confusion, we call the AWG modules with or without IQ mixers RF-AWG or IF-AWG modules, respectively, and refer to AWG when discussing features they share in common. The DAQ modules are essentially the dual of RF-AWG modules. Each DAQ module offers two RF input channels, which are down-converted to IF signals by the on-board IQ mixers, then digitized by analog-to-digital converters (ADCs) with a sampling rate of 1 Gsps and a resolution of 8 bits.

To meet expanded system requirements, multiple chassises can be cascaded in a tree-like structure, forming a scalable system with one master chassis connected to a maximum of 11 first-level slave chassis, and more than a hundred second-level slave chassises. The system's stability and efficiency are bolstered by a unified clock network, a 2-level trigger chain, and 1 Gbps UDP ethernet communication, all integrated on the system backplane. Electronics tests of M^2CS show key metrics comparable to commercial instruments. The IF-AWG output has a spurious-free dynamic range (SFDR) of < -50 dBc over the entire bandwidth of 500 MHz, and a phase noise floor of -140 dBc/Hz beyond 10 kHz frequency offset. The IQ mixers on the RF-AWG modules can be carefully calibrated to suppress the carrier and image sideband leakage to below -80 dBm.

Table 1. Overview of key metrics of M^2CS.

Module	Performance	Value	Unit
IF-AWG	sampling rate	2	Gsps
	resolution	14	Bits
	bandwidth	DC-500	MHz
	phase noise floor	-140	dBc/Hz
	SFDR	< -50	dBc
	max waveform length	200	μs
RF-AWG	leakage suppression	< -80	dBm
	frequency range	4–8	GHz
DAQ	sampling rate	1	Gsps
	resolution	8	Bits
	demodulation	12	channels
Backplane	slot number	14	slots
	ethernet speed	1	Gb/s
	feedback loop latency	180	ns

The DAQ module supports fast on-board demodulation of 12 channels with a feedback loop latency as low as 180 ns, enabling fast mid-circuit quantum measurement and error correction. An overview of key metrics is listed in Table 1 for M^2CS. Finally, we benchmark the M^2CS performance with superconducting transmon qubits, showing 128.7 μs qubit lifetime and 99.73% CZ gate fidelity, comparable to state-of-the-art results. This confirms M^2CS's capability to meet the stringent requirements of quantum experiments running on intermediate-scale superconducting quantum processors.

2. System architecture

The system architecture of M^2CS, depicted in Fig. 1, comprises four principal parts: a unified clock network, a two-level trigger chain, a low-latency feedback loop and a 1 Gbps UDP ethernet communication network. These parts are primarily constituted by FPGA internal logic located on the backplane and the modules, supplemented by auxiliary components such as clock and communication chips.

The unified clock network distributes 10 MHz reference clock sourced from a rubidium atomic clock. All FPGAs internally multiply the 10 MHz clock to 250 MHz, serving as the primary operating frequency. The 2 GHz and 1 GHz sampling clocks required for the AWG and DAQ modules are distributed from the backplane using a clock generation device HMC7044 from Analog Devices Inc.,[31] ensuring precise clock alignment across modules. Additionally, the HMC7044 provides a unified 500 MHz synchronous clock to the digital-to-analog (DAC) chips on the AWG modules, facilitating synchronization of all output channels without manual calibration.

To flexibly control the synchronization of signal generation and acquisition in M^2CS, we adopt a two-level trigger chain architecture. The level 1 trigger is used to align the zero-time points of all chassises. When a user command is received from the host computer, a software start trigger is sent to the master chassis, which subsequently distributes level 1 trigger signals to all slave chassises. This action initiates simultaneous operation of all backplanes within the system. Subsequently, the backplanes transmit level 2 triggers to different modules based on user-defined timestamps, allowing users to control the start time of each module with flexibility.

In the low-latency feedback loop, the FPGA on the DAQ module discriminates the qubit states based on the phase of the demodulated signals. These state discrimination results are transmitted back to the backplane encoded in low-voltage differential signaling (LVDS) format via physically independent category 8 ethernet cables. The FPGA on the backplane, based on these results, sends level 2 branch triggers to the AWG modules at the user-defined timestamps. The FPGA on the AWG module selects the corresponding branch waveform data for output based on the branch triggers and a playlist uploaded in advance.

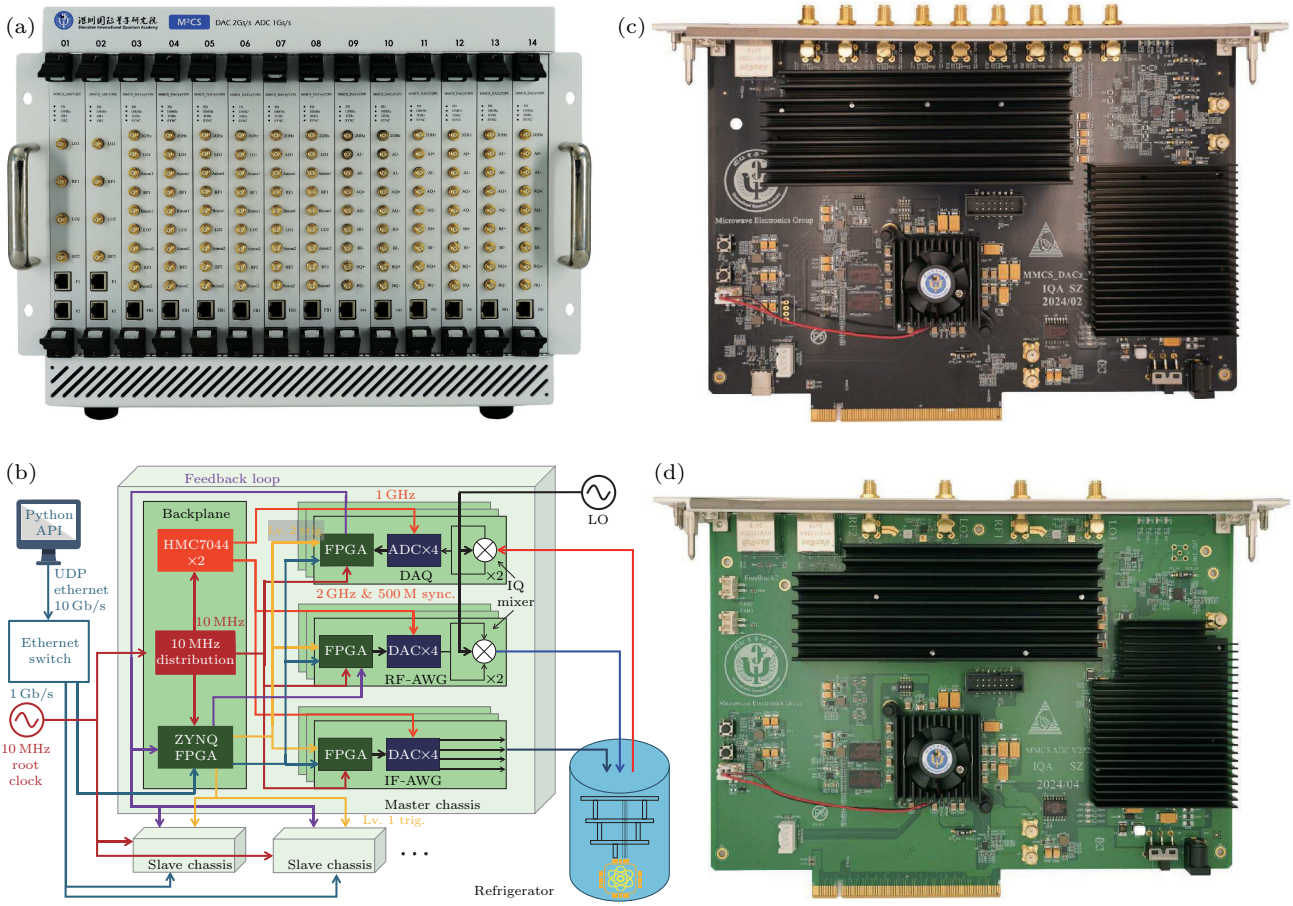


Fig. 1. System architecture of M^{2}CS. (a) Photograph of a M^{2}CS chassis. (b) Schematic of the system architecture. (c) and (d) Photographs of AWG and DAQ modules, respectively.

During the communication with host computers, M^{2}CS is tasked with uploading waveform data to AWG modules and downloading sampled data along with demodulation outcomes from DAQ modules. The total data volume can reach magnitudes of MB or even GB per experiment cycle. Given the impact of communication bandwidth on experiment efficiency, the chassises are connected to the host computer through a commercial ethernet switch operating at 10 Gb/s, and data is distributed with a 1 Gb/s UDP ethernet protocol within each chassis supported by the ZYNQ FPGA[32] on the backplane, where UDP datagrams are unpacked and distributed either to the designated module or the backplane itself based on the datagram's content.

Diverging from standard compactPCI chassis backplanes, the M^{2}CS backplane not only provides standard functionalities such as power supply and wiring but also offers highly integrated features, including dynamic clock networks, communication switching, and custom triggers, as depicted in Fig. 2(a). The main control FPGA utilizes Xilinx's ZYNQ-7045 chip.[32] On its processing system (PS) side, it accommodates Dual-core ARM Cortex-A9 processors running clock management software. Upon detecting the insertion of AWG or DAQ modules, the ZYNQ controls the HMC7044 clock chip[31] to provide 2 GHz or 1 GHz clock for the module, respectively. On the programmable logic (PL) side, hardware logic circuits are employed to perform unpacking, packing, and forwarding of 1 Gbps UDP datagram. The low-latency nature of hardware logic ensures forwarding delays of only a few tens of nanoseconds.

In the level 2 trigger RAM, users can store custom 36-bit trigger instructions. This instruction set consists of lower 4 bits representing trigger types (start, stop, or branch requests for AWG modules to select branch waveforms) and upper 32 bits denoting timestamps. When the system timer matches the timestamp value, the control finite state machine (FSM) executes the instruction. For start/stop/branch trigger types, the FSM directly transmits the lower 4 bits of the instruction. For feedback trigger types, the FSM adjusts the output to branch 0 or 1 trigger based on feedback from the DAQ.

The AWG modules in our system are equipped with AD9739 DAC chips with a sampling rate of 2 Gsps and a resolution of 14 bits.[33] Xilinx's Kintex-7 FPGA[34] is utilized as the main control FPGA, allowing each channel to store waveform data up to 400 k, with a maximum 200 μs waveform for each channel. We employ the LVDS communication format between the AD9739 and FPGA to minimize the transmission delays.

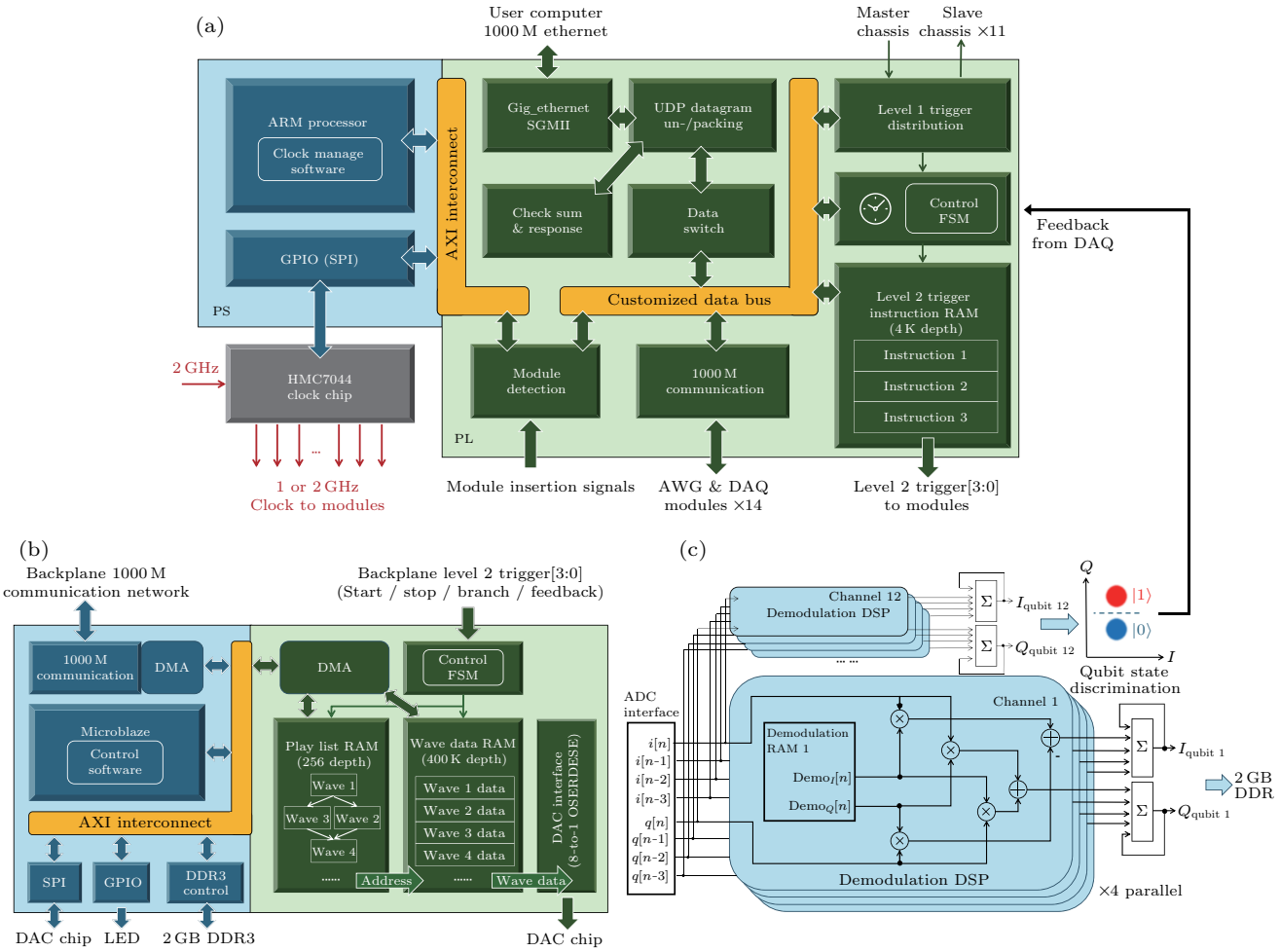


Fig. 2. Block diagram of the backplane, the AWG and the DAQ modules. (a) Schematic of backplane FPGA logic. The blue part is the processing system (PS) side of ZYNQ, which includes an ARM processor. The processor is responsible for running clock management software and dynamically controlling the clock chip output at 1 GHz or 2 GHz depending on the DAQ or AWG module detected. The green part is the programmable logic (PL) side of ZYNQ, which contains FPGA hardware resources. The FPGA is responsible for communication, triggering and feedback functions. The level 1 trigger resets the timer inside the FSM, and when the timer value equals the timestamp in instructions, the level 2 trigger is sent to the DAQ and AWG modules. (b) Schematic of AWG FPGA logic. The blue parts are responsible for data communication and register configuration before and after the experiment. The green parts are responsible for waveform generation during the experiment. (c) Schematic of DAQ DSP for real-time demodulation and qubit state discrimination.

As illustrated in Fig. 2(b), we utilize Xilinx's MicroBlaze soft-core processor within the FPGA to execute control software written in C language. This software manages pre- and post-experiment data processing as well as parameter configurations. Upon receiving waveform data from the backplane, it is temporarily stored in the 2 GB DDR memory via the AXI bus before being efficiently transferred to each channel's RAM using the MicroBlaze-controlled DMA (direct memory access) module.

During experiments, main control of the AWG is transferred to the control FSM. Trigger signals received from the backplane prompt the FSM to access the play list RAM, retrieving the storage address of the next waveform data. Subsequently, waveform data is fetched from the wave data RAM based on this address and then promptly dispatched to the AD9739 via the interface module. To support branching functions, the play list RAM accommodates waveform data storage structures with branches. This readout link has been finely optimized, with an internal FPGA delay of only 32 ns (8 clock cycles) from receiving the trigger to transmitting the waveform.

Each DAQ module features two dual-channel, 1 Gsps, 8-bit ADC08D1020 chips.[35] It also uses the Xilinx Kintex-7 FPGA as its primary control FPGA. Each dual-channel ADC chip connects to an IQ mixer to down-convert the RF input to IF signals for subsequent sampling and processing. For low-latency demodulation of qubit readout signal, a digital signal processing (DSP) module has been designed within the DAQ FPGA, as depicted in Fig. 2(c). Each RF input is down-converted to two IF signals first, which are subsequently digitized to two sequences of data $i[n]$ and $q[n]$, respectively, where n is the index of the data. To obtain the qubit-state-imparted phase information, the data array is demodulated into a data point (I, Q) in the phase space by the DSP in the following way:

$$I = \sum_n i[n] \times \text{demod}_I[n] - q[n] \times \text{demod}_Q[n],$$

$$Q = \sum_n i[n] \times \mathrm{demod}_Q[n] + q[n] \times \mathrm{demod}_I[n], \quad (1)$$

where $\mathrm{demod}_I[n]$ and $\mathrm{demod}_Q[n]$ are user-defined demodulation factors, typically taking the form of

$$\begin{aligned} \mathrm{demod}_I[n] &= \cos(-\omega_{\mathrm{demod}} \times n\Delta t + \phi_{\mathrm{demod}}), \\ \mathrm{demod}_Q[n] &= \sin(-\omega_{\mathrm{demod}} \times n\Delta t + \phi_{\mathrm{demod}}), \end{aligned} \quad (2)$$

where $\omega_{\mathrm{demod}}/2\pi$ is the demodulation frequency, $\Delta t = 1$ ns is the time step determined by the DAQ sampling rate, and ϕ_{demod} is the demodulation phase. One can also incorporate an envelope such as Hann window into the demodulation factor to optimize the demodulation performance.

Up to 12 channels of user-defined demodulation factors are supported for multiplexed readout of superconducting qubits coupled to the same readout line.

The DAQ module also supports multiple-time readouts with up to 8 μs sample length. The module includes 2 GB of DDR memory, providing storage for 60000 sets of demodulation results and over 10 ms of raw data storage per readout line. To implement fast feedback control protocols, the DSP module compares the IQ demodulation data with the user-defined state discrimination thresholds to discriminate the superconducting qubit's state, which is subsequently transmitted to the backplane through the low-latency feedback loop.

3. Electronics performance

The spurious-free dynamic range (SFDR) is a critical specification for evaluating the quality of IF-AWG output spectrum. SFDR quantifies the power distinction between the generated signal and the highest spurious signal, typically the harmonics. We connect an IF-AWG module to a Rohde & Schwarz FSL18 spectrum analyzer to measure its spectrum across the 10–2000 MHz range, see Fig. 3(a) for example, where a SFDR of −69.4 dBc is measured for a 100 MHz sinusoidal wave generated by the IF-AWG. The SFDR measurements at different IF-AWG output frequencies are shown as inset to Fig. 3(a), which are below −50 dBc over the entire bandwidth of 500 MHz. A Rohde & Schwarz FSWP26 phase noise analyzer is used to conduct the phase noise tests. We benchmark the phase noise performance of sinusoidal waves generated by the IF-AWG at different frequencies from 50 MHz to 500 MHz, as depicted in Fig. 3(b). The results indicate a phase noise floor of about −140 dBc/Hz beyond 10 kHz frequency offset. Integrating the phase noise in Fig. 3(b) from 1 Hz to 30 MHz yields a root mean square (RMS) phase jitter of 1 ps for the IF-AWG output.

Frequency tunable superconducting qubits require precise direct current (DC) sources to adjust their operating frequencies, as well as fast Z pulses to dynamically tune the qubit frequencies for gate operations. As the number of qubits rapidly increases, it is highly desirable to reduce the wiring channels and use IF-AWGs to provide both the DC bias and fast Z pulses. This requires proper wiring inside the dilution fridge, and that the IF-AWG output voltage is sufficiently stable to avoid qubit frequency drift. The IF-AWG outputs are buffered by low noise, large-bandwidth differential amplifiers to convert the DAC differential outputs to single-ended outputs with a DC voltage swing of −1 V to 1 V, yielding a least significant bit (LSB) resolution of 122 μV. The differential amplifiers are powered by two stages of low-dropout regulators to reject ripples from the power supply. As a benchmark test, we set the IF-AWG output to 0 V and 200 mV respectively, and monitor its long term stability (8 hours) using a KEITHLEY DMM6500 $6\frac{1}{2}$ digital multimeter, showing a peak-to-peak fluctuation of 31 $\mu V_{p\text{-}p}$ and 121 $\mu V_{p\text{-}p}$ respectively, see Fig. 3(c). With a typical wiring attenuation of 30 dB and a mutual inductance coupling of 2 pH to the qubit junction loops, this voltage fluctuation corresponds to a flux shift of the order of 1 $\mu\Phi_0$ and the qubit frequency shift of the order of 1 MHz, a tolerable value given the time span of 8 hours. While the slow drift of the DC voltage only affects the operating frequencies of the qubits, the low frequency noise at the audio band can affect the phase coherence of frequency tunable qubits. We measure the low frequency noise spectrum of the IF-AWG with a Rohde & Schwarz upv audio analyzer, as shown in Fig. 3(d), where the spectrum reaches a noise floor of 20 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 10 kHz. It is worth mentioning that the noise floor of the audio analyzer is 10 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, as confirmed by a 50 Ω load.

To generate RF microwave pulses for qubit XY control and state detection, RF-AWG modules are quipped with two surface-mounted IQ mixers. IQ mixers can up-convert IF pulses that are relatively easy to handle with electronic devices to RF microwave pulses, or inversely down-convert RF signals to IF signals for subsequent processing. They have been commonly used in point-to-point communication, test and measurement applications and so on. An IQ mixer consists of four ports: the LO port which is driven by a local oscillator with a continuous drive of $\cos(\omega_{\mathrm{LO}}t)$, two IF ports for in-phase (I port) and quadrature (Q port) modulation of the LO drive, and the RF port whose output is ideally given by $\mathrm{RF}(t) = I(t)\cos(\omega_{\mathrm{LO}}t) + Q(t)\sin(\omega_{\mathrm{LO}}t)$. By modulating the I and Q ports at a sideband frequency as $I(t) = \cos(\omega_{\mathrm{sb}}t)$, $Q(t) = -\sin(\omega_{\mathrm{sb}}t)$, one can obtain a frequency up-conversion at the RF port: $\mathrm{RF}(t) = \cos(\omega_{\mathrm{sb}}t)\cos(\omega_{\mathrm{LO}}t) - \sin(\omega_{\mathrm{sb}}t)\sin(\omega_{\mathrm{LO}}t) = \cos[(\omega_{\mathrm{LO}} + \omega_{\mathrm{sb}})t]$. However, as nonlinear analog devices, nonidealities such as offset and amplitude/phase imbalance in the I and Q ports lead to signal leakage at the LO frequency or the image sideband frequency (i.e., $\omega_{\mathrm{LO}} - \omega_{\mathrm{sb}}$), which could detrimentally affect the qubit coherence and quantum gate fidelity. Techniques that eliminate LO and image sideband leakages have been well-established at

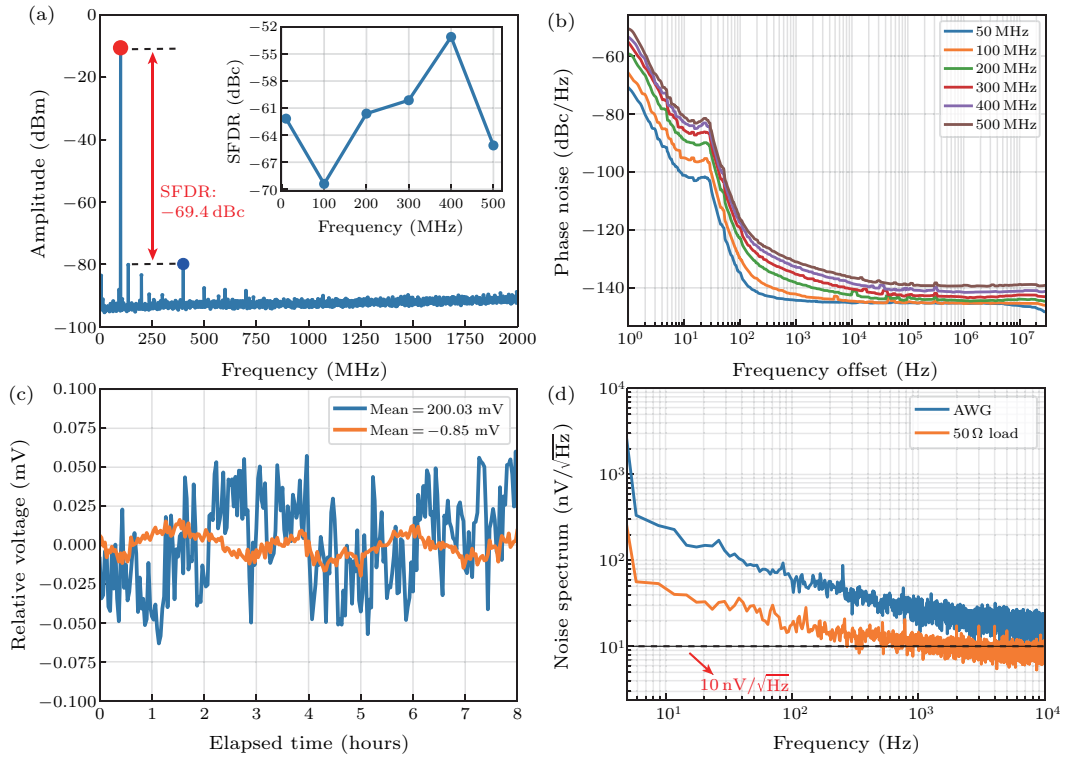


Fig. 3. IF-AWG module benchmark. (a) AWG output spectrum, where a SFDR of −69.4 dBc is measured for a 100 MHz sinusoidal wave generated by the AWG. Inset: SFDR over the entire bandwidth of 500 MHz. (b) Phase noise measurement for different sinusoidal wave frequencies, reaching a phase noise floor of about −140 dBc/Hz at 10 kHz offset. (c) Voltage drift over 8 hours where the AWG output is set to 0 V (200 mV), showing an average voltage of −0.85 mV (200.03 mV) and a peak-to-peak fluctuation of 31 $\mu V_{p\text{-}p}$ (121 $\mu V_{p\text{-}p}$). Each data point is averaged over 1 minute. (d) Low frequency noise spectrum of the AWG output, reaching a noise floor of 20 nV/$\sqrt{\text{Hz}}$. Note the instrument noise floor is about 10 nV/$\sqrt{\text{Hz}}$, as confirmed by a 50 Ω load.

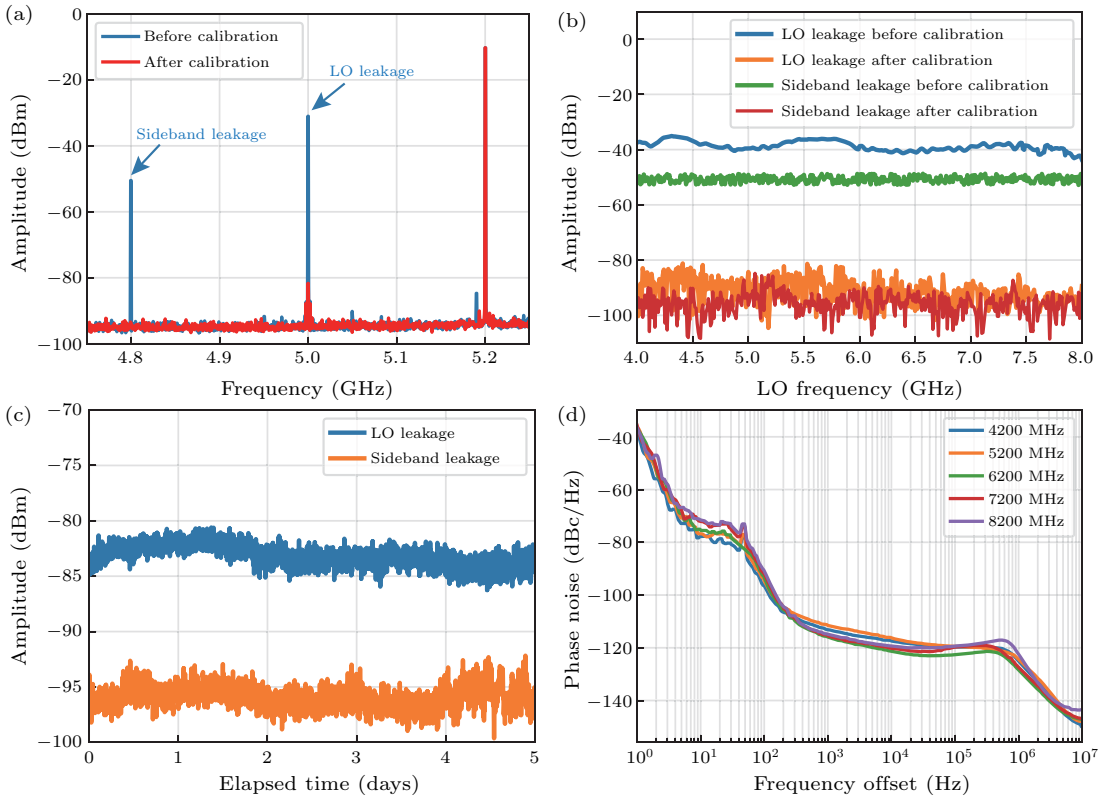


Fig. 4. RF-AWG module benchmark. (a) RF-AWG output spectrum before and after calibration, where the LO frequency $\omega_{LO}/2\pi =$ 5 GHz, and the sideband frequency $\omega_{sb}/2\pi = 200$ MHz. The LO leakage is suppressed from ~ -30 dBm to < -80 dBm, whereas the image sideband leakage is suppressed from ~ -50 dBm to < -90 dBm. (b) The LO and sideband leakage calibration at various $\omega_{LO}/2\pi$ from 4 GHz to 8 GHz, with $\omega_{sb}/2\pi$ fixed at 200 MHz. (c) Long term stability of the mixer calibration. (d) Phase noise of the RF-AWG output, where $\omega_{LO}/2\pi$ is changed from 4 GHz to 8 GHz at a step of 1 GHz, and $\omega_{sb}/2\pi$ is fixed at 200 MHz.

room temperature utilizing spectrum analyzers or additional instruments for output diagnosis.[36,37] In Fig. 4(a), we show the RF-AWG output spectrum before and after applying such calibration techniques, where the LO frequency is 5 GHz, and the sideband frequency is 200 MHz. The LO leakage at 5 GHz is suppressed from ~ -30 dBm to < -80 dBm, whereas the image sideband leakage is suppressed from ~ -50 dBm to < -90 dBm. Figure 4(b) shows the LO and sideband leakage calibration at various LO frequencies from 4 GHz to 8 GHz, with the sideband frequency fixed at 200 MHz. Both the LO and image sideband leakages are suppressed < -80 dBm after the calibration over the entire C band. One critical question arises as to how stable the calibration is. In Fig. 4(c), we test the long term stability of the calibration and find the LO and image sideband leakages being quite stable over 5 days. Utilizing high speed DAC chips, one can also synthesize RF microwave pulses directly without the need for mixer calibration, but these cutting-edge devices usually have worse phase noise (typically around -90 dBc at 1 kHz offset) and complex synchronization. The frequency mixing scheme we adopt here is relatively simple in system architecture because of low digital clock frequency and shows better phase noise performance. Figure 4(d) shows the phase noise of the RF-AWG output, where the LO frequencies are changed from 4 GHz to 8 GHz at a step of 1 GHz, the sideband frequency is fixed at 200 MHz, with a phase noise < -110 dBc at 1 kHz offset. This is a 20 dB improvement in terms of phase noise compared to direct synthesis schemes. Limited by efficiency and resource, such calibration method is cumbersome for large-scale quantum processors, requiring hundreds or even thousands of channels. To address this challenge, an *in situ* calibration method of mixers with superconducting qubits has been demonstrated.[38]

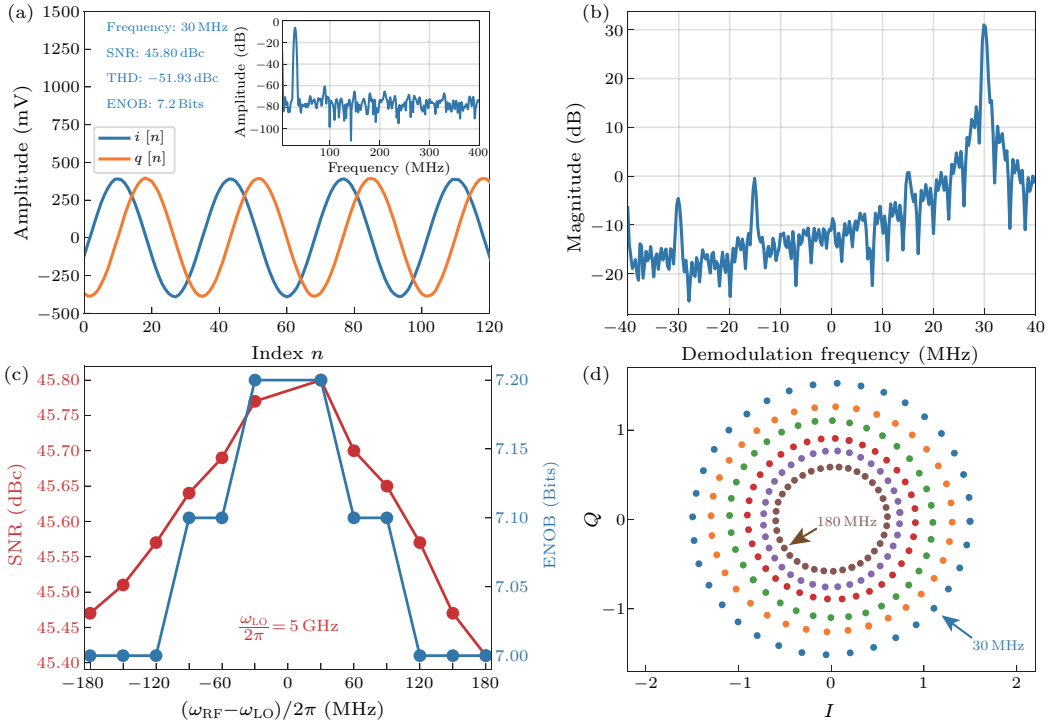


Fig. 5. DAQ module benchmark. (a) Detecting an RF signal with frequency $\omega_{\rm RF}/2\pi = 5.03$ GHz. Setting the LO frequency of the DAQ to 5 GHz, the RF signal is down-converted to 30 MHz and then digitized, where the in-phase sequence $i[n]$ and quadrature sequence $q[n]$ differ by 90 degrees, as expected. Inset: FFT analysis of the $i[n]$ sequence, from which we obtain the SNR, THD and ENOB parameters. (b) Fast demodulation of the sequence in (a) implemented on the FPGA. The demodulation frequency $\omega_{\rm demod}/2\pi$ is artificially varied here to demonstrate its frequency selectivity. A clear peak is observed in the demodulated signal magnitude when $\omega_{\rm demod}/2\pi = 30$ MHz. (c) SNR and ENOB of the DAQ for input RF signals of various frequencies $\omega_{\rm RF}/2\pi$ from $(5-0.18)$ GHz to $(5+0.18)$ GHz, with $\omega_{\rm LO}/2\pi$ set to 5 GHz. (d) Multiplexed demodulation. The input signal consists of a composite of various sideband frequency waves, ranging from 30 MHz to 180 MHz, with increments of 30 MHz. The input signal is digitized and simultaneously demodulated with $\omega_{\rm demod}/2\pi$ matching the sideband frequencies, while $\phi_{\rm demod}$ is varied at a step of 30 degrees. The demodulated data (I, Q) for each $\omega_{\rm demod}/2\pi$ are concentric around the origin in the phase space.

To test the functionality of the DAQ module, we drive the LO port of the mixers on the DAQ module at 5 GHz, and directly apply a continuous microwave signal to the RF input port. As adjacent readout resonators are typically separated in frequency by ~ 30 MHz or more,[3] we apply a 5.03 GHz microwave signal to the RF input and digitize the down-converted IF signals to two sequences of data $i[n]$ and $q[n]$, as shown in Fig. 5(a). Fast Fourier transform (FFT) analysis of the $i[n]$ sequence is shown in inset of Fig. 5(a), from which we obtain a signal-to-noise ratio (SNR) of 45.80 dBc, a total harmonic distortion (THD) of -51.93 dBc, and 7.2 effective number of bits (ENOB). The FPGA on the DAQ module supports fast on-board demodulation of up to 12 channels, where the demodulation factor of each channel is user-

defined. In Fig. 5(b), we show the fast on-board demodulation of the signal in Fig. 5(a), where the horizontal axis is the user-defined demodulation frequency $\omega_{\text{demod}}/2\pi$ artificially varied to demonstrate its frequency selectivity. A clear peak is observed in the demodulated signal magnitude when $\omega_{\text{demod}}/2\pi = 30$ MHz, with more than 30 dBc contrast over spurious peaks. We further vary the RF input frequency $\omega_{\text{RF}}/2\pi$ from $(5-0.18)$ GHz to $(5+0.18)$ GHz, and analyze the SNR and ENOB of the DAQ, as shown in Fig. 5(c), with >45 dBc SNR and >7 ENOB over the entire frequency range. To verify the frequency multiplexing and phase coherence, we apply input waveforms comprising the superposition of sinusoidal waves at 6 different sideband frequencies from 30 MHz to 180 MHz with decreasing amplitudes. The input signal is digitized and simultaneously demodulated with demodulation frequencies $\omega_{\text{demod}}/2\pi$ matching the sideband frequencies, while the demodulation phase ϕ_{demod} is varied at a step of 30 degrees, see Fig. 5(d). The demodulated data for the same $\omega_{\text{demod}}/2\pi$ are concentric around the origin in the phase space.

Synchronization consistency across multiple channels is extremely important, especially in large-scale systems.[27] To achieve synchronization across multiple AWG channels, we utilize an external 500 MHz synchronization clock network, as recommended in the AD9739 datasheet. The HMC7044 clock device is employed to generate both the 2 GHz sampling clock for the DAC chips and the 500 MHz synchronization clock, which is derived from a stable 10 MHz rubidium atomic clock. To ensure precise phase alignment, the PCB trace lengths for clock channels are carefully designed to match propagation delays across all components. This meticulous hardware design ensures synchronization across different AWG channels, eliminating the need for manual calibration. Additionally, we have implemented a careful power-on sequencing protocol to ensure consistent and reliable system timing performance during power cycling. Complementing our hardware synchronization, we have implemented software control through the FPGA logic. The FPGA IO pins provide programmable delays with 32 steps of 78 ps, enabling precise control over clock and trigger timing. This feature is especially beneficial for synchronizing the DAQ modules with the AWG modules, ensuring that the system operates seamlessly. We have conducted rigorous experimental tests to measure the time jitter between AWG channels, which have consistently shown results below 10 ps, as illustrated in Figs. 6(a) and 6(b), well within the required tolerance for qubit operations. We notice that the synchronization between DAQ and AWG modules could occasionally enter a metastable region. We evaluate the system's metastability by analyzing the variance in demodulation results, as shown in Figs. 6(c) and 6(d). The results reveal a metastable region of approximately 500 ps. By adjusting the FPGA IO delays, we can effectively avoid metastability, significantly enhancing the system stability.

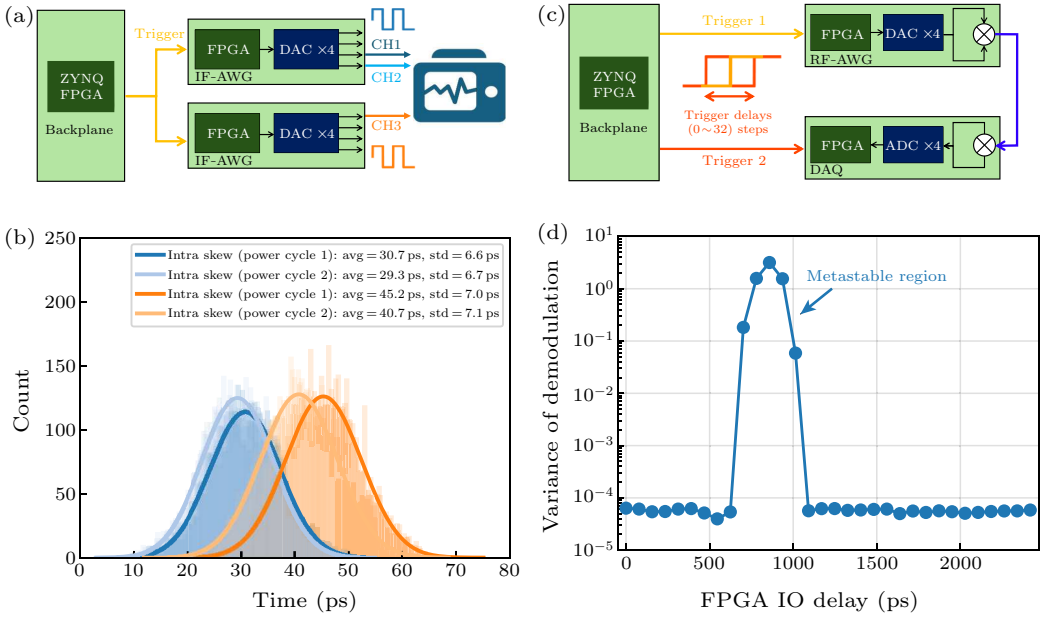


Fig. 6. Synchronization consistency between channels. (a) Jitter measurement setup: two IF-AWG modules generate 10 MHz square wave signals, output through CH1, CH2, and CH3 to an oscilloscope. Intra-board jitter is measured between CH1 and CH2, while inter-board jitter is measured between CH1 and CH3. (b) Jitter measurement results: the *x*-axis shows the edge-to-edge values between oscilloscope channels, while the *y*-axis represents skew occurrences. The results compare two power cycle measurements, showing intra-board (CH1 vs. CH2) and inter-board (CH1 vs. CH3) jitter. System skew remains below 10 ps and stable across power cycles. (c) Metastability measurement setup: the RF-AWG directly connects to the DAQ, capturing a fixed-phase single-tone signal. Metastability is assessed by varying the trigger delay in 78 ps steps, up to 32 steps, and analyzing the variance in DAQ demodulation results. (d) Metastability results: the variance of demodulation versus FPGA IO delays, revealing a metastable region around 500 ps, which can be avoided by adjusting the trigger delay.

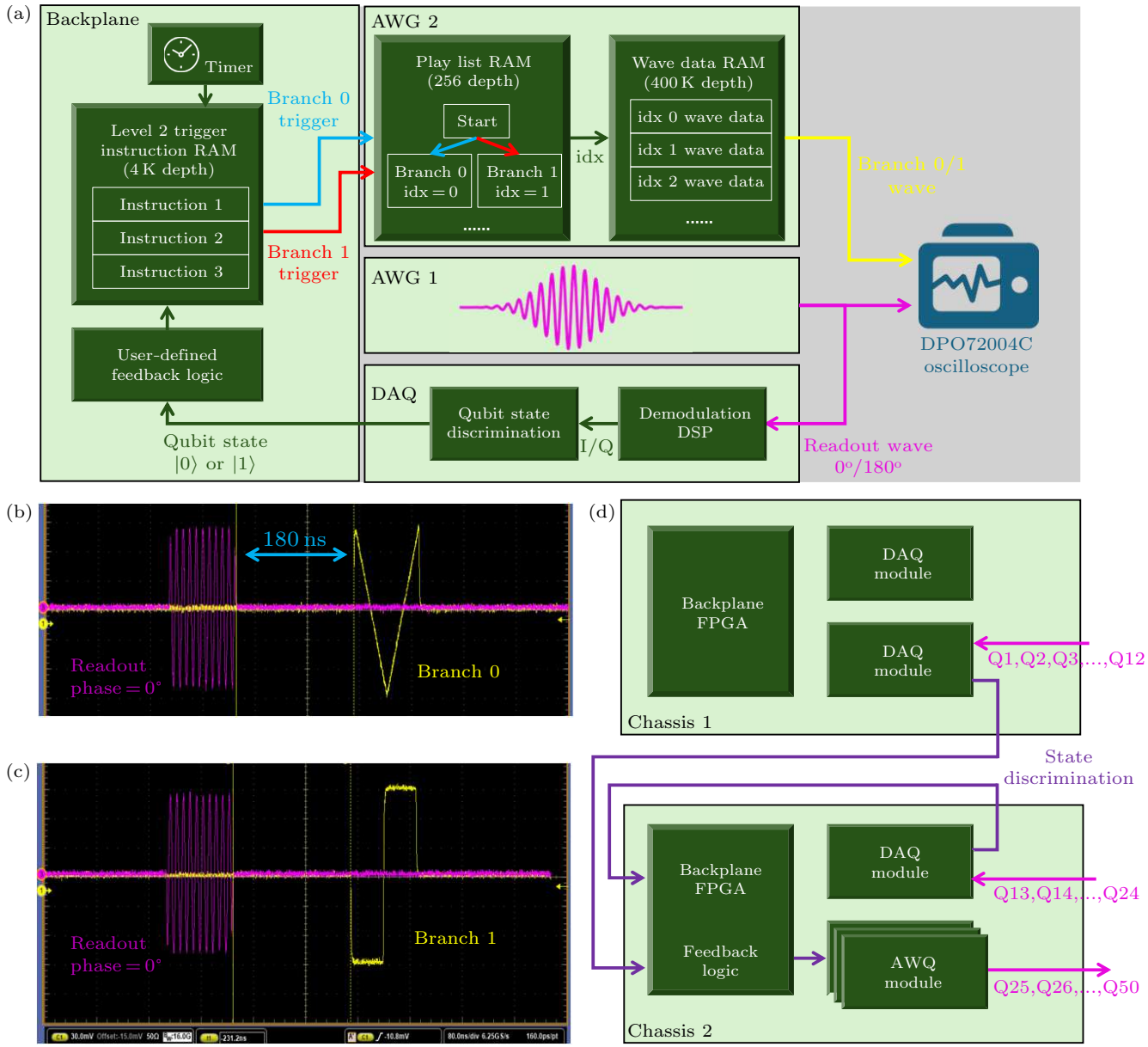


Fig. 7. Feedback loop test. (a) Schematic of the feedback FPGA logic and the feedback loop test setup. (b) and (c) Oscilloscope result capturing that AWG 2 outputs a saw or a square wave depending on the phase of the readout pulse generated by AWG 1. A latency of 180 ns is observed from the end of the readout pulse generated by AWG 1 to the start of the AWG 2 output. (d) An example of non-local feedback.

With the AWG and DAQ fully tested separately, we can connect them together and test the feedback functionality, as shown in Fig. 7. In this test, AWG 1 is used to generate a 100 ns readout wave to the DAQ module with phases of either 0 or 180 degrees to respectively simulate the detection of qubit $|0\rangle$ or $|1\rangle$ state. The DAQ's sampling window is also set to 100 ns to align with the readout waveform. After the DAQ completes the discrimination of the qubit state, the results are transmitted to the backplane via a 1 m ethernet cable.

The backplane's FPGA then dispatches branch trigger signals to AWG 2 based on the outcomes of the state classification. AWG 2 selectively outputs either branch 0 or branch 1 waveform accordingly. AWG 1 and AWG 2 outputs are connected to the oscilloscope via equal-length cables. As illustrated in Figs. 7(b) and 7(c), the total closed-loop latency of the feedback is 180 ns (excluding the 100 ns sampling length). Specifically, the AWG latency is 72 ns, the backplane latency is 24 ns, the DAQ latency is 48 ns, and the remaining 36 ns comes from communication and wiring.

M^{2}CS facilitates non-local feedback operations through a suite of integrated features. Each DAQ module is equipped with an RJ45 port in the front panel for the transmission of state discrimination results, while the backplane is designed with two dedicated RJ45 ports to receive these results. The flexibility of ethernet cable connections between the send and receive ports enables the backplane FPGA to aggregate qubit state data from various readout lines and to command all the AWGs within the chassis, thereby enabling non-local feedback operations. Moreover, the DAQ can establish direct connections to the backplane of another chassis without the need for intermediate data transfer, ensuring that feedback delays within a single chassis and across multiple chassises are con-

sistent, with minor variations attributable to the cable length, see Fig. 7(d) as an example. A limitation in the scalability of non-local feedback in our current design pertains to the number of RJ45 receive ports linked to the backplane FPGA. At present, a single backplane FPGA is capable of receiving input from two DAQ modules, which provides state information for a maximum of 24 qubits, and can manage up to 28 RFAWG channels for feedback purposes. To enhance the scalability of non-local feedback, the integration of a dedicated global feedback module is envisioned to augment the number of send and receive ports.

4. Benchmark with superconducting qubits

To demonstrate the practical performance of M^{2}CS, we utilize it to calibrate our superconducting quantum processor with 66 qubits.[39] The readout resonators of the superconducting qubits are around 6 GHz. As shown in Figs. 8(a) and 8(b), M^{2}CS achieves a readout fidelity of 99.2% for the qubit ground state $|0\rangle$ and 97.4% for the qubit excited state $|1\rangle$, without the assistance of parametric amplifiers. We further benchmark the qubit coherence by measuring the lifetime T_1, the Ramsey T_2, and the echo $T_{2,\mathrm{echo}}$ of the qubits, as shown in Figs. 8(c) and 8(d). In the T_1 measurement, an RF-AWG module outputs a so-called π-pulse at the qubit frequency after up-conversion, flipping the qubit from the ground state $|0\rangle$ to the first excited state $|1\rangle$. After some delay time t, the qubit state is detected using the DAQ to discriminate the probability P_1 of the qubit being in the $|1\rangle$ state. Scanning the delay time t, we observe an exponential decay in P_1 with a decay constant of $T_1 = 128.7$ µs. In the T_2 Ramsey measurement, a $\pi/2$-pulse from an RF-AWG rotates the qubit to an equal superposition of $|0\rangle$ state and $|1\rangle$ state. After some delay time t, another $\pi/2$-pulse is applied, followed by measurement using the DAQ. The probability P_1 of $|1\rangle$ state exhibits an oscillation with evolution time t, where the envelope of this oscillation decays at a dephasing time $T_{2,\mathrm{ramsey}} = 12.0$ µs. In the T_2 spin echo measurement, an additional refocusing π-pulse is added

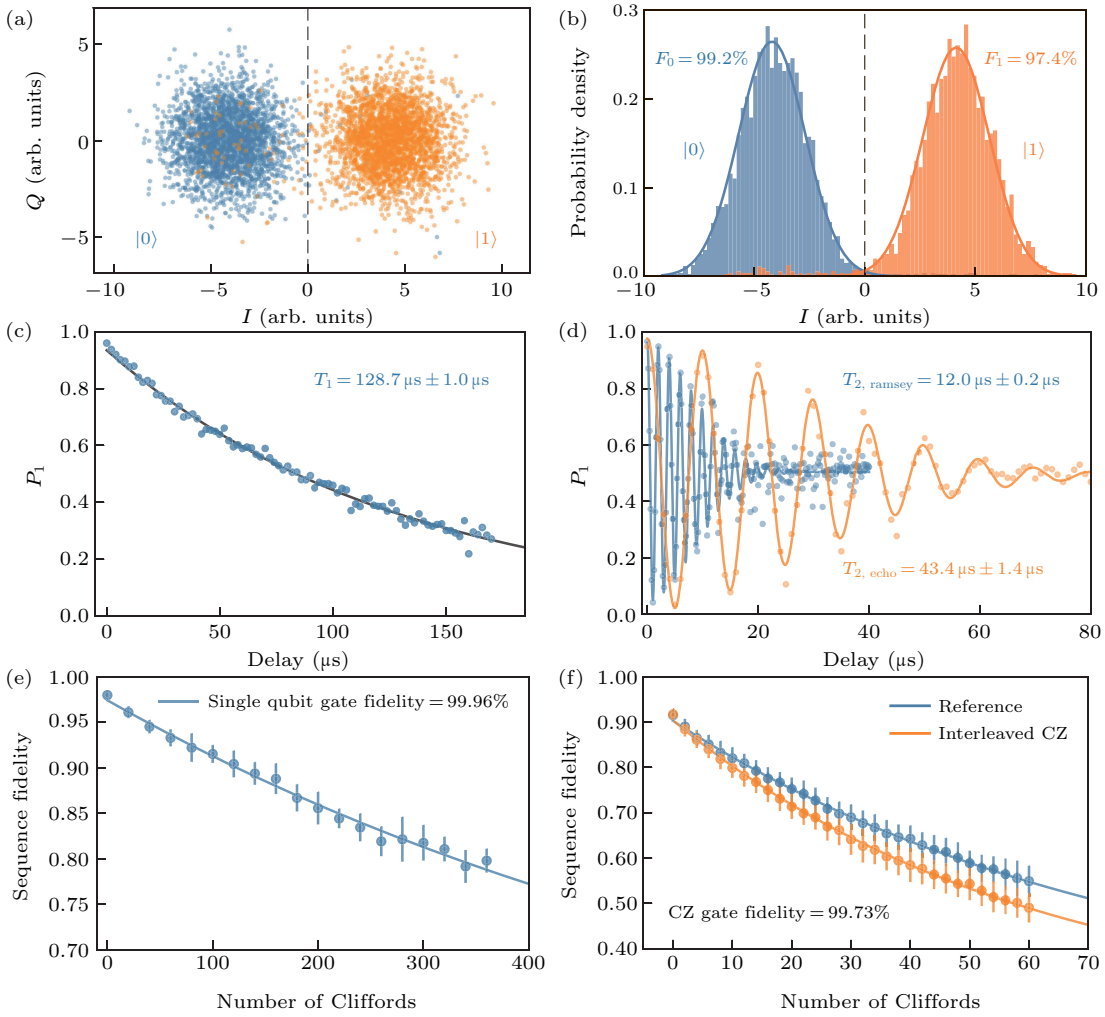


Fig. 8. Benchmarking M^{2}CS with superconducting qubits. (a) IQ scatter plot, where the qubit is prepared in $|0\rangle$ and $|1\rangle$ state respectively. The dashed line is the state discrimination threshold. The in-phase (I) and quadrature (Q) data are expressed in arbitrary units. (b) Histrogram of the data in (a) projected to the horizontal axis, with a readout fidelity of 99.2% for the qubit ground state $|0\rangle$ and 97.4% for the qubit excited state $|1\rangle$. (c), (d) Qubit coherence benchmark, showing a qubit $T_1 = 128.7$ µs, $T_{2,\mathrm{ramsey}} = 12.0$ µs and $T_{2,\mathrm{echo}} = 43.4$ µs, which was measured at the qubit sweet spot. (e), (f) Qubit gate benchmark, showing a single qubit gate fidelity of 99.96%, and two-qubit CZ gate fidelity of 99.73%.

between the two $\pi/2$-pulses to suppress low frequency noise, resulting in a longer coherence time of $T_{2,\text{echo}} = 43.4$ μs. The dephasing time for M^{2}CS is measured at the qubit sweet spot, with a qubit frequency of 3.8 GHz. We further calibrate single qubit gates and two-qubit control-Z (CZ) gates using randomized benchmarking (RB) to extract the gate errors by running m cycles of random Clifford gates,[3] obtaining single qubit gate fidelity of 99.96%, and two-qubit CZ gate fidelity of 99.73%, see Figs. 8(e) and 8(f). Both the qubit coherence and gate fidelities are comparable to state-of-the-art results.

5. Conclusion

In this study, we have demonstrated a microwave measurement and control system (M^{2}CS) tailored specifically for large-scale superconducting quantum processors. This customized and modular design can meet the stringent requirements of quantum experiments running on intermediate-scale quantum processors, effectively balancing overall performance, scalability and flexibility. Electronic tests of M^{2}CS show comparable key metrics to those of commercial instruments. Benchmark tests on transmon superconducting qubits confirm M^{2}CS's capability to control and measure quantum processors, where both the qubit coherence and gate fidelities are comparable to state-of-the-art results. The M^{2}CS architecture may be adopted to a wider range of scenarios, including other quantum computing platforms such as trapped ions[40] and silicon quantum dots,[41] as well as more traditional applications like microwave kinetic inductance detectors (MKIDs)[22,42] and phased array radar systems.

At present, our system is designed to effectively support our 66-qubit device.[39] However, given the compact and scalable nature of our design, we believe there is substantial potential for future enhancements. Here we consider the feasibility of supporting over 1000 qubits. Managing 1000 qubits requires several thousands of control channels, or roughly 100 chassises. A standard 42U rack can house up to 5 chassises, meaning 20 racks would be needed. Each rack occupies approximately 1 m^2. Thus, 20 racks would require around 20 m^2 of floor space. In terms of power, each chassis consumes approximately 450 W. Therefore, the total power consumption for 100 chassises would be around 45 kW. M^{2}CS's two-level trigger structure allows each master chassis to trigger up to 10 slave chassises. For a 100-chassis system, a three-level trigger structure would be sufficient to trigger all slave chassises from the master. Any delays introduced by each trigger level can be calibrated using the FPGA's programmable IO delay, ensuring precise waveform alignment across all levels. These resource assessments for supporting 1000 qubits show that it is indeed feasible, especially when the system stability and integration are further enhanced.

Acknowledgments

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