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Citation: Chin. Phys. B, 2024, 33 (**12**): 128502. DOI: 10.1088/1674-1056/ad8072
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A macro model of spin-transfer torque magnetic tunnel junction

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(Received 19 July 2024; revised manuscript received 27 September 2024; accepted manuscript online 27 September 2024)

The precise compact modeling of magnetic devices is pivotal for the integrated design of spin-transfer torque magnetic tunnel junction (STT-MTJ) in conjunction with CMOS circuitry. This work presents a macro model for an STT-MTJ which is compatible with SPICE simulation platforms. The model accurately replicates the electrical performance of the MTJ, encompassing the resistance-voltage characteristics and the pulse-width-dependent state switching behavior, and is validated with various experimental data. Additionally, the impact of process variations, particularly those affecting the MTJ diameter and barrier thickness is investigated and summarized in a corner model. Monte Carlo simulations demonstrate that our adaptable and streamlined model can be efficiently incorporated into the design of integrated circuits.

Keywords: STT-MTJ, macro model, process corner, Monte Carlo simulation

PACS: 85.70.Ay, 85.75.Dd **DOI:** 10.1088/1674-1056/ad8072

1. Introduction

Spin-transfer torque magnetic random access memory (STT-MRAM) is a promising technology for the next-generation non-volatile memory, offering advantages such as fast write speed, low power consumption, and high density.[1–4] The key element of an STT-MRAM device is a magnetic tunnel junction (MTJ) which consists of a thin barrier layer of MgO sandwiched between two ferromagnetic layers. Despite its considerable potential in STT-MRAM, the MTJ faces performance challenges due to process variations, including fluctuations in oxide thickness, surface roughness, and critical diameter (CD), all of which can significantly impact the device and overall circuit performance. Therefore, it is imperative to evaluate circuit tolerance to these process variations using an MTJ device model during the design phase to ensure the functionality of the chip.

The advent of memory designs that integrate both MTJ and CMOS technologies necessitates the use of SPICE-based models for simulating these hybrid circuits. Two types of SPICE models of STT-MTJ devices have been reported. The first type is predicated on the Landau–Lifshitz–Gilbert (LLG) equation.[5–8] These LLG-based models solve the complete LLG equation to forecast the MTJ's magnetic dynamics under various magnetic fields and write waveforms. While they capture the full physical details within an MTJ and can predict its performance without relying on experimental data, their complexity and computational intensity render them unsuitable for large-scale integrated circuit simulations. Conversely, macro models[9–11] are founded on compact equations that describe current-induced magnetic state switching and employ circuit components to emulate the electrical attributes of MTJ devices. Although macro models are of high computational efficiency, they fall short in providing detailed insights into MTJ magnetization dynamics and stochastic behaviors. Furthermore, most reported macro models overlook the parameter variations stemming from non-uniformities in the MTJ manufacturing process, thus limiting their applicability in realistic STT-MRAM chip design.

In this paper, we propose a macro model that accurately depicts the electrical behavior of STT-MTJ[12] with perpendicular magnetic anisotropy (PMA), encompassing the influence of process variations on some of the critical parameters of MTJ devices. To gather such variations, corner bias split experiments are dedicatedly designed to observe the effects of MTJ diameter and barrier thickness on performance. A corner model is subsequently constructed based on experimental measurements and corroborated through Monte Carlo simulations. The fitting results demonstrate a high degree of concordance with in-line data, affirming the proposed macro model and its methodology hold substantial promise for the design of STT-MRAM chips.

2. Device model

2.1. MTJ structure

The MTJ exhibits a multilayer structure, which is composed of a free magnetic layer (FL) and a reference layer (RL), separated by an ultra-thin insulating layer. Figure 1 provides a schematic representation of an MTJ with PMA (pMTJ) and its equivalent circuit. In this configuration, the magnetic moments of both the RL and FL are oriented perpendicular to the plane of the layers. Compared to MTJs that feature

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in-plane magnetic anisotropy, pMTJs benefit from enhanced thermal stability and a reduced form factor.[12] The equivalent circuit of an MTJ is characterized by a two-terminal voltage-controlled resistor, denoted as $R_{\rm MTJ}$. The read and write operations are facilitated by the application of an appropriate voltage across the MTJ, inducing the switching of the magnetic state within the FL.

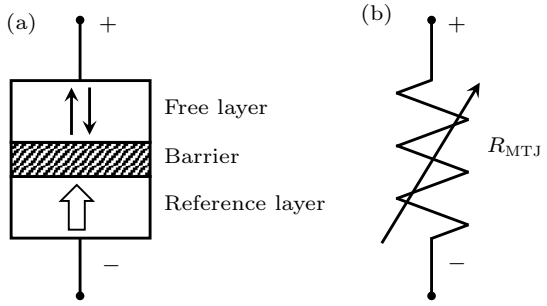


Fig. 1. (a) Structure of the pMTJ device, (b) equivalent circuit indicating the device resistance $R_{\rm MTJ}$.

2.2. Tunneling magnetoresistance ratio

The MTJ is in a low resistive state (logically defined as 0) when the magnetic moments of the two ferromagnetic layers are parallel (P), while it is in a high resistive state (logically defined as 1) when these magnetic moments are anti-parallel (AP). The distinction in resistance between these two states is quantified by the tunnel magnetoresistance ratio (TMR),[13,14]

$$\mathrm{TMR} = \frac{R_{\rm AP} - R_{\rm P}}{R_{\rm P}}, \tag{1}$$

where $R_{\rm P}$ is the resistance of the P state, and $R_{\rm AP}$ is the resistance of the AP state.

The device resistance of the AP state decreases with an increment in bias voltage, which can be approximated by the Gaussian function,[15] or derived from the MTJ conductance physical model.[13] Its temperature dependence can be explained by Julliere-based model[16–18] or phonon-assisted tunneling model.[19,20] Our resistance model for STT-MTJ is phenomenological, as depicted in equation set

$$\begin{cases} R_{\rm MTJ} = R_{\rm P}, & \text{MTJ at "P" state,} \\ R_{\rm MTJ} = R_{\rm AP}, & \text{MTJ at "AP" state,} \end{cases} \tag{2a}$$

$$R_{\rm P}(V,T) = R_{\rm P0}, \tag{2b}$$

$$R_{\rm AP}(V,T) = \frac{R_{\rm P}(V,T)}{a(T)\cdot V_{\rm MTJ}^2 + b(T)\cdot V_{\rm MTJ} + c(T)}, \tag{2c}$$

where $R_{\rm MTJ}$ represents the MTJ resistance, $R_{\rm P0}$ is the constant resistance, $V_{\rm MTJ}$ is the applied MTJ voltage, and T is the ambient temperature in degrees Celsius. The parameters a, b, and c are temperature-dependent, as detailed in the following:

$$a(T) = a_{T25}[a_{\rm r}(T-25)+1], \tag{3a}$$

$$b(T) = b_{T25}[b_{\rm r}(T-25)+1], \tag{3b}$$

$$c(T) = c_{T25}[c_{\rm r}(T-25)+1], \tag{3c}$$

where coefficients a_{T25}, b_{T25}, and c_{T25} represent their values at room temperature, with $a_{\rm r}$, $b_{\rm r}$, and $c_{\rm r}$ being the respective temperature coefficients. The current flowing through the device is given by Ohm's law, $I = V_{\rm MTJ}/R_{\rm MTJ}$.

In this model, the thickness and area dependence of the MTJ resistance are not considered. This implies that the MTJ device integrated into the circuit design possesses a fixed CD and a constant resistance-area product (RA), given by the design rules of any mainstream manufacturing platform. The CD is the diameter of the MTJ pillar at the MgO barrier level, while the RA parameter is exponentially related to the oxide thickness.[14] Both parameters significantly influence the MTJ resistance and the write voltage.

2.3. Switching voltage

For an STT-MTJ, the device resistive state can be altered by applying an appropriate write voltage (or current), termed as critical voltage $V_{\rm c}^{\rm P-to-AP}$ and $V_{\rm c}^{\rm AP-to-P}$ for writing 1 and 0, respectively. However, factors such as thermal fluctuation and the initial angle of the magnetic moments in the FL induce randomness during state switching.[21,22] The critical voltage here corresponds to the write voltage with a switching probability of 50%, which is determined by statistical measurements across multiple MTJ devices. Notably, the critical switching voltages for the two states may differ.[12]

The commonly referenced physical model that illustrates the pulse width dependence of $V_{\rm c}$ was proposed by Slonczewski[23] and Sun,[24] and has been incorporated into previous compact models. Our switching model, however, articulates this dependence through Eq. (4), where τ is the duration of a square pulse, and $a_{\tau1}$, $a_{\tau2}$, $b_{\tau1}$, and $b_{\tau2}$ are fitting parameters for pulse width dependence. Additionally, a_{V1} and a_{V2} are fitting parameters for temperature dependence. In this model, the relationship between critical voltage and operating temperature is linearly defined, although it can be expanded to a quadratic or higher-order function to achieve a better fit.

$$V_{\rm c}^{\rm AP-to-P}(\tau,T) = (a_{\tau1}\ln\tau + b_{\tau1})\times[a_{V1}(T-25)+1], \tag{4a}$$

$$V_{\rm c}^{\rm P-to-AP}(\tau,T) = (a_{\tau2}\ln\tau + b_{\tau2})\times[a_{V2}(T-25)+1]. \tag{4b}$$

Akin to other macro models, our model supports only constant pulse voltage or current input. The fitting parameters are derived from pulsed I–V measurements, which employ a series of square pulses with escalating pulse levels across various pulse durations. Consequently, the switching voltage model may exhibit reduced accuracy under different waveform types.

2.4. Model validation

The proposed macro model is implemented in the Verilog-A language and validated against experimental data. An initial assessment involves examining the R–V characteristics at various temperatures and comparing the TMR with experimental results. Figure 2 shows this comparison, with the

data obtained from DC measurements. In our device model, R_P is assumed to be constant when varying the applied voltage V_{MTJ} and temperature,[25,26] which simplifies the *R*–*V* characteristic expression and performs adequately under low voltage conditions. R_{AP} decreases as V_{MTJ} increases, and the *R*–*V* curve shrinks with rising operating temperature, a behavior that is accurately captured by the model. Figure 3 demonstrates the temperature dependence of TMR at $V_{MTJ} = 50$ mV. A more pronounced discrepancy between the simulation and empirical outcomes is noticeable at temperatures below 0 °C, which may be attributed to the different experimental apparatus employed for low-temperature and high-temperature measurements.

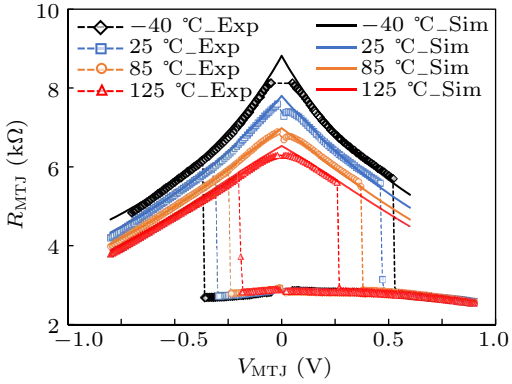


Fig. 2. Validation of the proposed model through the *R*–*V* curve at different temperatures. The dashed lines with symbols represent the experimental results, while the solid lines depict the model results.

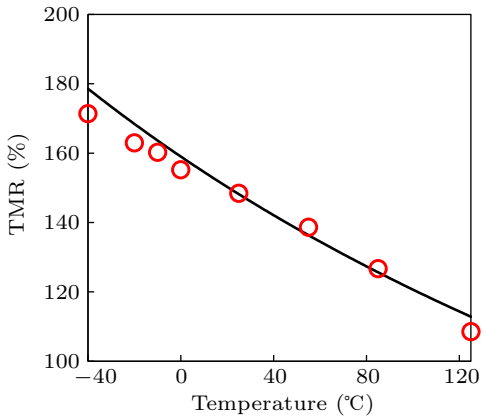


Fig. 3. Temperature dependence of TMR at $V_{MTJ} = -50$ mV. The symbols denote the experimental data, and the fitting line shows good agreement with the experiment around room temperature.

In the next, performance of the model under various write pulse widths is examined. It is common that P-to-AP and AP-to-P critical switching voltages differ, and the switching speed increases with pulse level. Figure 4 displays the relationship between pulse-width-dependent critical voltage and experimental data. The worst fit is observed at the shortest pulse width of 20 ns. For most cases, our model aligns well with the measurements at different temperatures. Taking AP-to-P switching as an example, the temperature dependence of critical voltage with varied pulse durations is also delineated in Fig. 5, exhibiting a linear correlation between V_c and temperature. All simulated results exhibit a consistency of over 90%, reinforcing the validity and robustness of our model.

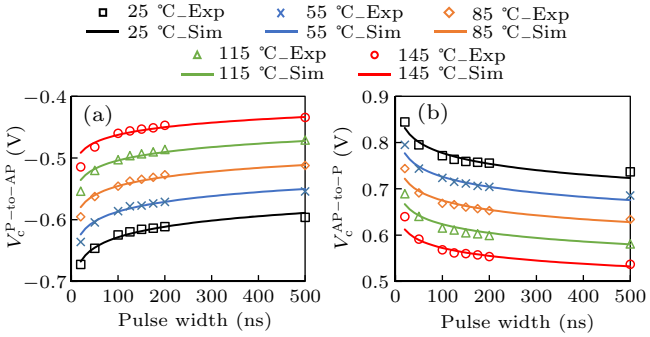


Fig. 4. Validation of pulse-width-dependent critical voltage $V_c^{P-to-AP}$ (a) and $V_c^{AP-to-P}$ (b) at different temperatures. The symbols are the experimental data, while the lines show the model results, revealing a logarithmic function relationship between critical voltage and pulse width.

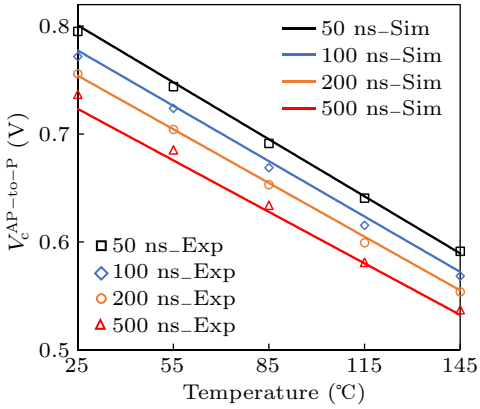


Fig. 5. Dependence of critical voltage $V_c^{AP-to-P}$ on temperature at different pulse widths. The symbols are the experimental data, and the lines indicate the model results.

Finally, transient simulations are conducted by applying square pulse waves with different pulse widths to verify the write operation. As shown in Fig. 6, P-to-AP and AP-to-P switching occurs once the applied voltage level reaches sufficient time. An abrupt change in current is detected, corresponding to the state switching between P and AP states. A higher voltage level leads to faster switching speed, and $V_c^{P-to-AP}$ and $V_c^{AP-to-P}$ can be different, as described by Eq. (4).

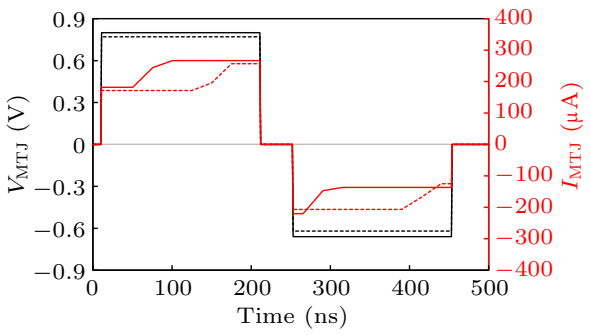


Fig. 6. State transition under pulse of two different voltage level conditions. A higher pulse level (solid line) indicates more rapid switching for both AP-to-P and P-to-AP state transitions.

3. Process corner and Monte Carlo model

Like standard CMOS processes, MTJs are fabricated by following a sort of techniques. The key steps include the sputtering of the MTJ stack, photolithography, and film etching, which determine the CD and RA of the MTJ. Owing to unavoidable process fluctuations, the properties of MTJ nanopillars vary from wafer to wafer, also from die to die. Such fluctuations exert a significant influence on the electrical switching behavior and must be meticulously evaluated prior to IC design.[11,27,28]

Our compact model does not facilitate the study of technology scaling since it lacks the incorporation of CD and barrier thickness. To optimize the design of a bitcell, it is imperative that the variation sources be embedded into the model. Therefore, the statistical distribution of electrical parameters including $R_{\rm P}$, $R_{\rm AP}$, TMR, $V_{\rm c}^{\rm P-to-AP}$, and $V_{\rm c}^{\rm AP-to-P}$ should be provided. The variability of these parameters is investigated through corner bias split experiments. Consequently, the electrical switching behavior of the MTJ device can be comprehensively characterized using Monte Carlo simulations.

3.1. Process corner experiment

To investigate the influence of process variation on MTJ devices, corner bias split experiments are performed using five pieces of wafers. Table 1 presents the detailed process conditions for each wafer, where RA and CD are varied systematically. The RA is controlled and evaluated based on the deposition time of the barrier layer, while the CD is adjusted by the exposure condition during lithography. These two technology parameters are persistently monitored in-line, employing statistical process control (SPC) to ensure their values remain within the specified upper and lower thresholds. We expect to characterize process corners using these two variants and develop an MTJ corner model.

More specifically, wafer #1 is under baseline (BSL) condition, whereas the RA for wafers #2 and #4 is increased by 0.5 $\Omega\cdot\mu{\rm m}^2$, and for wafers #3 and #5, it is decreased by 0.5 $\Omega\cdot\mu{\rm m}^2$. With the exception of the BSL wafer #1, the surface of each wafer is divided into two distinct areas: the MTJ CD in the left semicircle is either BSL +2 nm (for wafers #2,3) or BSL +4 nm (for wafers #4, 5), and the MTJ CD in the right semicircle is either BSL −2 nm (for wafers #2, 3) or BSL −4 nm (for wafers #4, 5), as depicted in Fig. 7. The bias of RA and CD is in accordance with the process fluctuation monitored inline to ensure that the extracted parameters can be effectively utilized in our MTJ model.

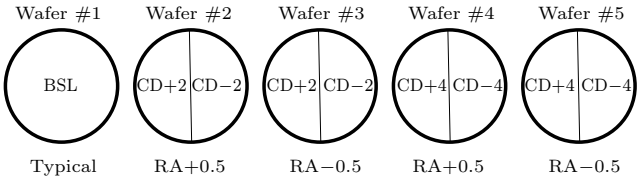


Fig. 7. Process corner bias split across five wafers. Unlike the BSL wafer, the surface of each wafer is segregated into two regions to accommodate asymmetric CD biases. The RA is split into three conditions, reflecting variations in barrier thickness.

Table 1. Corner bias split table.

Process	Parameter	Condition	1	2	3	4	5
MTJ deposition	RA	BSL	√				
		$+0.5\ \Omega\cdot\mu{\rm m}^2$		√		√	
		$-0.5\ \Omega\cdot\mu{\rm m}^2$			√		√
MTJ lithography	CD	BSL	√				
		dual-quadrant CD +/− 2 nm		√	√		
		dual-quadrant CD +/− 4 nm				√	√

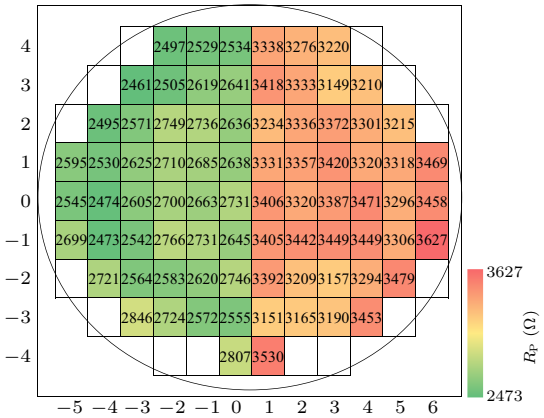


Fig. 8. The $R_{\rm P}$ mapping of wafer #4. MTJs in the left part have a larger CD and thus exhibit a smaller measured $R_{\rm P}$.

To verify the CD bias in each wafer, we check the $R_{\rm P}$ mapping diagram. For instance, the mapping of average $R_{\rm P}$ for each die on wafer #4 in Fig. 8 reveals a smaller $R_{\rm P}$ in the left semicircle and a larger $R_{\rm P}$ in the right semicircle. Given that $R_{\rm P}\propto {\rm RA}/{\rm CD}^2$, a larger CD results in a smaller $R_{\rm P}$ for the same RA, which consists with our expectations.

3.2. Experiment results

TMR and $R_{\rm P}$ data are collected from a wafer access test with a sampling of over 350 devices, while the $V_{\rm c}$ data are collected over 60 samples from pulsed *I*–*V* experiments. The dependencies of $\Delta R_{\rm P}$, ΔTMR, $\Delta V_{\rm c}^{\rm P-to-AP}$, $\Delta V_{\rm c}^{\rm AP-to-P}$ on RA and CD are illustrated in Fig. 9. Theoretically, the dependence of MTJ parameters on RA and CD is governed by a complex set of expressions.[9] However, within the narrow split range

here, we approximate these relationships linearly, considering only first-order functions.

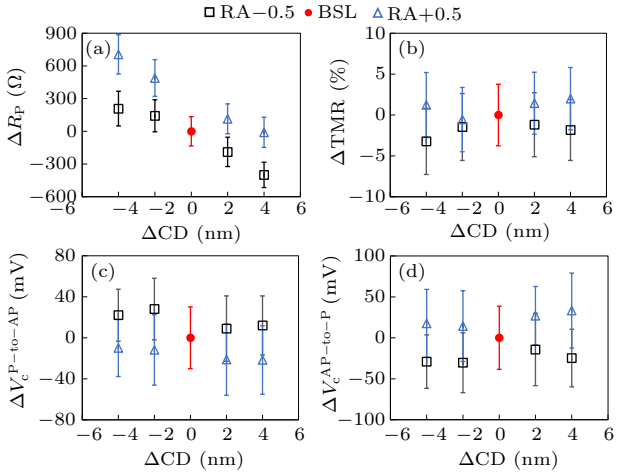


Fig. 9. CD and RA dependence of (a) $\Delta R_{\rm P}$, (b) ΔTMR, (c) $\Delta V_{\rm c}^{\rm P-to-AP}$, and (d) $\Delta V_{\rm c}^{\rm AP-to-P}$ for the MTJ electrical behavior.

The outcomes of the linear fitting are summarized in Table 2. The variations in CD have little effect on TMR and $V_{\rm c}$, but an increasing trend in CD correlates with a decrease in RA. The tight distribution of $R_{\rm P}$ demonstrates excellent device uniformity, suggesting that within-wafer-level variations have been minimized. This is likely due to the mitigation of edge damage during the MTJ etching through our optimized process. An increment in RA by 0.5 $\Omega\cdot\mu{\rm m}^2$ results in an approximate deviation of 200 Ω in $R_{\rm P}$ and 20-mV deviation in $V_{\rm c}$. Given the significant impact of RA on both read and write operations, there is a need to enhance the process control of RA to avoid limiting the performance of the memory array when integrated with CMOS technology.

Table 2. Fitting matrix of process corner experiment.

Parameter	Unit	ΔCD factor, a	ΔRA factor, b
$\Delta R_{\rm P}$	Ω	−84	384
ΔTMR	%	0	3
$\Delta V_{\rm c}^{\rm P-to-AP}$	mV	1.8	34
$\Delta V_{\rm c}^{\rm AP-to-P}$	mV	1.7	48

$\Delta[\text{Parameter}] = a\times\Delta\text{CD} + b\times\Delta\text{RA}$

Combining the influence of CD and RA fluctuations obtained above, a total deviation range of $\Delta R_{\rm P} = \pm 550$ Ω can be obtained, which agrees with the global corner data monitored from the in-line database. Leveraging the results from the process corner bias split experiments, an MTJ SPICE-based corner model can be constructed. We also embed the local mismatch into the macro model derived from the macro test in a chip.

3.3. Monte Carlo simulation results

In reference to CMOS process corners, our MTJ model, embedded with which incorporates sources of process variation, defines three corners: TG, LG, and HG. The "TG" corner represents the typical global corner, which describes the average behavior of most devices, characterized by a mean value of resistance and switching voltage. The "LG" and "HG" corners represent the global process corners arising from manufacturing variations. Specifically, the "LG" corner devices exhibit lower $R_{\rm p}$, whereas the "HG" corner corresponds to devices with higher $R_{\rm p}$. These global corners support local variation function, which are validated through Monte Carlo simulations, as shown in Fig. 10. For each global corner, ten thousand simulations are performed, taking in account mismatch variations, which exhibits the distributions of $R_{\rm P}$ and $R_{\rm AP}$. The $R_{\rm AP}$ distribution exhibits greater variability than the $R_{\rm P}$ distribution. MTJs at the designed LG corner have smaller resistance, whereas those at the FG corner demonstrate larger resistance compared to the TG corner for both high and low resistive states. By integrating our model with the standard CMOS model, further exploration of MRAM bitcells and large memory arrays can be pursued, incorporating such variations.

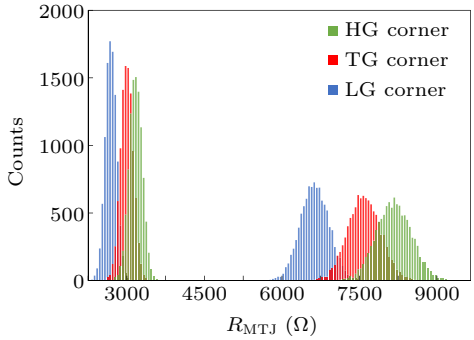


Fig. 10. Resistance distributions at different global corners, including local variation effects, using Monte Carlo simulations. Three sets of data on the left correspond to $R_{\rm P}$ distributions, while the other three sets on the right represent $R_{\rm AP}$ distributions.

We also run Monte Carlo simulations to verify the P-to-AP state switching with our corner model. Figure 11 shows the influence of device variation on the write functionality at the TG corner. An overdrive is recommended to definitely realize the data writing, based on the standard deviation of $V_{\rm c}$ or write error rate test.

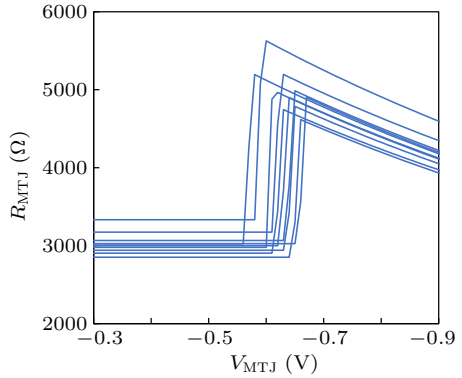


Fig. 11. Monte Carlo simulations demonstrating the P-to-AP transitions at different write voltages.

Finally, we demonstrate the capability to optimize an MRAM bitcell using our model. A typical MRAM bitcell is

based on the one transistor one junction (1T-1MTJ) configuration as illustrated in Fig. 12. The NMOS transistor is used for accessing the MTJ via the bit line (BL) when the gate node (WL) voltage is high. By using the 14-nm CMOS technology design kit and our MTJ macro model, 1T-1MTJ Monte Carlo simulations are performed at the SS corner for NMOS and the LG corner for MTJ. The minimum bit line voltage $V_{\rm BL}$ required to achieve AP-to-P switching is plotted against various word line voltage $V_{\rm WL}$ for transistors with either two fins or four fins at one finger, a length of 16 nm, and at room temperature. As anticipated, transistors with more fins and higher $V_{\rm WL}$ offer an increased current supply capability. MTJ device variation significantly impacts the selection of power supply components and transistor type.

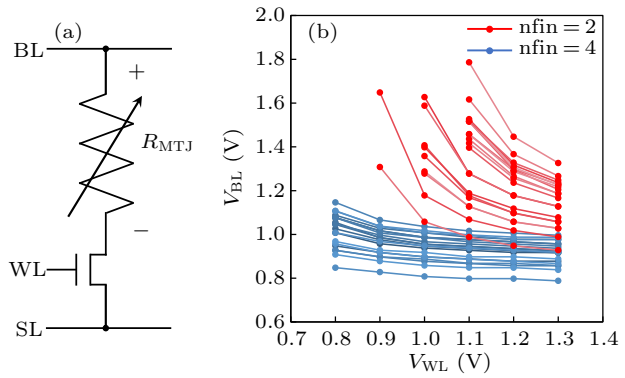


Fig. 12. Bitcell simulation results: (a) circuit diagram composed of one transistor and one MTJ; (b) Monte Carlo simulations with twenty attempts displaying the required $V_{\rm BL}$ versus $V_{\rm WL}$ for AP-to-P switching at 2 fins (red) and 4 fins (blue), one finger, 16-nm length, and room temperature. The source line is grounded. The transistor operates at the SS corner and the MTJ is positioned at the LG corner. $V_{\rm BL}$ values exceeding 2 V are not included in the graph.

4. Conclusion

The macro model of STT-MTJ presented here is implemented in the Verilog-A language, enabling its efficient integration with popular circuit simulators to design MRAM circuits in conjunction with CMOS devices and other components. Our compact model accurately captures the electrical behavior of the MTJ by phenomenological equations. Process variations affecting the RA and CD are thoroughly investigated utilizing corner bias split experiments. These investigations are embedded into our model, providing a clear illustration of resistance distributions and variations in critical voltage. To elucidate the impact of device variation on circuit design, we have designed and simulated a simple 1T-1MTJ bitcell.

One limitation of our model is its lack of consideration for the technological scaling of the MTJ, such as the shrinking of radius and the optimization of barrier thickness. Notwithstanding this limitation, the model is flexible and can be updated to accommodate the evolving electrical characteristics of STT-MTJs, thereby supporting the advancement of nonvolatile, MTJ-based very large-scale integrated circuit designs.

Acknowledgements

Project supported by the National Science and Technology Major Project of China (Grant No. 2020AAA0109003). We also acknowledge the support from Hikstor Pilot line.

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