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Back-side stress to ease p-MOSFET degradation on e-MRAM chips

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The magnetoresistive random access memory process makes a great contribution to threshold voltage deterioration of metal–oxide–silicon field-effect transistors, especially on p-type devices. Herein, a method was proposed to reduce the threshold voltage degradation by utilizing back-side stress. Through the deposition of tensile material on the back side, positive charges generated by silicon–hydrogen bond breakage were inhibited, resulting in a potential reduction in threshold voltage shift by up to 20%. In addition, it was found that the method could only relieve silicon–hydrogen bond breakage physically, thus failing to provide a complete cure. However, it holds significant potential for applications where additional thermal budget is undesired. Furthermore, it was also concluded that the method used in this work is irreversible, with its effect sustained to the chip package phase, and it ensures competitive reliability of the resulting magnetic tunnel junction devices.

Keywords: back-side stress, metal–oxide–silicon field-effect transistor (MOSFET), magnetoresistive random access memory (MRAM), threshold voltage

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1. Introduction

The technology of spin-transfer-torque magnetoresistive random access memory (STT-MRAM), based on perpendicular magnetic tunnel junction (MTJ), has emerged as a promising solution for next generation non-volatile memory. Due to its high density, low power, superior endurance and high data retention capabilities along with scalability beyond 28 nm at reduced cost, this approach is poised to replace embedded-flash and static random access memory (SRAM) technologies. MRAM is now a key enabler of embedded applications such as low-power microcontroller units (MCUs), and wearable and Internet of things (IoT) applications.[1–3] MRAM devices are usually embedded in an interconnect structure disposed over a substrate, and are independent of transistor processing steps. However, MRAM integration involves several metallization steps, some differing from traditional interconnection processes. The stress arising from these additional and unconventional metallization steps cannot be overlooked. Previous research indicates that tensile stress negatively impacts MOSFET performance, particularly on p-MOSFETs.[4–6] Given the concurrent presence of MRAM and other logic intellectual properties (IPs), it is of considerable significance to ensure consistent device performance throughout MRAM integration.

In the standard complementary metal oxide semiconductor (CMOS) process, post H_2 annealing is extensively used to repair the damage caused during the fabrication process, such as plasma-induced damage and fixed interface charge.[7–10] However, the MTJ is vulnerable when subjected to additional thermal processes or extra H atoms, which can negatively impact MTJ device performance and reliability.[11–14]

In this paper, a solution to ease the p-MOSFET degradation on e-MRAM chips by applying wafer back-side (BS) stress is reported. The effect was maintained despite the removal of the BS material, indicating that the method was irreversible and could be advantageous not only at wafer level but also from a packaging perspective. Moreover, using this method, the MTJ devices still presented competitive performance on endurance and data retention.

2. Materials and methods

This study employed a dual approach to preparing wafers. Initially, a logic-only wafer underwent the standard foundry gate-last high-K metal gate process, followed by the standard back-end-of-line (BEOL) process. Conversely, the MRAM-integrated wafer was elaborated through a sequential patterning of bottom via (BV), bottom electrode (BE), magnetic tunneling junction (MTJ) and top electrode (TE) on the inter-metal level. Then, the standard BEOL process involving top via (TV) and top metal (TM), aluminum pad (Al) and a passivation was conducted. Figure 1(a) depicts the schematic structure of the MRAM-integrated device, with MRAM-specific steps (dashed line box) distinguished from common processes

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(solid line box), as illustrated in Fig. 1(b). Two components, MOSFET and MTJ, are shown in Fig. 1(a). To be more specific, the MTJ was integrated between metal 4 and TM. The MTJ was composed of a seed layer, Co/Pt-based synthetic antiferromagnetic (SAF) layers, MgO barrier, and a CoFeB-based free layer with a MgO cap, as shown in Fig. 1(a). The base pressure was approximately 10^{-9} Torr, and the deposition pressure was less than 1 mTorr. Metallic layers and MgO layer were deposited by direct current (DC) and radio frequency (RF) magnetron sputtering, respectively.

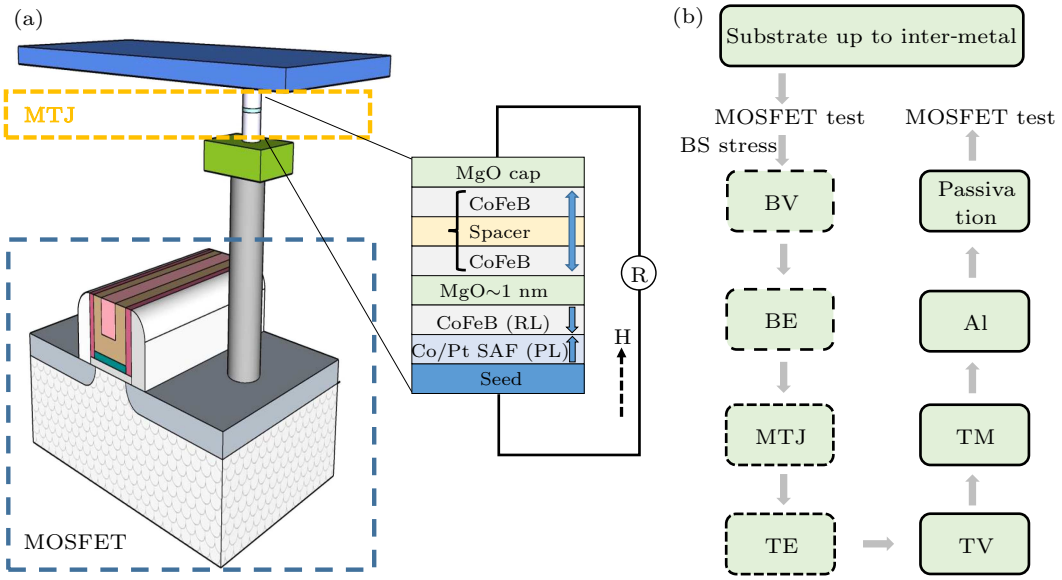


Fig. 1. (a) Schematic structure and connection relationship between MOSFET and MTJ and (b) preparation steps of MRAM integrated chip. BS stress was applied just before MRAM loop, that is, before BV preparation. MOSFET tests were carried out before MRAM loop and after passivation.

The BS stress was achieved by SiN ($\sim$ 3000 Å), which was deposited through chemical vapor deposition (CVD) at 220 °C for 60–85 s, since its deposition and removal method are compatible with the common wafer fabrication process. In order to enhance the adhesion between silicon nitride (SiN) and bare Si substrate, a thin layer ($\sim$ 300 Å) of tetraethoxysilane (TEOS) was deposited at 250 °C for 2.5 s prior to SiN deposition. To control the stress, different SiH_4:NH_3 ratios were adopted, with a higher ratio yielding more compressive stress and a lower ratio resulting in tensile stress.

To remove the BS materials, chemical mechanical polishing (CMP) was utilized, followed by cleaning with diluted hydrofluoric acid (DHF). CMP was used to remove bulk material, while longtime DHF cleaning was employed to thoroughly remove the remaining material.

Furthermore, warpage measurements were conducted using an ellipsometer to gauge the distance between the detector and the wafer surface along the diameter (49 points). The reference was established using a bare silicon substrate with the overall warpage determined by the differential between the experimental and reference wafers.

This study focused on the electrical characteristics of MOSFET devices, including threshold voltage (V_{TH}), saturation drain current (I_{Dsat}) and linear drain current (I_{Dlin}). V_{TH} was determined using a constant current method, I_{Dlin} was extracted when $V_{GS} = V_{DD}$ and $V_{DS} = 0.1$ V, and I_{Dsat} was obtained when $V_{GS} = V_{DS} = V_{DD}$. These electrical properties were scrutinized at various stages, including the pre-MRAM loop (pre-BV preparation) and post-Al (final test). To give a statistical analysis, over 50 MOS devices were tested. In order to investigate the interface quality of MOSFET due to the MRAM BEOL process, the capacitance–voltage (CV) curve was measured for the device, which was swept from accumulation to inversion phase. The electrical characteristics were determined and CV curve measurements were performed in a 12 inch wafer testing system. The CV measurement was done with an amplitude of $1.1V_{DD}$ modulated by a small sinusoidal alternating current (AC) modulation voltage with a frequency of 100 kHz. For the above measurements, two distinct test structures were employed: a single MOSFET device with dimensions of 0.03 μm length and 0.6 μm width for p-MOSFET (0.3 μm for nMOSFET) for device electrical characteristics, and a p-MOSFET capacitance test structure with an area of 1150 μm^2. There was approximately a 1 mm distance between the tested devices and the MRAM chip on the wafer, ensuring good correlation between the devices used in the chip. In addition, four kinds of devices, i.e., high-threshold voltage device (HVT), regular-threshold voltage device (RVT), low-threshold voltage device (LVT) and ultra-low threshold voltage device (uLVT), were assessed. The difference between them lies in the doping level of N or P well.

The post H_2 annealing process was carried out in a thermal annealing furnace at 350 °C for half an hour with 5% H_2 purging into the furnace, mirroring the best-known method

(BKM) used by foundries.

The H_c of free layer was defined as the magnetic field when resistance of MTJ changed under a sweeping magnetic field. The measurements were performed in a commercial 12 inch wafer testing system with a maximum available field of 6 kOe applied perpendicular to the film plane. Tunneling magnetoresistance (TMR) was calculated by the following equation:

$$\mathrm{TMR}(\%) = \frac{R_h - R_0}{R_0} \times 100\%,$$

where R_h and R_0 stand for the higher and lower resistance value, respectively, measured during the H_c test.

Bipolar voltage pulses were used for endurance measurement. Herein, the Weibull distribution equation was fitted to the test results as $\ln(-\ln(1-F)) = \beta(\ln(t) - \ln(\alpha))$, where F denotes a failure probability, t represents the breakdown cycle, β refers to a shape parameter and α is a characteristic breakdown cycle. β was obtained from the slope, and α from the intercept for each stress voltage.[15–17] For data retention tests, the effective energy barrier ($E_b/(kT)$) at three different acceleration temperatures was measured, and the data were linearly fitted to the desired temperature.[18,19]

3. Results and discussion

The threshold voltage shift (ΔV_{TH}) was calculated by the absolute threshold voltage (V_{TH}) value difference between post passivation and the pre-MRAM loop. Figure 2(a) presents V_{TH} shifts due to MRAM integration under different conditions. The logic-only wafer (without MRAM) was the control group. It could be observed that compared with the logic-only wafer where the V_{TH} shift could be disregarded, the MRAM process contributed significantly to the V_{TH} deterioration, especially on p-MOSFET, where V_{TH} increased by as much as 50 mV across various p-type devices. On the other hand, BS tensile stress could ease this phenomenon by 10 mV (around 20%). The dashed line in Fig. 2(a) indicates the tolerable V_{TH} shift range, revealing that the chip function might not be guaranteed in the case of any data beyond this range.

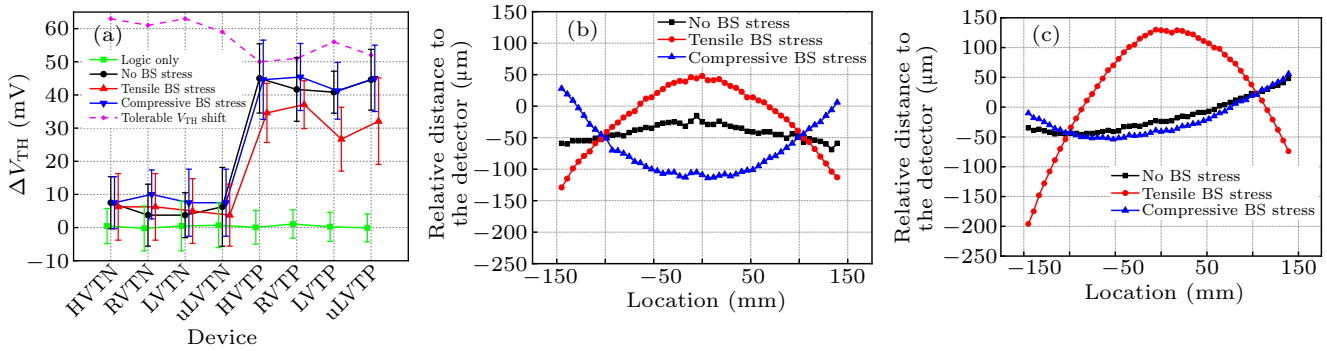


Fig. 2. (a) The V_{TH} shifts due to MRAM integration under different conditions. Logic-only wafer (W/O MRAM integration) was used as the control. ΔV_{TH} was calculated by the absolute V_{TH} value difference between the final test and the pre-MRAM loop. A positive value of ΔV_{TH} means an increase in V_{TH}, and a negative value means that V_{TH} decreases. Four types of n-MOSFET and p-MOSFET can be referred to the methodology section. The dashed line indicates the tolerable V_{TH} shift range, meaning that the chip function might not be guaranteed if there are values beyond this. Wafer configuration before (b) and after (c) MTJ deposition and annealing. The value was calculated by the distance difference between the experimental wafer and the bare Si wafer to the detector.

To investigate the underlying failure mode, the research started with correlating the wafer stress with V_{TH}. As shown in Figs. 2(b) and 2(c), the MRAM deposition and annealing process tended to pull the wafer to a tensile configuration, which was further worsened by BS compressive stress. Conversely, the BS tensile stress tended to bend the wafer into a compressive configuration. The configuration trend caused by BS stress matched well with the shift trend of the p-MOSFET V_{TH}, indicating the close association between the V_{TH} deterioration of p-MOSFET and the wafer configuration.

Before delving further into understanding the underlying mechanism, efforts were made to investigate whether channel mobility was affected by the MRAM integration. I_{Dlin} was measured under different over drive (V_{DD}–V_{TH}). As shown in Fig. 3(a), the slope and intercept were preserved, indicating no carrier mobility degradation resulting from MRAM BEOL. Based on the above conclusions, it was highly considered that the degradation of p-MOSFET resulted from the interfacial charge enhanced by stress.[20–22] V_{TH} did not change too much, even with the BS compressive stress being applied (refer to Fig. 2(a)), suggesting that the interfacial charge was saturated. Subsequently, the assumed failure mechanism of p-MOSFET was verified by CV measurement. Figure 3(b) shows the CV curves under different conditions. Compared with logic-only wafer, the flat-band voltage shifted towards negative bias for 50 mV in the control group (no BS stress) provided that the C_{min} remained nearly the same. When comparing the curve between the control group (no BS stress) and the experimental group (with BS tensile stress), the curve of the experimental wafer shifted towards positive bias for 10 mV, demonstrating that the positive charges generated by Si–H bond breaking were restrained.[23,24]

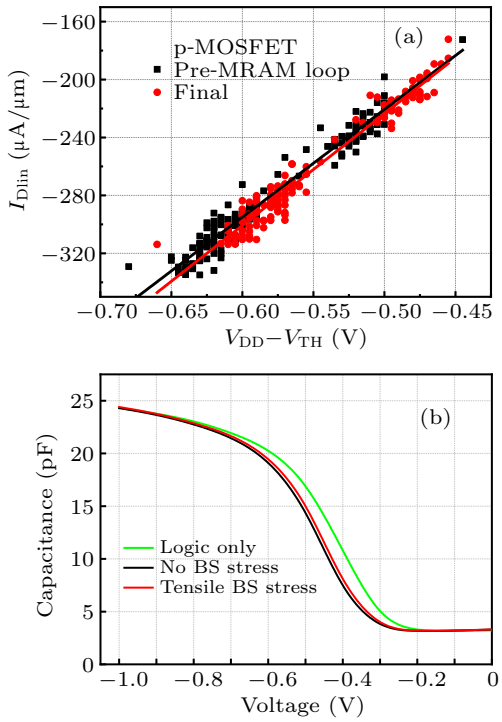


Fig. 3. (a) The I_{Dlin} versus V_{DD}–V_{TH} curves of p-MOSFET, electrical characteristic parameters were evaluated at the pre-MRAM loop and the final stage; and (b) capacitance–voltage curves under different wafer conditions. Positive curve shift means less interfacial positive charge generated during the BEOL process.

The V_{TH} shifts obtained due to backside material being removed are shown in Fig. 4(a). The conclusion could be drawn that the effect of backside stress was memorized and was irreversible. The observed tendency was independent of the type of device used in the experiments. Moreover, to check whether the V_{TH} shift could be remedied by later stress engineering, the BS tensile material was deposited, not immediately before the MRAM loop, but after the final MOSFET test followed by another MOSFET test to quantify the difference. The V_{TH} did not recover at all (as shown in Fig. 4(b)) despite the overall tensile stress being released (as shown in Fig. 4(c)). This phenomenon further confirmed that the deterioration of pMOSFET could be attributed to chemical bond breakage, particularly Si–H bond breakage. It could not be simply remedied by physical stress alone, highlighting the future research interest in addressing the broken bond chemically.

Post H_2 annealing is commonly used to repair the Si–H breakage,[7–10] but additional thermal budget and H atoms are detrimental to MTJ performance.[11–14] The effective H_c of free layer was measured to quantify the effect of H_2 annealing and BS stress. The H_c values pre and post H_2 annealing and other BS stress condition wafers were measured. As shown in Figs. 5(a) and 5(b), a notable H_c drop was observed when H_2 annealing was applied, while no significant H_c degradation was detected on the BS stressed wafer. Hence, it was inferred that commonly used post H_2 annealing on MRAM integrated wafer might not be effective when considering the performance of MTJ. Meanwhile, we tried to find out if TMR, another key device parameter in MTJ, changes due to BS SiN deposition. As shown in Fig. 5(c), there is no significant TMR change when BS stress is applied.

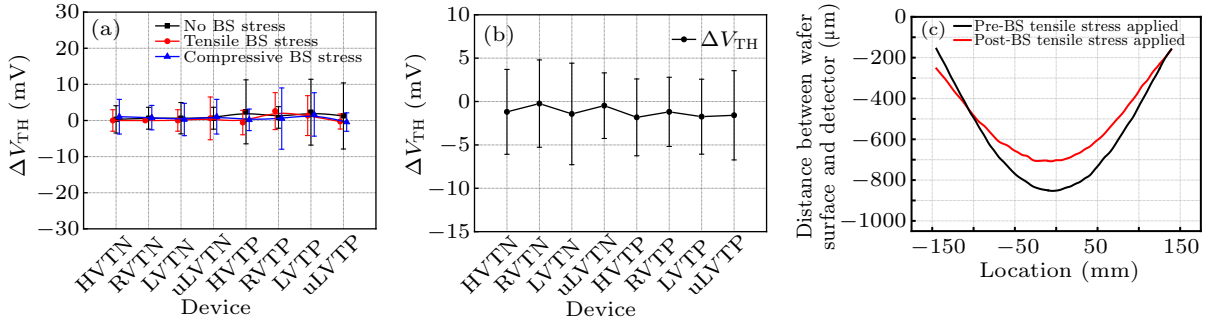


Fig. 4. (a) The ΔV_{TH} due to BS material removal, ΔV_{TH} was calculated by the absolute V_{TH} value difference between post-BS SiN removal and pre-BS SiN removal, four types of n-MOSFET and p-MOSFET can be referred to Section 2; (b) ΔV_{TH} due to BS stress applied at the final test step, ΔV_{TH} was calculated by the absolute V_{TH} value difference between post-BS stress applied and pre-BS stress applied at the final MOSFET test step, four types of n-MOSFET and p-MOSFET can be referred to Section 2; and (c) wafer configuration before and after BS stress applied at the final MOSFET test step. The value was calculated by the distance difference between the experimental wafer and the bare Si wafer to the detector.

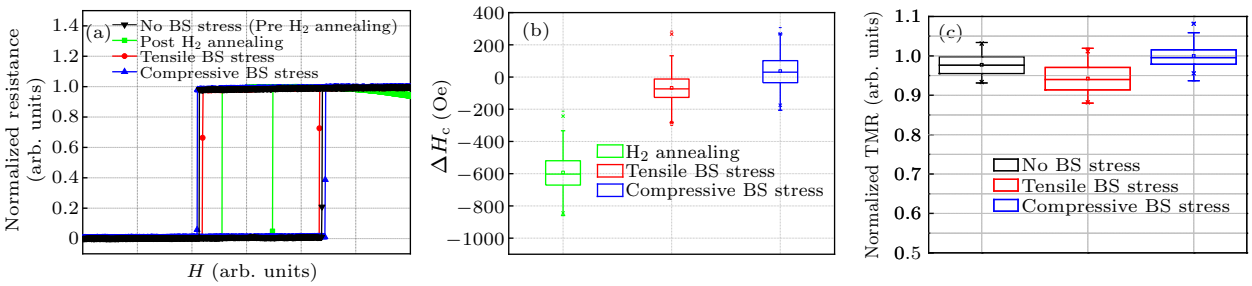


Fig. 5. (a) Typical R–H curve of different wafers; (b) H_c shift due to different process conditions and (c) normalized TMR of different process conditions. The value was normalized by the 75% quantile of TMR value of no BS stress condition.

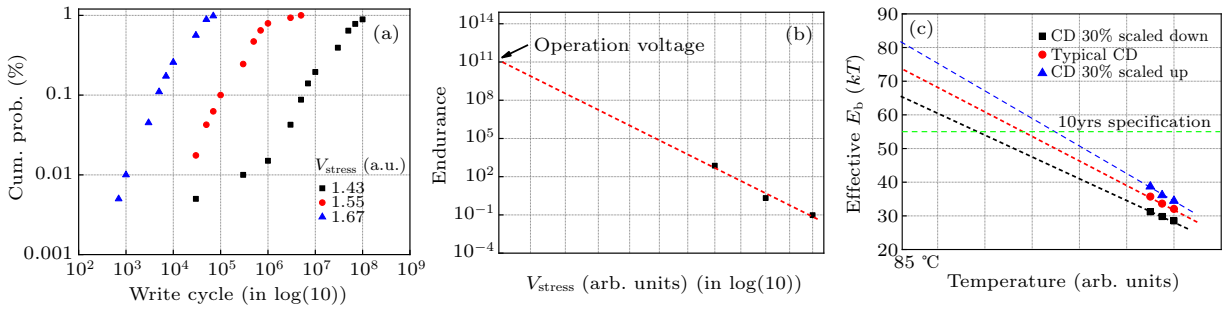


Fig. 6. (a) Weibull plot for MTJ with typical critical dimension (CD), (b) endurance cycle as a function of 20 ns voltage pulse fitted by power law and (c) effective energy barrier of MTJ with different MTJ sizes, all satisfying the 10 year retention requirement when $T = 85$ °C.

To ensure that MTJ reliability was not impacted by the new approach, the endurance and data retention measurements were conducted. As shown in Figs. 6(a) and 6(b), using the power-law model, endurance was extrapolated to be $> 10^{10}$ cycles at the write operation condition (shown in Fig. 6(b)). Furthermore, the data retention could extend beyond 10 years at 85 °C, despite scaling down the MTJ size by 30% (shown in Fig. 6(c)). Both the competitive endurance and data retention results confirmed the possibility of obtaining the desired MTJ performance when utilizing BS tensile stress.

4. Conclusion and perspectives

In this study, a method to ease the p-MOSFET V_{TH} deterioration was proposed. BS tensile stress was found to mitigate the V_{TH} shift, while BS compressive stress might worsen or not contribute anything to the V_{TH} shift, depending on whether the Si–H bond could be further broken. The failure model was verified to be interfacial positive charge, as evidenced by the shift of the capacitance–voltage curve towards the positive direction when the BS tensile stress was applied. In addition, it was concluded that this method could not be reversed, and the failure could not be recovered simply by means of post BS stress repair upon the breaking of Si–H bond. This method does not contribute anything to the thermal budget and is useful when the thermal budget is considered, such as eMRAM application. The performance and reliability of the MTJ device proved competitive when implementing this new method.

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