

Recent progress on ambipolar 2D semiconductors in emergent reconfigurable electronics and optoelectronics

Yuehao Zhao(赵月豪), Haoran Sun(孙浩然), Zhe Sheng(盛喆), David Wei Zhang(张卫), Peng Zhou(周鹏), and Zengxing Zhang(张增星)

Citation: Chin. Phys. B, 2023, 32 (**12**): 128505. DOI: 10.1088/1674-1056/ad08a5
Journal homepage: http://cpb.iphy.ac.cn; http://iopscience.iop.org/cpb

What follows is a list of articles you may be interested in

Ultra-high photoresponsive photodetector based on ReS_2/SnS_2 heterostructure

Binghui Wang(王冰辉), Yanhui Xing(邢艳辉), Shengyuan Dong(董晟园), Jiahao Li(李嘉豪), Jun Han(韩军), Huayao Tu(涂华垚), Ting Lei(雷挺), Wenxin He(贺雯馨), Baoshun Zhang(张宝顺), and Zhongming Zeng(曾中明)
Chin. Phys. B, 2023, 32 (**9**): 098504. DOI: 10.1088/1674-1056/acd9c0

Graphene-based heterojunction for enhanced photodetectors

Haiting Yao(姚海婷), Xin Guo(郭鑫), Aida Bao(鲍爱达), Haiyang Mao(毛海央),Youchun Ma(马游春), and Xuechao Li(李学超)
Chin. Phys. B, 2022, 31 (**3**): 038501. DOI: 10.1088/1674-1056/ac1b8b

A field-effect WSe_2/Si heterojunction diode

Rui Yu(余睿), Zhe Sheng(盛喆), Wennan Hu(胡文楠), Yue Wang(王越), Jianguo Dong(董建国), Haoran Sun(孙浩然), Zengguang Cheng(程增光), and Zengxing Zhang(张增星)
Chin. Phys. B, 2023, 32 (**1**): 018505. DOI: 10.1088/1674-1056/ac9049

A double quantum dot defined by top gates in a single crystalline InSb nanosheet

Yuanjie Chen(陈元杰), Shaoyun Huang(黄少云), Jingwei Mu(慕经纬), Dong Pan(潘东), Jianhua Zhao(赵建华), and Hong-Qi Xu(徐洪起)
Chin. Phys. B, 2021, 30 (**12**): 128501. DOI: 10.1088/1674-1056/abff2e

Effect of electrical contact on performance of WSe_2 field effect transistors

Yi-Di Pang(庞奕荻), En-Xiu Wu(武恩秀), Zhi-Hao Xu(徐志昊), Xiao-Dong Hu(胡晓东), Sen Wu(吴森), Lin-Yan Xu(徐临燕), and Jing Liu(刘晶)
Chin. Phys. B, 2021, 30 (**6**): 068501. DOI: 10.1088/1674-1056/abd752

TOPICAL REVIEW — Post-Moore era: Materials and device physics

Recent progress on ambipolar 2D semiconductors in emergent reconfigurable electronics and optoelectronics

Yuehao Zhao(赵月豪)[1,†], Haoran Sun(孙浩然)[1,†], Zhe Sheng(盛喆)[1,3,†], David Wei Zhang(张卫)[1,2], Peng Zhou(周鹏)[1,2,‡], and Zengxing Zhang(张增星)[1,2,§]

[1] *School of Microelectronics, Fudan University, Shanghai* 200433, *China*
[2] *National Integrated Circuit Innovation Center, Shanghai* 201203, *China*
[3] *School of Information Science and Technology, Hangzhou Normal University, Hangzhou* 311121, *China*

(Received 31 July 2023; revised manuscript received 21 October 2023; accepted manuscript online 2 November 2023)

In these days, the increasing massive data are being produced and demanded to be processed with the rapid growth of information technology. It is difficult to rely solely on the shrinking of semiconductor devices and scale-up of the integrated circuits (ICs) again in the foreseeable future. Exploring new materials, new-principle semiconductor devices and new computing architectures is becoming an urgent topic in this field. Ambipolar two-dimensional (2D) semiconductors, possessing excellent electrostatic field controllability and flexibly modulated major charge carriers, offer a possibility to construct reconfigurable devices and enable the ICs with new functions, showing great potential in computing capacity, energy efficiency, time delay and cost. This review focuses on the recent significant advancements in reconfigurable electronic and optoelectronic devices of ambipolar 2D semiconductors, and demonstrates their potential approach towards ICs, like reconfigurable circuits and neuromorphic chips. It is expected to help readers understand the device design principle of ambipolar 2D semiconductors, and push forward exploring more new-principle devices and new-architecture computing circuits, and even their product applications.

Keywords: two-dimensional material, ambipolar semiconductor, semiconductor device

PACS: 85.60.Dw, 73.40.Lq, 85.30.Tv, 81.16.–c **DOI:** 10.1088/1674-1056/ad08a5

1. Introduction

Over the past few decades, integrated circuits (ICs) have experienced rapid growth following Moore's Law.[1] As the semiconductor device size continues to shrink, the scale of ICs continues to increase from large-scale integration to the current very large-scale integration, driving the informationization of human society. However, the characteristic dimension of transistors is approaching the physical limits, which will bring inevitable challenges such as short-channel effects, quantum tunneling effects, and thermal carrier effects.[2–4] In the foreseeable future, the improvement of the computing capacity and energy efficiency will be difficult to rely solely on the shrinking gain. On the other hand, the rapid advancement of information technology, like artificial intelligence and big data technologies are being increasingly applied in various fields,[5–8] which demand increasing tough requirements on the computing capacity, energy efficiency, time delay and cost. The traditional von Neumann architecture has shown limitations in handling these highly complex and data-intensive tasks.[9] This is primarily due to the separation of its computational and storage functions,[10–12] leading to the so-called memory wall problem.[13,14] Therefore, it is urgent to explore new materials, new-principle devices and new computing architectures to break the limitations of Moore's Law and the von Neumann bottleneck, holding the potential to drive a new wave of industrial revolution.[4]

Recently, two-dimensional (2D) semiconductor materials have gained intensive attention due to their unique physical and chemical properties.[15–17] 2D semiconductor materials possess an ultrathin thickness and exhibit excellent electrical, optical, and mechanical properties.[18–25] Utilizing such ultrathin 2D materials as the channel in transistors enables a possibility of the high performance retention with the device size continuing to shrink. Therefore, they are considered as one of the most important candidates to overcome the size reduction bottleneck of transistors and have a wide range of applications in emerging electronic and optoelectronic devices.[26–32] Among various 2D materials, ambipolar 2D semiconductors are of ambipolar transport characteristics under gate voltage control with the major charge carriers flexibly modulated between electrons and holes at demanded concentrations. They have the ability to rapidly, dynamically, and reversibly tune the dominant carrier type through electric fields. This unique property allows for the design and fabrication of new-principle devices like reconfigurable devices, offering the capability to program electronic and optoelectronic circuits according to specific requirements and providing exciting functionali-

[†]These authors contributed equally to this work.
[‡]Corresponding author. E-mail: pengzhou@fudan.edu.cn
[§]Corresponding author. E-mail: zhangzx@fudan.edu.cn

© 2023 Chinese Physical Society and IOP Publishing Ltd

ties for future semiconductor products.[33] Compared to mainstream reconfigurable circuits like field-programmable gate arrays (FPGA), reconfigurable circuits based on ambipolar 2D semiconductors enable the possibility of reconfiguring circuits at the device levels. So far, the significance of ambipolar 2D semiconductors has been recognized with lots of significant advancements, and a few specialized reviews have been composed in this field.[34–37] Here we dedicate an overview on the recent progress of ambipolar 2D semiconductors applied in reconfigurable devices and circuits. We hope the review will help readers to well understand the applications of ambipolar 2D semiconductors, and push forward exploring new-principle devices and new-architecture computing circuits, and even their product applications.

2. Ambipolar 2D semiconductors

Ambipolar semiconductors refer to the ones that the charge carriers can be reversibly and flexibly modulated, including the major carrier type and concentration.[15] Generally, the conduction in semiconductors primarily relies on electrons and holes. Intrinsic semiconductors typically exhibit low carrier concentration and poor conductivity. The concentration of electrons or holes is often augmented through doping high-valent or low-valent chemical elements, which is dominant in current industrial electronic and optoelectronic applications. For 2D semiconductors, there have a variety of strategies to complete p-/n-type modulation,[38] such as intrinsic defect tailoring,[39,40] substitutional doping,[41] surface charge transfer,[42,43] chemical intercalation,[44] electrostatic field modulation,[45,46] dielectric interface engineering,[47,48] annealing,[32] and so on. Taking electrostatic field modulation as an example, when a positive gate voltage is applied, according to the working principle of a capacitor, negative charges (electrons) will accumulate in the 2D semiconductor channel layer, resulting in an n-type behavior of transistors, as shown in Fig. 1(a). Conversely, when a negative gate voltage is applied, the accumulation of positive charges (holes) in the channel layer leads to a p-type behavior of transistors, as shown in Fig. 1(b). As a result, the transfer characteristics of field-effect transistors (FETs) present V-shaped curves, as shown in that of graphene, black phosphorus (BP) and WSe_2 FETs (Figs. 1(c)–1(h)).[35]

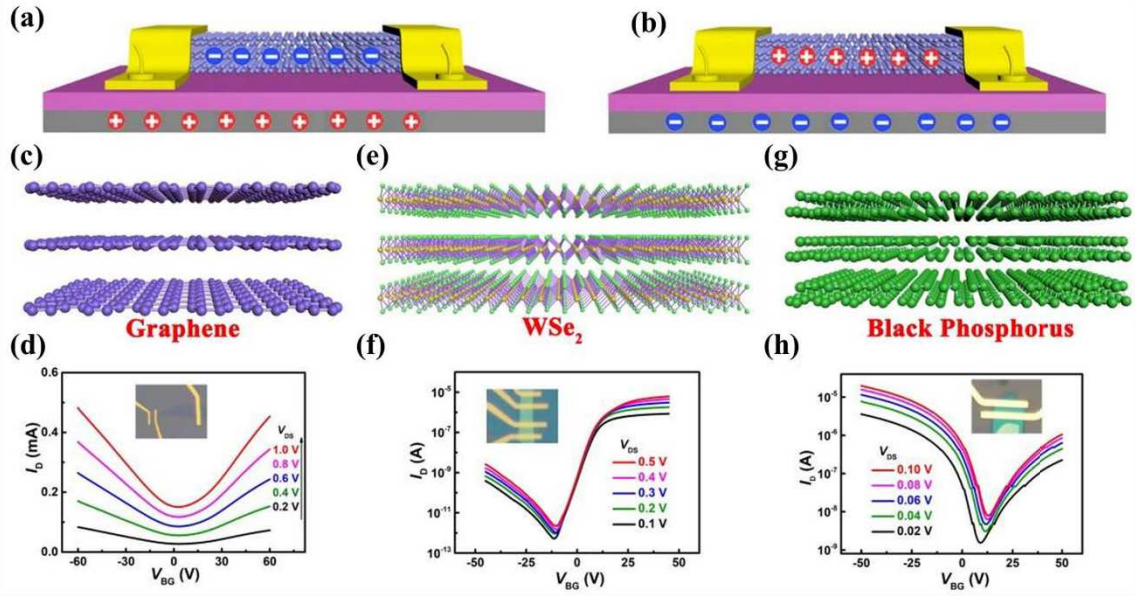


Fig. 1. Ambipolar 2D crystals can be flexibly tuned by external electrical fields between (a) n-type and (b) p-type. Panels (c), (e) and (g) are the schematic crystal structures of typical ambipolar 2D crystals of few-layer graphene, WSe_2 and black phosphorus (BP). Panels (d), (f) and (h) are the transfer characteristic curves of the corresponding FETs. All figures are from Ref. [35].

Although there are diverse methods for p-/n-type modulation in semiconductors, achieving dynamic regulation between p-type and n-type is challenging. For example, with Nb dopant, MoS_2 performs a p-type behavior,[49] while Re makes it as an n-type semiconductor.[50] The p-type of WSe_2 can be obtained with Au dopant,[51] and Sn-doped WS_2 exhibits n-type property.[52] These chemical dopants are non-volatile. Once the doping happens and the devices are packaged, it is difficult to modulate the major charge carriers again.[53] Strain can also affect the electrical properties of 2D semiconductors.[54] Similarly, after devices are packaged, it is difficult to modulate them again at the device level. The ultra-thin characteristics of 2D materials make them vulnerable to external field regulation, which in turn enables the modification of their carrier doping concentration and polarity relatively easily.[55] This capability is expected to be utilized in the design and fabrication of new device structures and even to generate novel functionalities for the improvement and enhancement of traditional semiconductors. In this paper, we mainly focus on the ambipolar semiconductors that are driven by such an electrostatic field.

Graphene is a 2D material composed of carbon

atoms,[56,57] which is the first widely studied ambipolar 2D material. So far, ambipolar behavior has been found in a variety of 2D materials, mainly in elemental materials and metal chalcogenide 2D semiconductors,[15] including elemental semiconductors like graphene,[57] phosphorene (BP),[58] silicene,[59] germanane,[60] tellurene,[61] and black arsenic;[62] metal disulfide 2D semiconductors like MoS_2,[63,64] WS_2,[65,66] ReS_2,[67,68] and SnS_2;[69] metal diselenide 2D semiconductors like $MoSe_2$,[70,71] WSe_2,[72–74] $ReSe_2$,[67] $PtSe_2$,[75,76] and $PdSe_2$;[77–79] metal ditelluride 2D semiconductors like $MoTe_2$,[80,81] and WTe_2;[82,83] ternary and other chalcogenide 2D semiconductors like $Mo(Se_{1-x}Te_x)_2$,[84] $W(Se_{1-x}Te_x)_2$,[85] SnSe,[86] SnS,[87] InSe,[88] InSb,[89] Cr_2S_3,[90] Nb_2SiTe_4,[91] and $(Bi_xSb_{1-x})Te_3$.[92] In addition to the aforementioned inorganic 2D materials, some organic 2D materials also exhibit similar properties.[34]

3. Ambipolar 2D semiconductors for reconfigurable electronics

Under the modulation of external electric field, ambipolar 2D crystals exhibit tunable transport behavior of charge carriers. As a result, it is possible to develop electrostatically tunable and reconfigurable devices through specific device structure designs, like ambipolar field-effect transistors/memories[93–95] and gate-tunable p–n junctions/Schottky junctions.[96,97] These devices are of various novel electronic functions for rectification and logic operations. Such reconfigurable devices enrich the application scenarios of circuits and demonstrate significant potential in achieving multi-purpose integration of circuits, reducing transistor redundancy, simplifying circuit design, and enhancing integrated circuit performance.[30,53]

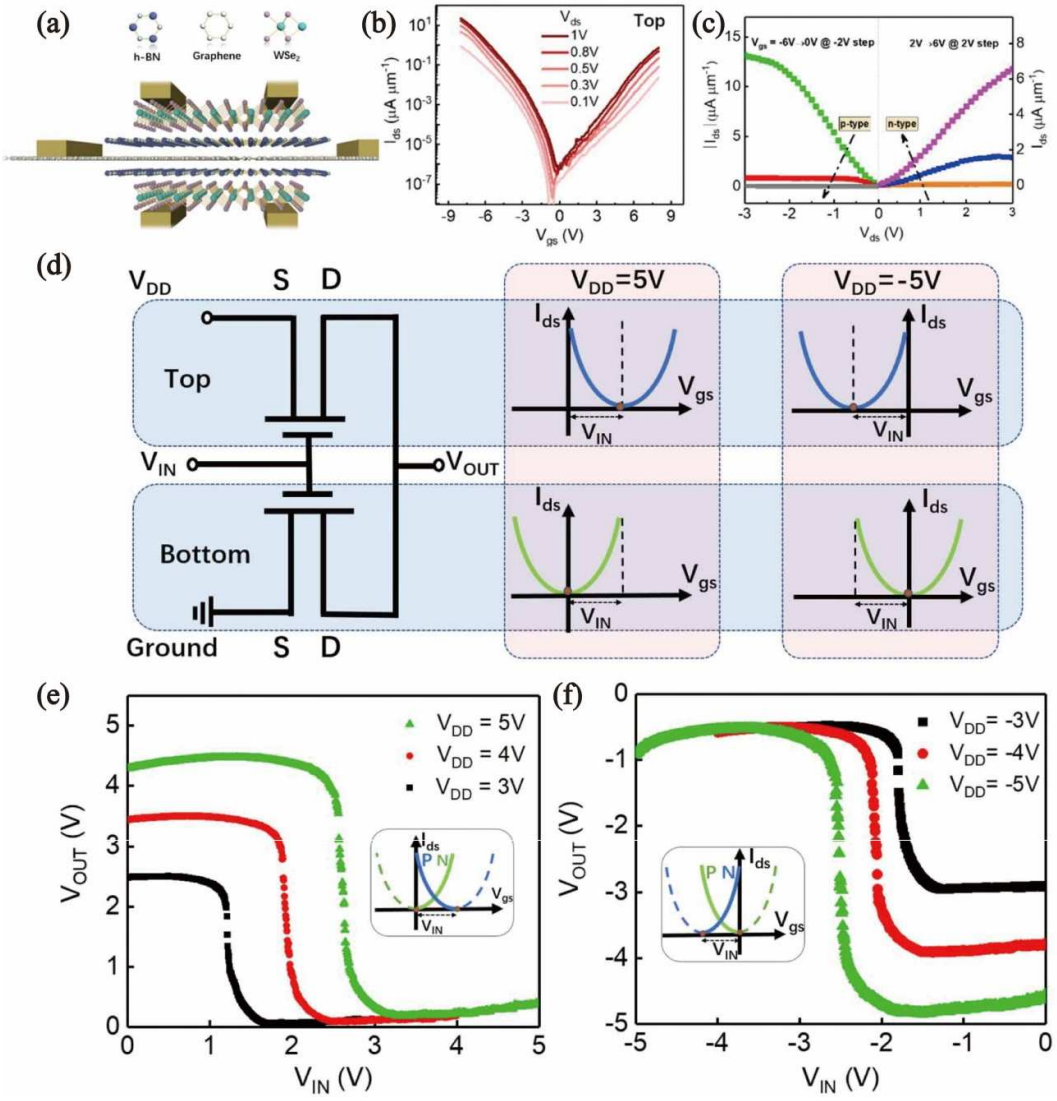


Fig. 2. (a) Schematic of ambipolar 2D WSe_2 CFET device. (b) Transfer characteristic curves of the top WSe_2 transistor. (c) Output characteristic curves of the top WSe_2 transistor. (d) Equivalent circuit diagram of the inverter based on the CFET with series-connected vertical stacked transistors. (e) and (f) V_{OUT}–V_{IN} curves of the ambipolar WSe_2 CFET inverter working in the first and third quadrants. All figures are from Ref. [98].

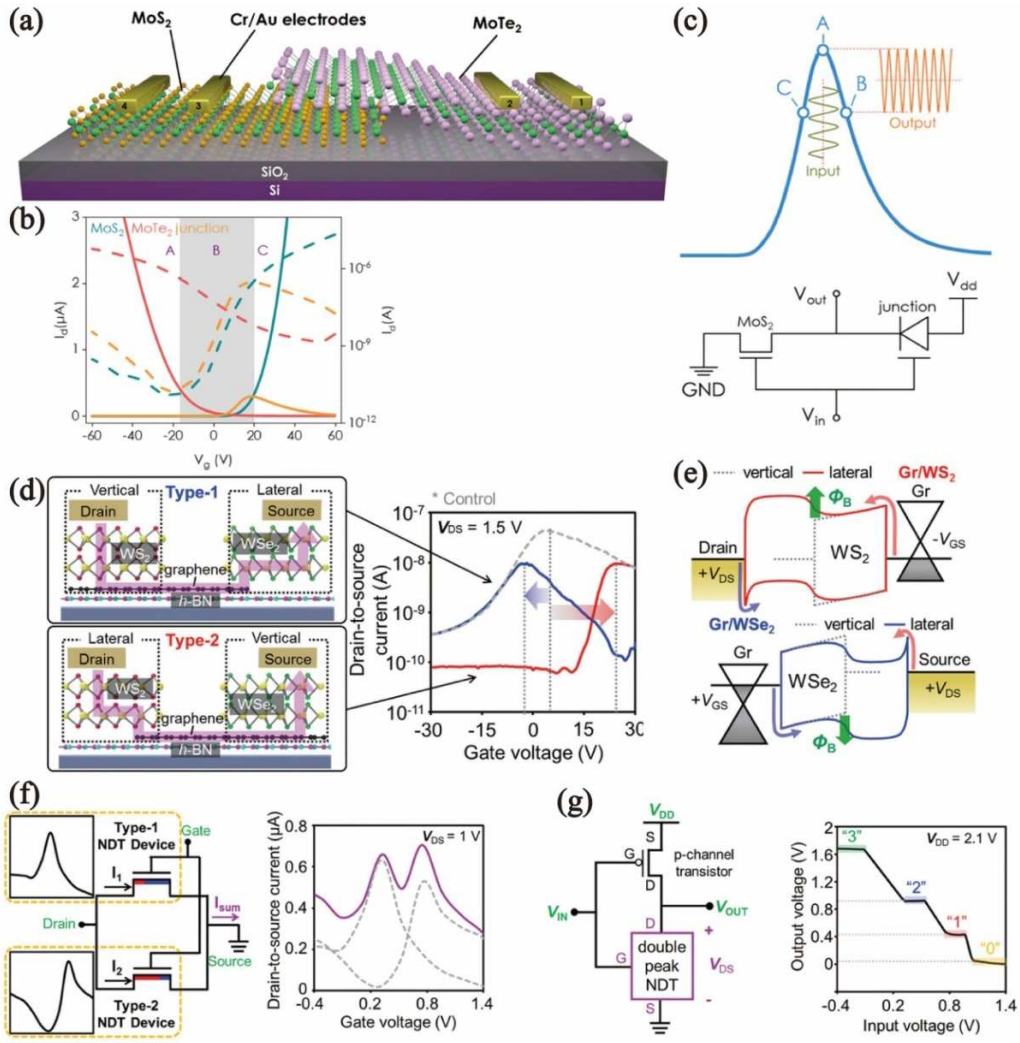


Fig. 3. (a) Schematic of the $MoTe_2/MoS_2$ heterojunction device. (b) Transfer characteristic curves of the $MoTe_2$ FET, MoS_2 FET, and $MoTe_2/MoS_2$ heterojunction devices. (c) Principle of the anti-ambipolar frequency multiplier and schematic diagram of the multiplier circuit. (d) Schematic diagram of a type-1 device composed of a WS_2–graphene vertical junction and a graphene–WSe_2 lateral junction (top figure) and a type-2 device composed of a WS_2–graphene lateral junction and a graphene–WSe_2 vertical junction (bottom figure). The panel also shows the I_D–V_G characteristic curves. (e) Band structure of the drain-WS_2–graphene (top) and graphene–WSe_2-source (bottom). (f) Schematic diagram illustrating the implementation strategy of a dual-peak NDT device and its I_D–V_G characteristics curve. (g) Circuit structure and voltage transfer characteristics of quaternary inverter. Panels (a)–(c) are from Ref. [101], and panels (d)–(g) are from Ref. [102].

3.1. Ambipolar 2D semiconductors based field-effect transistors

An ambipolar FET is of similar device configuration to traditional FETs, including source/drain/gate electrodes, channel and dielectric layers, as in Fig. 1. Different from unipolar FETs, the major charge carrier type in the channel can be regulated by an external electric field, allowing the device dominated by electrons or holes following the gate to be applied with positive or negative voltages. They thus exhibit V-shaped transfer curves (Fig. 1). Such characteristics can be explored for novel applications different from unipolar FETs.[99,100] For example, Hu *et al.*[98] proposed a complementary field-effect transistor (CFET) based on ambipolar FETs by employing the idea of transitioning from planar to vertical stacking, as illustrated in Fig. 2(a). In such a device, the graphene acts as an internal common gate, and the top and bottom are composed of two independent ambipolar FETs. Due to the good holes and electrons injection, the transistors at the top and bottom have similar ambipolar characteristics (Figs. 2(b) and 2(c)). By assigning the polarity and amplitude by V_{DD} and V_{IN}, the operations of the n-channel and p-channel between the two transistors are interchangeable (Fig. 2(d)). This allows for the CFET to function as an inverter working in both the first and third quadrants (Figs. 2(e) and 2(f)). This switchable characteristic should be applicable for large voltage swing circuits by using only two such inverters with the advantages on simplifying the circuits and lowering consumption of electronic units like transistors, which commonly need bulky negative-voltage components in conventional design.[98]

In addition to the V-shaped transfer characteristics, researchers have also developed an inverted V-shaped transfer curve (anti-ambipolar behavior) based on ambipolar 2D semiconductors. This anti-ambipolar characteristic allows for the realization of complex electronic functionalities through a sin-

gle device, greatly simplifying circuit design and manufacturing processes. Anti-ambipolar devices can be used for multi-value logic inverters and frequency doubling circuits.[103–105] As shown in Fig. 3(a), the $MoTe_2/MoS_2$ PN heterojunction exhibits pronounced anti-ambipolar characteristics.[101] Figure 3(b) illustrates the mechanism behind the anti-ambipolar *I*–*V* curves, showing the transfer characteristics of $MoTe_2$ FET (red line), MoS_2 FET (blue line), and the heterojunction (orange line). This anti-ambipolar characteristic can be understood as the junction being formed by the series connection of a p-type ($MoTe_2$) FET and an n-type (MoS_2) FET. Therefore, when both FETs are turned on at around $V_G = +20$ V, the total current reaches its maximum value. Figure 3(c) illustrates the principle of a frequency multiplier based on the anti-ambipolar curve. An input sinusoidal signal oscillates between points A, B, and C marked on the anti-ambipolar curve, resulting in an output signal with a frequency twice than that of the input signal, reaching a maximum of 3 kHz. By utilizing the FETs based on BP devices, the maximum frequency multiplication can be further extended to 128 kHz.[96]

The anti-ambipolar behavior can also perform negative differential transconductance (NDT). Figure 3(d) displays the schematics of two types of NDT devices.[102] Combining two NDT devices with peak currents located at different positions yields a dual-peak NDT device (Fig. 3(f)). The band structure of the drain-WS_2–graphene and graphene–WSe_2-source junction is shown in Fig. 3(e). By combining the dual-peak NDT device with a p-channel transistor in series, a quaternary inverter circuit is formed (Fig. 3(g)).

3.2. Ambipolar 2D semiconductors for reconfigurable rectification circuits

The p–n junction is one of the most fundamental and essential structure in semiconductors, widely used in rectifier circuits. The carrier types of ambipolar 2D crystals can be flexibly controlled with the electric field. Thus, a homogeneous p–n junction can be formed in a channel through local electric field modulation. This p–n junction can be reconfigured to other junction states by varying the electric field, enabling it with programmable ability. Researchers have developed various reconfigurable p–n junction structures, such as horizontal split gates,[106–108] heterojunctions,[97] semi-floating gate structures,[29] and ferroelectric gate structures.[109–111]

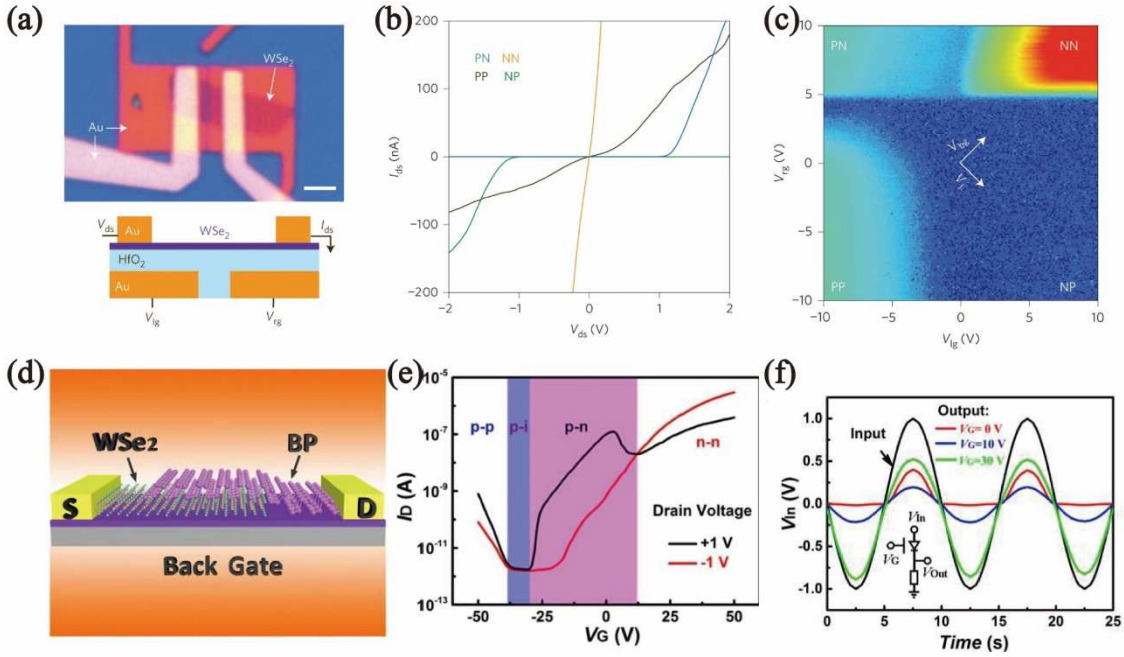


Fig. 4. (a) Optical image and schematic of a split-gate FET for p–n junction. (b) I_{ds}–V_{ds} curves of the device at different split-gate control configurations. (c) Current magnitude $|I_{ds}|$ through the device when the drain–source bias V_{DS} is maintained while the two back gates vary independently. (d) Schematic of a reconfigurable p–n junction device based on an ambipolar BP/WSe_2 heterojunction FET. (e) Transfer characteristic curves. (f) Performance of the device as a reconfigurable rectifier circuit. Panels (a)–(c) are from Ref. [106], and panels (d)–(f) are from Ref. [97].

In 2014, researchers fabricated p–n homojunction devices based on a parallel split-gate device structure and ambipolar 2D WSe_2.[106–108] These devices exhibit switchable rectification characteristics, as shown in Figs. 4(a) and 4(b). The discrete dual-gate structure divides an ambipolar channel into two regions where the electric field acts independently. This allows for localized electric field doping within the same channel material, enabling the device to operate flexibly in four different states: p–n junction, n–p junction, n–n junction, and p–p junction, as shown in Fig. 4(c). Li *et al.*[97] fabricated a heterojunction FET based on ambipolar BP and WSe_2 (Fig. 4(d)), which can undergo transitions between p–p junction, p–i junction, p–n junction, and n–n junction states through a control gate (Fig. 4(e)). Based on the reconfiguration of the rectifi-

cation states, they proposed that the device can be developed for programmable (reconfigurable) rectifier circuits (Fig. 4(f)). By controlling the gate voltage, the circuit can process alternating current (AC) signals to be rectified or non-rectified, which may enable rectification circuits with programmable (computing) ability.[97]

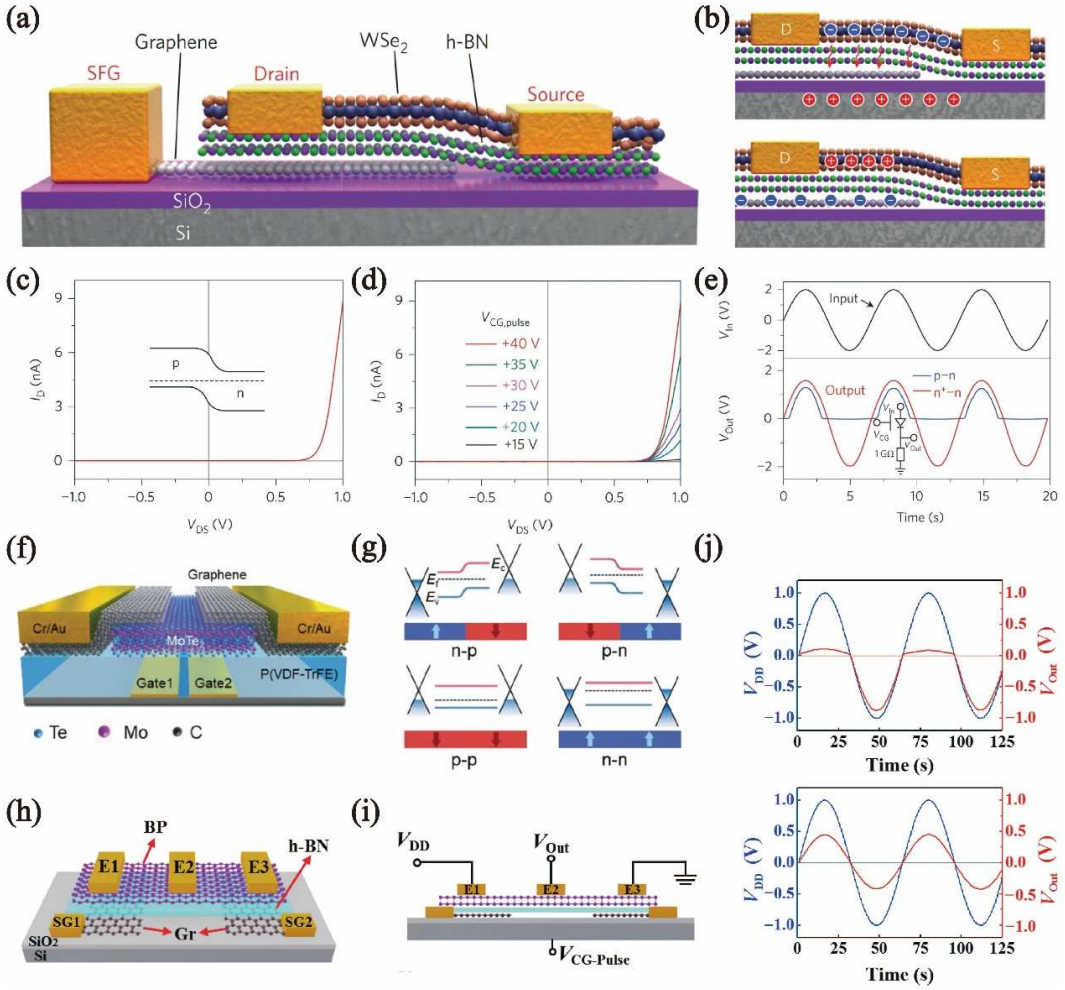


Fig. 5. (a) Reconfigurable p–n junction device based on a semi-floating gate field-effect transistor. (b) Working mechanism of the device under positive control gate pulse voltage modulation. (c) I_D–V_{DS} curve across the WSe_2 with a +40 V pulse on the Si. (d) Output curves under positive control gate pulse voltage. (e) Filtering characteristics of the device in different rectification states, with a schematic diagram of the rectification circuit. (f) Reconfigurable p–n junction device based on a ferroelectric parallel dual-gate FET. (g) Schematic diagram illustrating the principle. (h) BP/h-BN/graphene heterojunction with a semi-gate device. (i) Design schematic of the reconfigurable rectifier circuit. (j) Rectification results of a sine wave signal after negative gate voltage pulse (top image) and positive gate voltage pulse (bottom image). Panels (a)–(e) are from Ref. [29], panels (f)–(g) are from Ref. [111], and panels (h)–(j) are from Ref. [28].

The devices mentioned above require continuous gate voltages to maintain them in various reconfigurable states, leading to a significant energy cost. Floating gate and ferroelectric gate can address this drawback since they are of memory capability. Figure 5(a) illustrates the structure of a WSe_2/h-BN/graphene-based semi-floating gate field-effect transistor device.[29] When a positive voltage is applied to the silicon control gate, electrons accumulate in the WSe_2 channel due to the field effect. Simultaneously, under the influence of the electric field, these electrons tunnel through the barrier layer and reach the semi-floating gate. Once the control gate voltage disappears, these electrons are stored in the semi-floating gate layer, leading to p-doping of the channel layer in the aligned WSe_2 (Figs. 5(c) and 5(d)), thus exhibiting p–n junction behavior since WSe_2 is intrinsically n-type (Fig. 5(b)). Under negative control gate voltage pulse, the stored holes in the semi-floating gate will dope the aligned WSe_2 with electrons, causing WSe_2 to behave as n^+–n junction. This enables the formation of non-volatile p–n junction and n^+–n junction in the WSe_2 channel, which can be utilized to develop reconfigurable logic rectifier devices and enrich the rectifier circuits with computing and memory ability (Fig. 5(e)). The memory function has been also achieved by controlling the polarity of ferroelectric materials. Figure 5(f) illustrates the schematic diagram of a reconfigurable p–n junction device based on a ferroelectric parallel split-gate structure, where ferroelectric P(VDF-TrFE) film acts as the dielectric.[111] In the upward polarization state, electrons accumulate in neighboring $MoTe_2$ channel, thereby inducing n-type doping. In the downward polarization state, the channel

is p-type doping. By modulating the polarization direction of P(VDF-TrFE) in different regions, the working states of n–p junction, p–n junction, p–p junction and n–n junction can be obtained in the device. These reconfigurable states can be maintained for a long time, which means low power consumption.

For reconfigurable rectification circuits based on programmable p–n junctions, the circuits often employ one resistor as the load (Fig. 5(e)). This is not good for voltage output and circuits fabrication. To address such problem, Sheng *et al.* proposed a complementary gate-programmable p–n junctions design, which includes two back-to-back semi-gate devices (Fig. 5(h)), where the BP serves as the channel and two graphene flakes are the two semi-gates. To control the voltages on the semi-gates, the back-to-back devices can perform n–p junction and p–n junction, respectively. While AC signals input, one device favors the transportation of a certain direction of ACs, and another one blocks the transportation, which is of similar designing principle to CMOS circuits and should be of advantage on output impedance and static power consumption. If using the two semi-gates as semi-floating gates, the circuits will possess memory ability and become two back-to-back programmable p–n junction memories (Fig. 5(i)). They find that the reconfiguration speed of the circuit can reach 25 μs, and it can handle reconfigurable rectification with a reconfigurable frequency of up to 1 kHz.[28]

3.3. Ambipolar 2D semiconductor for reconfigurable logic gates

As essential building blocks to perform logic operations for the data processing, logic gates play a crucial role in modern computer science. The emergence of ambipolar semiconductor devices opens up new possibilities for the future logic gates. Logic gates based on ambipolar semiconductor devices can integrate multiple logic functions by flexibly tuning the polarity of ambipolar 2D semiconductors. This property demonstrates great adaptability to different scenarios with high performance and area-efficiency. In contrast, the functionality and performance of traditional logic gates are constrained due to the limited characteristics of unipolar MOSFET. In addition, such reconfigurable feature makes it more competitive to identify specific functionality of logic gates, which signifies that they can be employed to construct secure electronic systems to provide the encryption of chip.[112]

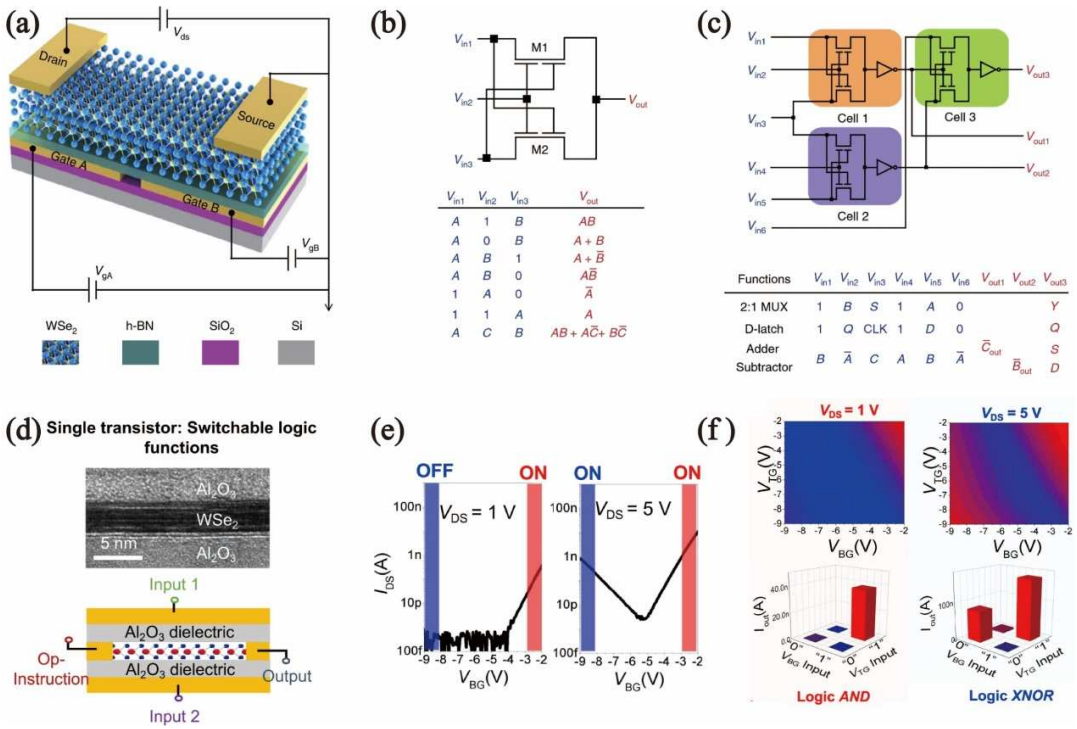


Fig. 6. (a) Schematic of an electrically tunable homojunction (ETH) device based on parallel dual-gate structure. (b) Schematic of the reconfigurable logic gate and corresponding logic functions realized by the connection of two ETH devices. (c) Circuit diagram to obtain reconfigurable microprocessor unit functions based on the connection of six ETH devices. (d) Schematic diagram of a small footprint device based on vertical dual-gate structure. The top and bottom gates serve as logic input 1 and input 2, current in device serves as logic output. (e) Transfer characteristics curves of the device via the voltage control of drain terminal. (f) Logic behaviors at V_{DS} of 1 V and 5 V, respectively, which show logic AND and XNOR, respectively. Panels (a)–(c) are from Ref. [30], and panels (d)–(f) are from Ref. [113].

Ambipolar semiconductor devices with at least two independent gates are indispensable for developing reconfigurable logic gates. Pan *et al.*[30] designed an electrically tunable homojunction (ETH) device based on a parallel dual-gate structure, as shown in Fig. 6(a). In this device, ambipolar WSe_2 is selected as the channel material, and two independent gates, along with drain terminal, collectively control the transportation of the device. When different combinations of gate and

drain voltage are applied, p–n, n–p, n–n, and p–p junctions can be achieved with different working states. This diversifies the field-effect characteristics at a device level, making it possible to develop reconfigurable logic gates. Based on such reconfigurable electrical characteristics, they fabricate a reconfigurable logic gate by serially connecting two ETH devices, see Fig. 6(b). The single logic gate can perform as an invertor, follower, OR logic gate, AND logic gate, etc., when two gates and a drain serve as three input terminals. In comparison, 4 transistors are required for OR or AND logic gate by using silicon-based MOSFETs. Furthermore, they propose a more complex reconfigurable logic gate based on six ETH devices. This configuration enables the realization of logic applications like MUX, D-latch, 1-bit full adder and subtractor for microprocessors (Fig. 6(c)), which can significantly reduce the resource consumption of transistor and hold promising to simplify design of the microprocessors and obtain a higher area-efficiency.

To further take advantage of the performance of 2D materials for reconfigurable logic applications, Zeng *et al.*[113] proposed a reconfigurable logic gate based on a WSe_2 transistor with a vertical dual-gate structure (Fig. 6(d)). WSe_2 is an ambipolar semiconductor whose transport properties rely heavily on the magnitude of V_{DS}. In other words, WSe_2 behaves as an n-type semiconductor at a small V_{DS} while as an ambipolar semiconductor at a large V_{DS}, as shown in Fig. 6(e). This is because a small V_{DS} leads to a slightly thin barrier at the drain terminal, blocking the injection of holes into the channel, even if the gate voltage is negatively biased. However, the hole barrier is dramatically thinned when the drain terminal is applied to a large V_{DS}, thus permitting the injection of holes and allowing WSe_2 to exhibit ambipolar transport behaviors. Based on this, they take the top and bottom gates as two logic inputs, the current in the device as the logic output, and realized AND and XNOR logic functions in this device via the modulation of V_{DS}. Such a reconfigurable logic gate thus can reduce 50% of the area for AND logic, and 87.5% for XNOR logic when compared to silicon-based logic gates, as two transistors are folded into this single device.

In addition to the advantage of area-efficiency, the reconfigurable nature of ambipolar semiconductor devices can be used to develop electronic system with hardware encryption function. Wu *et al.*[112] put forward a reconfigurable field-effect transistor based on a vertical triple-gate structure and ambipolar BP, as shown in Fig. 7(a). This transistor includes a bottom gate, a top gate and a polarity gate, in which the bottom gate and the top gate are shorted. The polarity gate under the drain electrode is designed to suppress undesired carriers from the drain electrode injecting into the channel, while allowing the desired carriers into the channel (see Fig. 7(b)). For $V_{pg} < 0$, it only allows holes injected from the drain electrode, while electrons are suppressed. When $V_g < 0$, the hole injection from the source is also enabled, then the current turns on. When $V_g = 0$, the hole injection from the source is turned off, and the electron injection on the drain side is suppressed by the negative V_{pg}. Then the device is in the off state. The device thus works in a p-FET mode. A similar n-FET mode can be obtained with $V_{pg} > 0$. Therefore, the device can be set to a particular polarity (n-type or p-type) by tuning the polarity gate, which makes it possible to develop reconfigurable logic gate with functions of logic locking and IC camouflaging. Figure 7(c) depicts the security primitive circuit, a NAND/NOR polymorphic gate composed of reconfigurable BP transistors. It is noteworthy that the polarity gate serves as the key to configure the secure circuit to operate as NAND ($key_i = 0$) or NOR ($key_i = 1$) logic gate. The logic gate can operate properly only when the correct key is set, and the wrong key will only result in a malfunctioning state and logic locking.

The devices mentioned above follow the design principle of the reconfigurable logic gate for von Neumann computing architecture, which faces limitations owing to the physical separation of data processing and memory units when dealing with large amounts of data. Logic in-memory computing architecture is more promising as it integrates processing units into memory units. Inspired by this, Sun *et al.*[114] proposed a partial floating-gate field-effect transistor (PFGFET) based on a vertical dual-gate structure to perform reconfigurable logic-in-memory behaviors, as displayed in Fig. 8(a). Here the device configuration seems similar to that in Fig. 7(a), but the working principle is different. In Fig. 8(a), the two partial graphene flakes under the h-BN are floating gates to trap carriers. When the control gate (CG) is subjected to positive or negative voltage pulses, holes/electrons tunnel into the floating gate layer and are trapped. The trapped charges manipulate the doping of the contact regions, while the top gate is responsible for modulating the channel regions. This allows the device to operate as a reconfigurable FET or a reconfigurable non-volatile memory. Taking the p-FET mode as an example, when the pulse on V_{CG} is -8 V, electrons are trapped in the floating gate, leading to a negligible barrier for holes but high barrier for electrons. With negative top gate voltages applied, the device is set to on state, resulting in a high current output. When positive top gate voltages are applied, the device is set to off state with low current output. When operating as an FET, NOT logic function with a gain as high as 197 can be achieved by using an n-type and a p-type PFGFET to mimic the CMOS inverter (Fig. 8(b)). When operating as a non-volatile memory, reconfigurable logic gates containing two PFGFETs in series can perform NOR, RN-IMP, NIMP and AND logic functions, and simultaneously realize *in situ* storage of logic results (Fig. 8(c)). Such reconfigurability with no more than two devices to construct a logic gate suggests great potential in high-density integration for in-memory computing architecture. Additionally, Sheng *et al.*[27] fabricated a middle-floating-gate FET based on a WSe_2/h-BN/graphene heterostructure to realize reconfigurable logic-

in-memory computing, see Fig. 8(d). The middle floating gate (graphene), control gate (Si) and V_{DS} can jointly control the transportation of the WSe_2 channel, which is similar to that in Figs. 6(d)–6(f). Thus, by using the charges stored in the floating gate serve as one stored logic input, the control gate as another one, and the current in the device acts as the logic output, the single device is able to work as a memory, and perform reconfigurable AND and XNOR logic by varying V_{DS} (Figs. 8(e) and 8(f)). This design can significantly reduce the consumption of transistors for logic gates and serve as a 2D compact reconfigurable transistor architecture in addressing the challenges posed by data-intensive applications in the future.

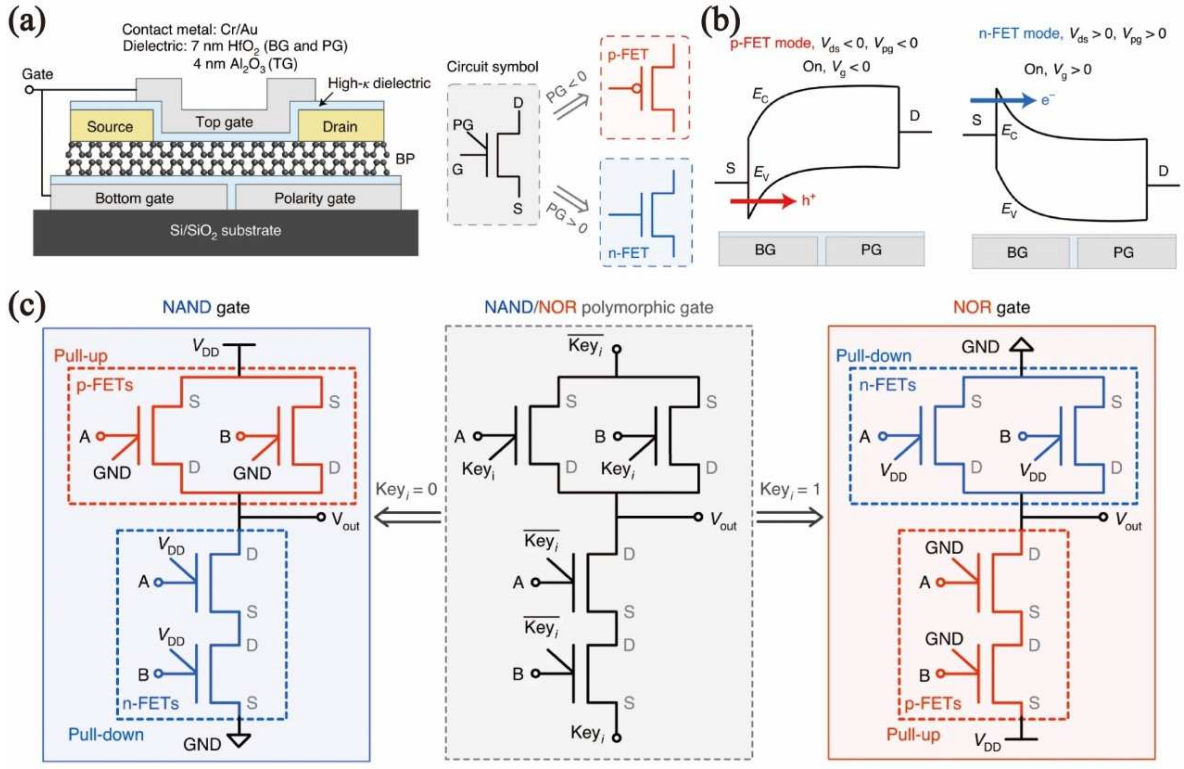


Fig. 7. (a) Schematic of a reconfigurable BP transistor with a vertical triple-gate structure for logic applications with hardware security. (b) Energy band diagrams of the transistor in the on-state for the p-FET mode and n-FET mode. (c) Schematic diagram of a NAND/NOR polymorphic gates by tuning polarity gate of the reconfigurable BP transistors to achieve hardware encryption. All figures are from Ref. [112].

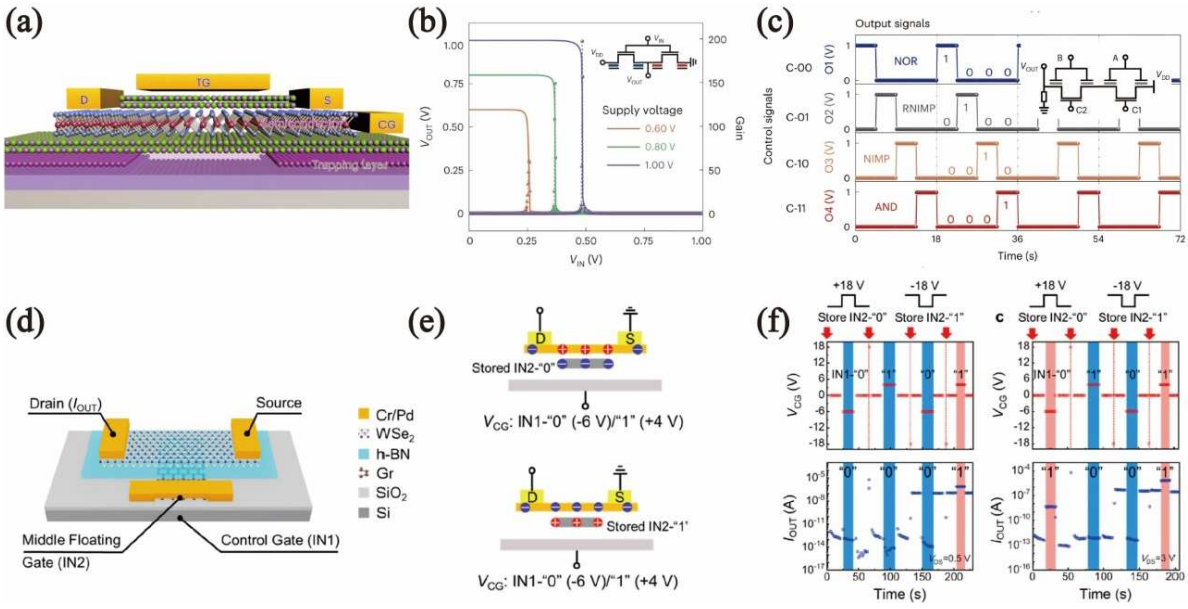


Fig. 8. (a) Schematic of a partial floating-gate field-effect transistor (PFGFET) with a vertical dual-gate structure for reconfigurable logic-in-memory applications. (b) Voltage transfer characteristics and corresponding voltage gain of the CMOS inverter composed of two reconfigurable WSe_2 PFGFETs. The inset shows the schematic of the inverter. (c) Reconfigurable logic gate and its logic functions obtained by two PFGFETs in series. (d) Schematic diagram of a middle-floating-gate field-effect transistor with an overlapping dual-gate structure. (e) Schematic of the device illustrating the operating principle for logic-in-memory computing. (f) Reconfigurable logic functions achieved in this single device. Panels (a)–(c) are from Ref. [114], and panels (d)–(f) are from Ref. [27].

4. Ambipolar 2D semiconductors for reconfigurable optoelectronics

Among various human senses, visual perception is particularly important. This is because 80% of the information in the natural world is perceived through the visual system.[115] To process the massive amount of data received by photodetectors, in-sensor image processing is favorable, especially in real-world and delay-sensitive applications in the era of big data, as it enables simultaneous sensing and processing of optical images without delays. For instance, rapid and accurate recognition can be achieved by convolutional neural networks (CNN) with optoelectronic device array as convolution kernels;[116] artificial neural networks (ANN) implemented with photodiode array have been used to simultaneously sense and process images projected onto chips.[5] To meet the increasing demands of image processing, it is highly desirable to develop new-principle optoelectronic devices and more advanced image sensors that possess reconfigurable and self-learning capabilities. Due to their excellent electrical, optical and photoelectrical properties, 2D materials have emerged as one of the promising candidates for efficient optoelectronics.[15,117,118] For ambipolar 2D semiconductors, their major carrier types (electrons/holes) and concentrations can be dynamically, reversibly, and in real-time modulated by external electrostatic field (corresponding to positive/negative gate voltages), boosting the development of various reconfigurable functional optoelectronic devices. In 2017, Zhang's group developed a field-programmed p–n junction diode with the device in Fig. 4(d), in which the build-in electric field in the diode can be modulated by the gate voltage. This resulted in that the photovoltaic properties can be modulated by the gate voltage. Based on this principle, they proposed the device can be used for logic photodetectors that means the device has the function of integrating photo-sensing and computing (in-sensor computing).[97] Based on ambipolar 2D semiconductors, they also designed and fabricated a semi-floating gate field-effect transistor (SFG-FET, Fig. 5(a)),[29] which was developed for a field-programmed nonvolatile p–n junction diode memory. Similarly, due to the modulated build-in electrical field, the device was developed with the integrated functions of photo-sensing, computing and memory (in-memory sensing and computing). These kinds of devices possess great potential in the fields of new-architecture reconfigurable neuromorphic devices, offering the possibility of achieving efficient environmental information processing.

4.1. Ambipolar 2D semiconductors for optoelectronic synapses

Numerous and various neurons constitute the neural network of the human brain, and the complexity of this network far exceeds any currently manufactured computing system.[119,120] In addition to memory cells, the human brain can make a quick and informed decision on recurring visual information, because human beings can memorize the repeated occurrence with the optimal solution, that is, the synaptic weights of this neural network have already updated to optimum by learning over and over again.[119] Synaptic plasticity is an experience-dependent change in the connections between neurons. The ability of synapses to be potentiated or depressed by changes in neuronal activity is considered to be a basic and decisive factor in learning and memory.[121–123] Synaptic plasticity mainly has two forms of long-term synaptic plasticity and short-term synaptic plasticity. The former usually lasts from a few minutes to a few hours, representing learning and memory ability, including long-term potentiation (LTP) and long-term depression (LTD), while the latter is regarded as the physiological basis of key calculations, showing a rapid decay of synaptic responses on a time scale of a few seconds, including short-term facilitation (STF), short-term depression (STD), and short-term potentiation (STP).[123,124]

In the process of simulating synaptic functionality, the internal conductivity (synaptic weight) of a synapse-like device is altered by external signals, and the conductance state is memorized by various memory mechanisms. In order to avoid refreshing the stored state or dissipating energy, the non-volatile characteristic of memory devices is essential.[119,125] Synapse-like devices share many common characteristics of non-volatile memories (NVM), such as facilitating programming, reading, and information retention.[126] In earlier stage, researchers often achieved optoelectronic synapses by simply integrating photodetectors with non-volatile memory devices.[127–129] Emerging NVM such as phase change memory (PCM) and resistive random access memory (RRAM) have been adopted as synapse-like devices.[126] By developing weight-update optimization algorithms for memory devices, it is possible to realize brain-inspired functionality.[130]

Optoelectronic synapse-like devices mainly rely on optical signals or optical and electrical combination signals to perform synaptic functionality simulation,[131,132] which can be used to develop neuromorphic visual systems.[133] Optoelectronic synapse (it actually binds one photoreceptor neuron) can simultaneously detect and memorize optical signals.[134,135] The introduction of light stimulation extends external stimulation beyond electricity, providing another degree of freedom for controlling device performance, and opens up new possibilities for multi-gate neuromorphic structures.[136] Moreover, the optoelectronic devices based on the optical signal drive have great advantages in power consumption, speed and stability,[120,137] which can be used to construct artificial visual neuromorphic system. Based on the MoS_2/h-BN

structure, Sun *et al.* constructed synapses regulated by optical and electrical stimulations.[134] The device uses h-BN with photoactive-inherent defects to memorize weights, and the ionization and neutralization of intrinsic defects can be excited by both optical and electrical spikes. When the optical spike is applied under a negative weight control voltage, electrons are excited from the inherent defects of h-BN and injected into MoS_2. The ionized defects in h-BN act as positive fixed charges, increasing the surface potential of MoS_2 and the electron injection rate from the presynaptic electrode to the channel region. This increases the channel conductance, which is called LTP. When the optical spike is applied under the positive weight control voltage, the photogenerated electrons fill the empty defect states in the h-BN, and the generated holes move to the MoS_2 region and recombine with the electrons in the MoS_2 conduction band. This reduces the channel conductance, known as LTD.

Li *et al.* fabricated a heterojunction device with n-type semiconductor CdS and ambipolar semiconductor BP (intrinsically p-type).[138] In the semi-photo-gate transistor structure as shown in Fig. 9(a), BP is used as the conduction channel and CdS serves as the photo-gate layer. Only part of the BP is aligned on the CdS. Upon laser irradiation, electrons are transferred from the CdS to the BP channel, while holes are trapped in the CdS (Fig. 9(b)). The holes trapped in the CdS induce mirror-image charges in the partial BP aligned on the CdS, which causes the upshift of the Fermi level and weakens the p-type characteristic (Fig. 9(c)). As the illumination power increases, the BP aligned on the CdS becomes n-type, and the device is adjusted from the p–p junction (resistor) to the p–n junction (diode), resulting in a decrease in the channel current (Fig. 9(d)). Light input can be used to define 2D p–n junctions instead of electrostatic field.[140] By this approach, they also develop an artificial photonic synapse based on the BP/CdS van der Waals heterojunction (Fig. 9(e)).[139] Figure 9(f) is a 2D plot of I_D as a function of the light intensity and V_G, which shows a negative light response of the heterojunction in more detail. When the illumination is removed, the trapped holes in the CdS can be well maintained (Fig. 9(h)), so that the channel remains in a small current state (Fig. 9(g)). This is the essential characteristic of the artificial photonic synapses with multimodal plasticity. Photo-activated postsynaptic current (PSC) shows a significant negative increment (defined as $-\Delta$PSC). In dark conditions, the positive gate voltage drives electrons to transfer into the CdS and recombine with trapped holes, resulting in a decrease of $-\Delta$PSC, which is a synaptic depression process. Based on the synergistic effect of optical programming and electrical erasing in the artificial synapse, LTP induced by light stimulation and LTD driven by electrical input are clearly demonstrated in Fig. 9(i).

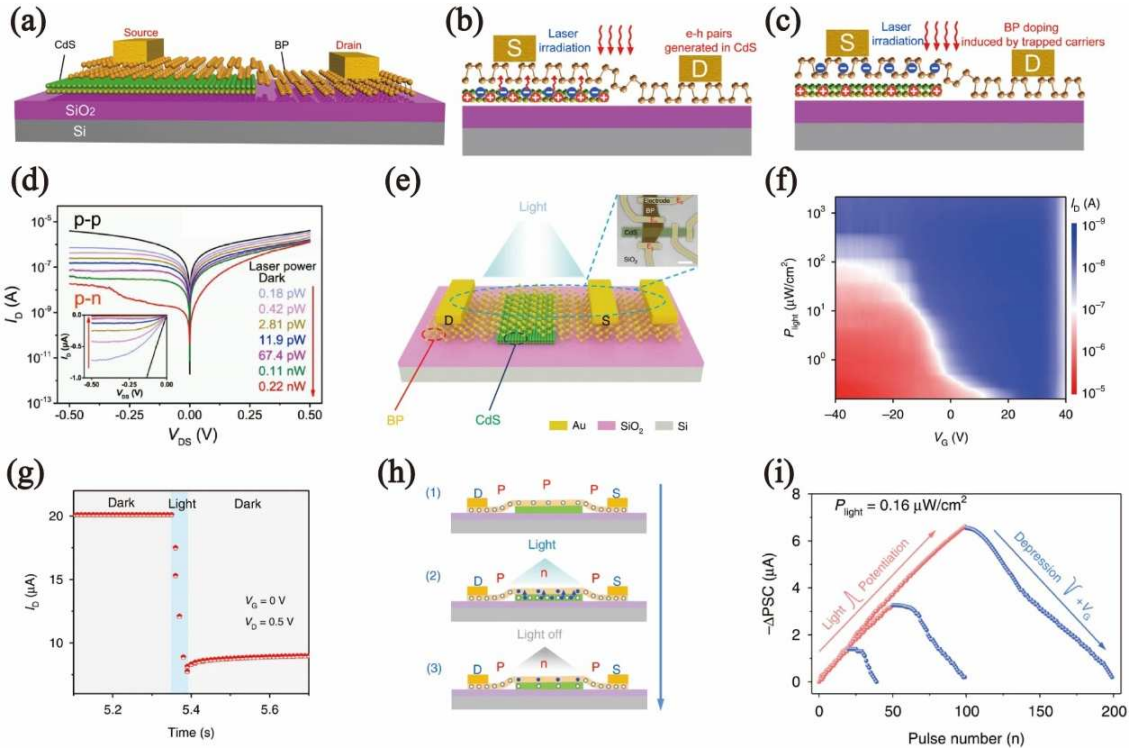


Fig. 9. (a) Schematic of the semi-photo-gate transistor device structure. (b) Separation of the electron–hole pairs in the CdS under laser illumination. (c) Charge carrier modulation in the BP over the CdS photo-gate layer. (d) I_D–V_{DS} curves across the BP under different laser powers. (e) Schematic of the artificial photonic synapse based on BP/CdS vdWs heterojunction. (f) 2D plot of I_D as a function of light power intensity and V_G. (g) Photo-activated postsynaptic current of the artificial photonic synapse ($-\Delta$PSC) after irradiation. (h) Working mechanism of the BP/CdS heterojunction. (i) LTP/LTD properties of the artificial photonic synapse. Panels (a)–(d) are from Ref. [138], and panels (e)–(i) are from Ref. [139].

4.2. Ambipolar 2D semiconductors for reconfigurable devices in neural networks

The key to neuromorphic computing lies in emulating the architecture and functionality of biological neural networks, thereby achieving brain-like high energy-efficiency and low power-consumption computation.[143] To construct a neural network, researchers need to develop electronic components with reconfigurable characteristics, allowing flexible resource allocation for different computing tasks.[144] Reconfigurable circuits possess the ability of self-adjustment to dynamically behave like neurons or synapses in biological neural systems.[145–147] These circuits can simulate synaptic behaviors such as LTP and LTD.[148] With reconfigurable circuits with self-adjustment capacity, efficient neural network models that apply to various tasks can be developed.

ANN and CNN are common neural network models for image and data processing, as shown in Fig. 10. In ANN, inputs are received by presynaptic neurons and weighted by synapses, and then the weighted inputs are transformed into an activation function and become new inputs of postsynaptic neurons. The neuron-layers in the ANN are all fully connected layers, meaning that each neuron of the hidden layer and output layer is connected to every neuron of the upper layer. ANN is suitable for various tasks such as classification, regression, and clustering.

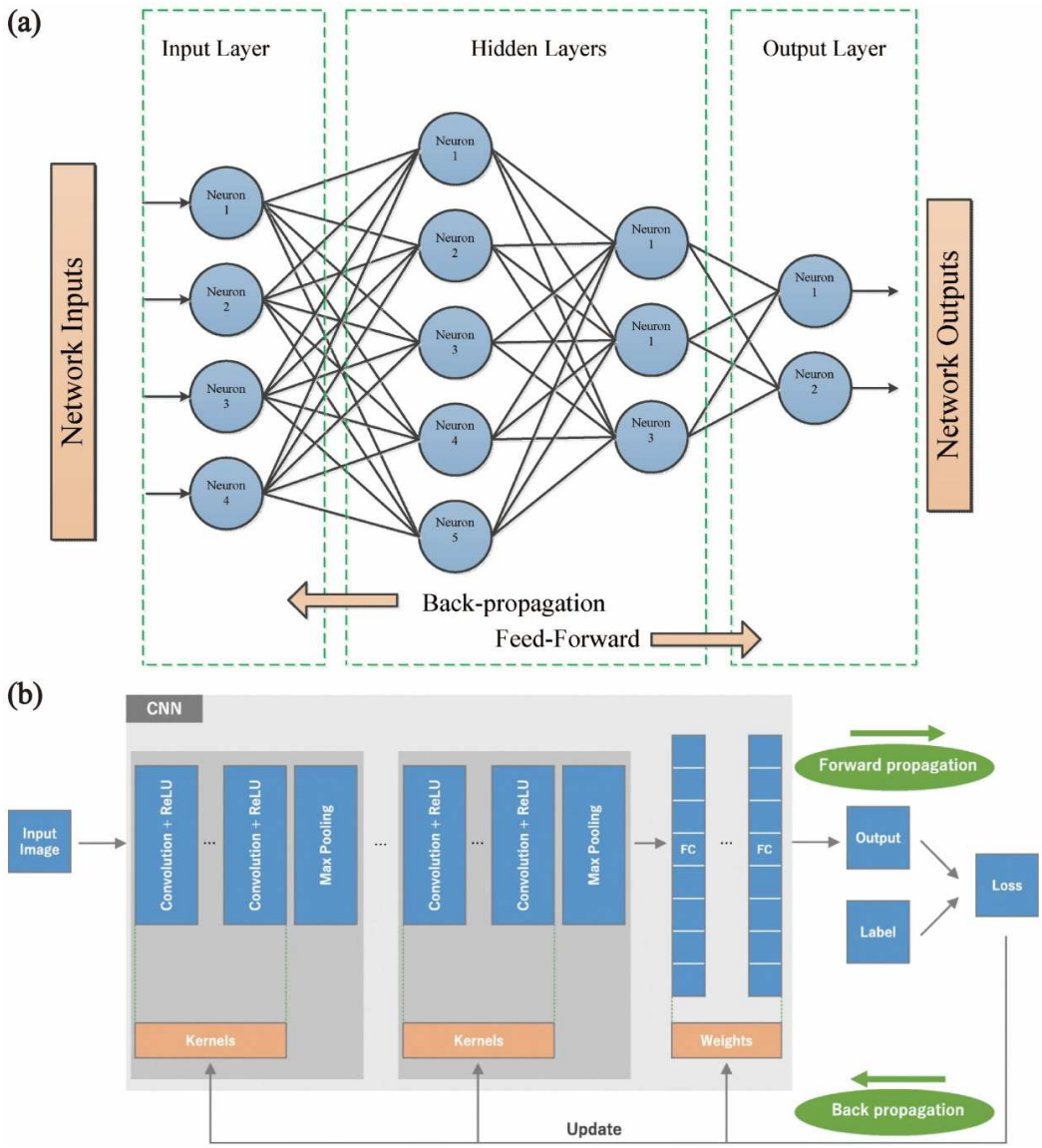


Fig. 10. (a) Schematic of an ANN architecture with feedforward and backpropagation algorithms.[141] (b) Schematic of the CNN architecture and training process.[142]

CNN is a more complex neural network than ANN, primarily used for image processing. The feature of the CNN is that it includes convolutional layer and pooling layer in addition to fully connected layer. The convolutional layer extracts feature from images by sliding different kernels and generates feature maps. And the pooling layer reduces the size of the feature maps. CNN gradually extracts high-level feature from images through multiple convolutional and pooling oper-

ations, and then performs classification or regression tasks by fully connected layer. CNN has achieved significant success in the field of machine vision system. It can automatically obtain features of images, such as edges, textures, and shapes, further fulfill tasks like image classification, object detection, and image segmentation.

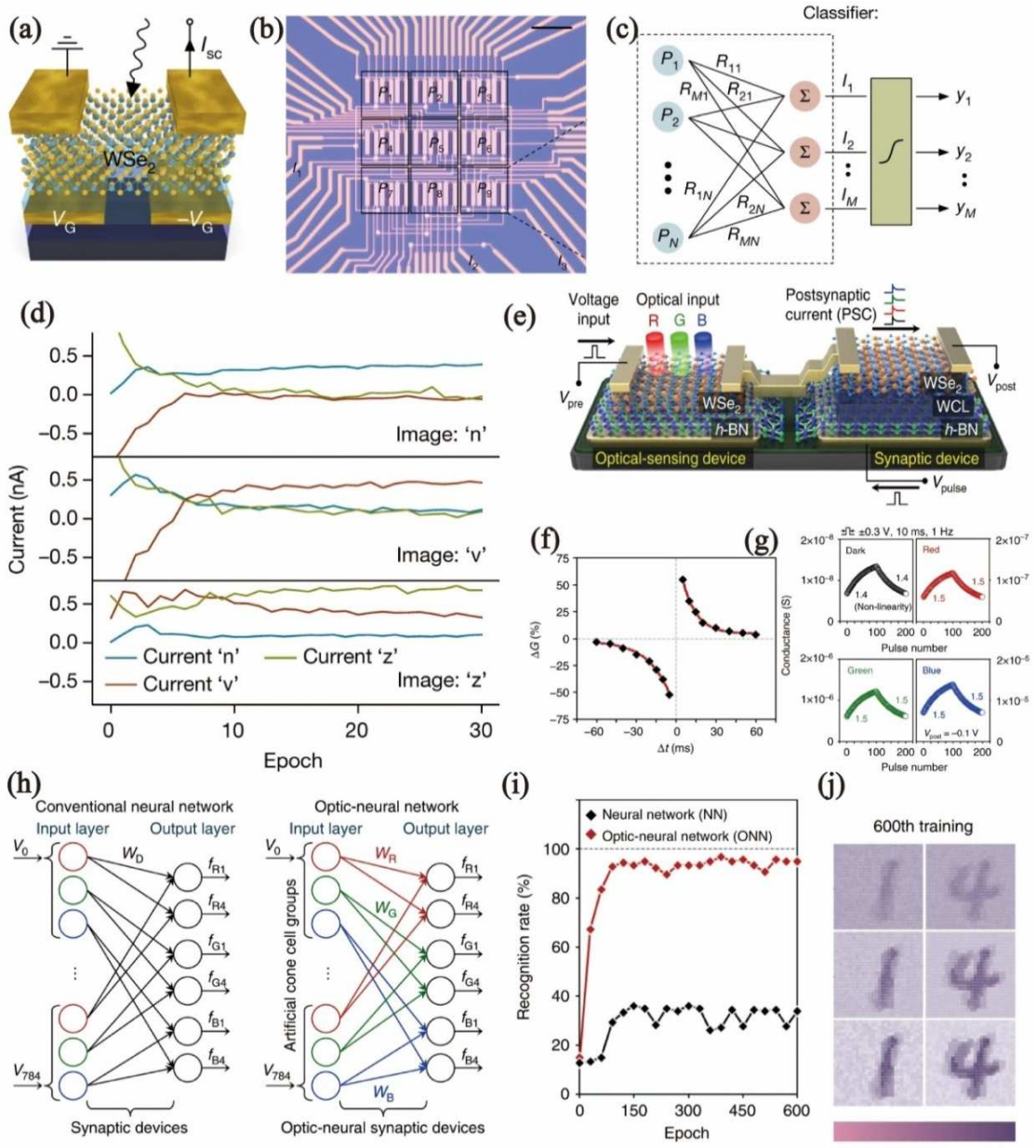


Fig. 11. (a) Schematic of a single WSe_2 photodiode. (b) Macroscopic image of the photodiodes array. (c) Schematic of the classifier. (d) Average current of each projected letter was measured at each epoch during training with a noise level of $\sigma = 0.2$. (e) h-BN/WSe_2 synaptic device integrated with a h-BN/WSe_2 photodetector. (f) Plasticity behavior of peak-timing-dependent in the synaptic-like device. (g) Long-term potentiation and depression curves under different wavelengths of light illumination. (h) Conventional neural network and artificial optical neural network for color image recognition. (i) Recognition rate as a function of training epochs. (j) Weight mapping image after the 600th training epochs. Panels (a)–(d) are from Ref. [5], and panels (e)–(j) are from Ref. [149].

Ambipolar 2D semiconductors have excellent electronic and photoelectric properties, which can constitute a reconfigurable photodetectors array with linear light intensity dependence.[150] Encoding the weights by gate-voltage matrix, the reconfigurable photodetectors array exhibits the capacity of image processing.[116] The integration of synapse behavior and photoreception possesses promising opportunities for neural network with simultaneous sensing and computing capacities, enabling low power-consumption and delay-free image recognition.[149] With ambipolar semiconductors, it becomes possible to directly receive external visual information and obtain pre-processed visual data in artificial visual systems. Simultaneously, neuromorphic computing can combine various sensors with a wide range of perception like vision, touch, and hearing.[119] Mennel *et al.*[5] fabricated a photodiode array that can simultaneously sense and process the image projected onto the chip. The sensor uses the photoresponsivity matrix to perform real-time multiplication by

the light intensity distribution of the projected image. The mth detector element of each pixel performs the matrix vector product operation and is added for general photocurrent, $I_m = \sum_{n=1}^{N} I_{mn} = \sum_{n=1}^{N} R_{mn} P_n$. Figure 11(a) is the schematic diagram of a WSe_2-based photodiode. WSe_2 is chosen because of its ambipolar conduction behavior and excellent photoelectric properties. The photo-response can be set by electrostatic doping of the gate electrodes. Two functions of the ANN are implemented: classifier and autoencoder. Figure 11(c) is the schematic diagram of the classifier, which is used to identify the letters n, v and z. In Fig. 11(d), the average current generated by letter projected on the chip of each epoch is shown. The general currents become well distinguishable after about 10 epochs, and the maximum current corresponds to the label of the projected letter.

Seo *et al.*[149] integrated a synapse-like device with an optical-sensing device with the same h-BN/WSe_2 heterostructure (Fig. 11(e)). The synapse-like device, whose synaptic weights were determined by the WSe_2 channel conductivity, relied on the capture or release of electrons in the weight control layer (WCL). Due to higher light absorption at shorter wavelengths, the resistance of the device was modulated as a function of the wavelength of the incident light, making it capable of color recognition. The device was controlled by input pulses with an amplitude of 0.3 V, enabling LTP/LTD and spike-timing-dependent plasticity (STDP) as depicted in Figs. 11(f) and 11(g), thus exhibiting learning and memory capabilities,[124] along with the potential for application in spiking neural networks. Utilizing the extracted device parameters and a simple perceptron network model, an optical neural network (ONN) was developed. Two types of neural network were implemented for recognizing target-color numbers from mixed-color images, as shown in Fig. 11(h). After the 50th epoch, the recognition rate of the ONN exceeded 90% as demonstrated in Fig. 11(i), significantly outperforming the neural network without optical sensing capability. Due to the strongest photo-response to blue light input, the synaptic weights for the blue pattern were higher than those for other colors after 600 training epochs, as illustrated in Fig. 11(j).

To meet the increasing demands of high-speed and low power-consumption image processing, it is highly desirable to employ reconfigurable photodetectors to build reconfigurable convolutional kernels for advanced image sensors to construct CNN with improved image processing architecture than ANN. As we mentioned above, ambipolar 2D semiconductors are suitable for optoelectronic devices. By encoding synaptic weights through a gate voltage matrix, different convolutional kernels can be constructed. Jang *et al.*[151] fabricated an in-sensor computing device using electrostatically doped dual-gate silicon p–i–n photodiode, which can be used for convolutional neural networks. It contains two contact electrodes on the intrinsic silicon wafer to provide the current path, and two top gate metal electrodes (Fig. 12(a)). When the top gate electrodes are biased with voltages of the same magnitude but opposite signs, electrostatically doped p and n regions are created. The silicon region not covered by the top gate metal is the intrinsic region, acting as the photosensitive area. Altering the gate voltage modifies the built-in potential (V_{bi}) (Fig. 12(a)), consequently modifying the magnitude and direction of the photocurrent for a given incident light power, as shown in Fig. 12(b). A 3×3 network of the electrostatically doped photodiode is used as an optical convolution processor, which can be electrically programmed into different convolutional filters (Fig. 12(c)). By designing image filtering kernels, the 3×3 photodiode network not only captures the input scene but also processes it simultaneously. Different combinations of gate voltages can achieve distinct repeated processing of the internal sensor images using various filtering kernels, as illustrated in Figs. 12(d) and 12(e). Pi *et al.*[150] utilized $PdSe_2$/$MoTe_2$ vdW heterostructure, which also possesses gate-tunable positive and negative photo-responses, as well as linear gate-dependent photoresponsivity and broadband sensing capability. Different objects emit light at different wavelengths. Therefore, in applications such as remote sensing and environmental monitoring, broadband convolutional processing is crucial for high-precision image recognition.

The visual sensor constructed with the aforementioned ambipolar 2D semiconductors possesses integrated optical and static signal and processing capability but lacks the ability to store visual information, thereby preventing the extraction and processing of moving objects.[116] However, in the era of the internet of things (IoTs), there are increasing demands for real-time and accurate detection of moving objects.[153] It requires the integration of memory cell, computing unit and perception sensor within the vision sensory system.[154] Zhang *et al.*[152] proposed a BP/Al_2O_3/WSe_2/h-BN heterostructure as neuromorphic optoelectronic device, which adopted a floating-gate structure for charge storage and electrostatic doping of the BP channel. The photoelectric synergistic regulation changes the stored charge in the floating gate WSe_2 to achieve positive and negative photoconductivities. The device realizes motion detection without extensively redundant and static information by reconfiguring the switch states, as shown in Fig. 13. By mapping the conductivity states of the visual sensory array, rapid and accurate motion recognition can be achieved. The spatial information with light intensities of the images corresponding to the start and end of the motion is multiplied by the positive and negative conductivity matrices, respectively, and then added together, resulting in a final pixel output ($W_1X + W_2Y$). Due to the similar absolute values but opposite directions of the positive and negative conductivity matrices, if there are no moving objects, the brightness distribution of almost all pixel outputs is close to zero. However, for a moving object, the amplitude difference cannot be completely canceled, and the detection result appears as bright spots distributed in the processed current map.

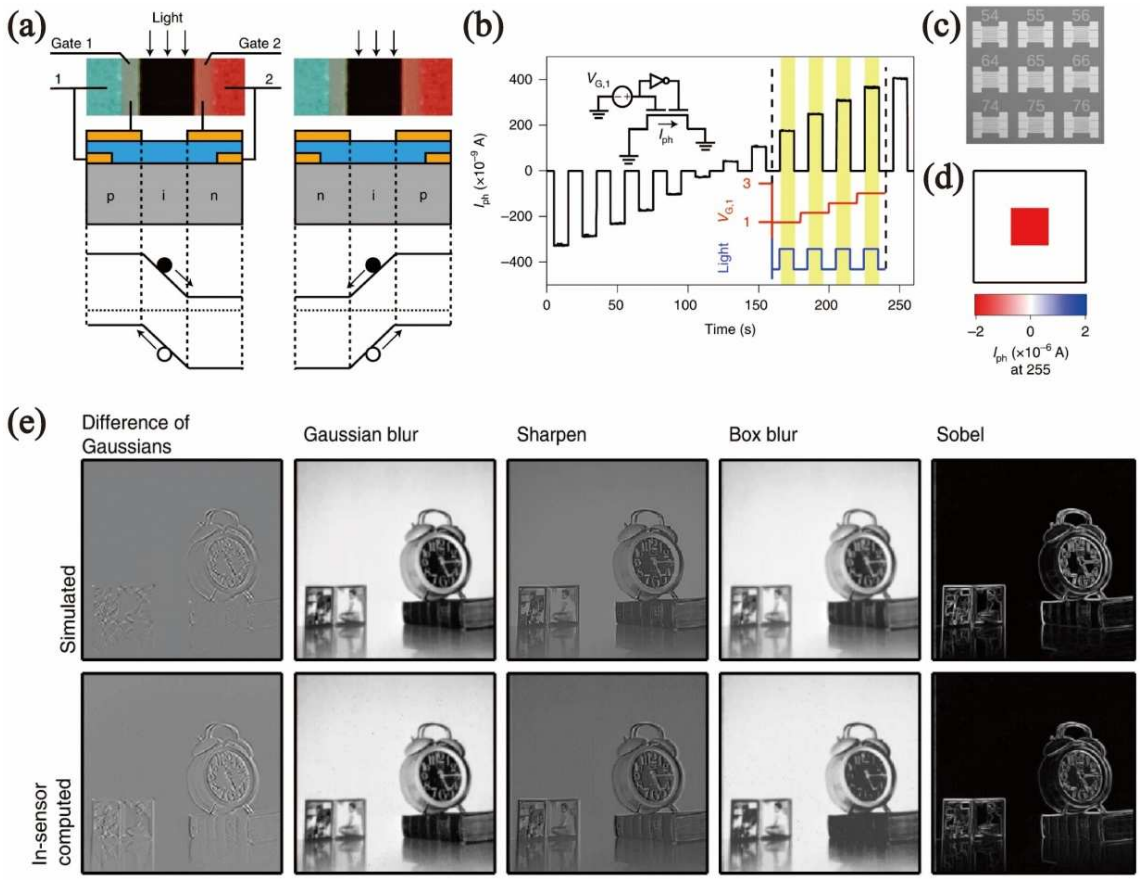


Fig. 12. (a) Part of the SEM image of the device (top) and the corresponding schematic (bottom) of the cross-sectional view of the photodiode, gate biased to form p–i–n and n–i–p configurations. (b) The photocurrents of a red-filtered halogen lamp at different gate voltages. (c) An SEM image of nine example photodiodes. (d) Programmed photocurrent map with a fixed power of light. (e) Various filtered images were obtained with digital computing (top) and in-sensor computing (bottom). All figures are from Ref. [151].

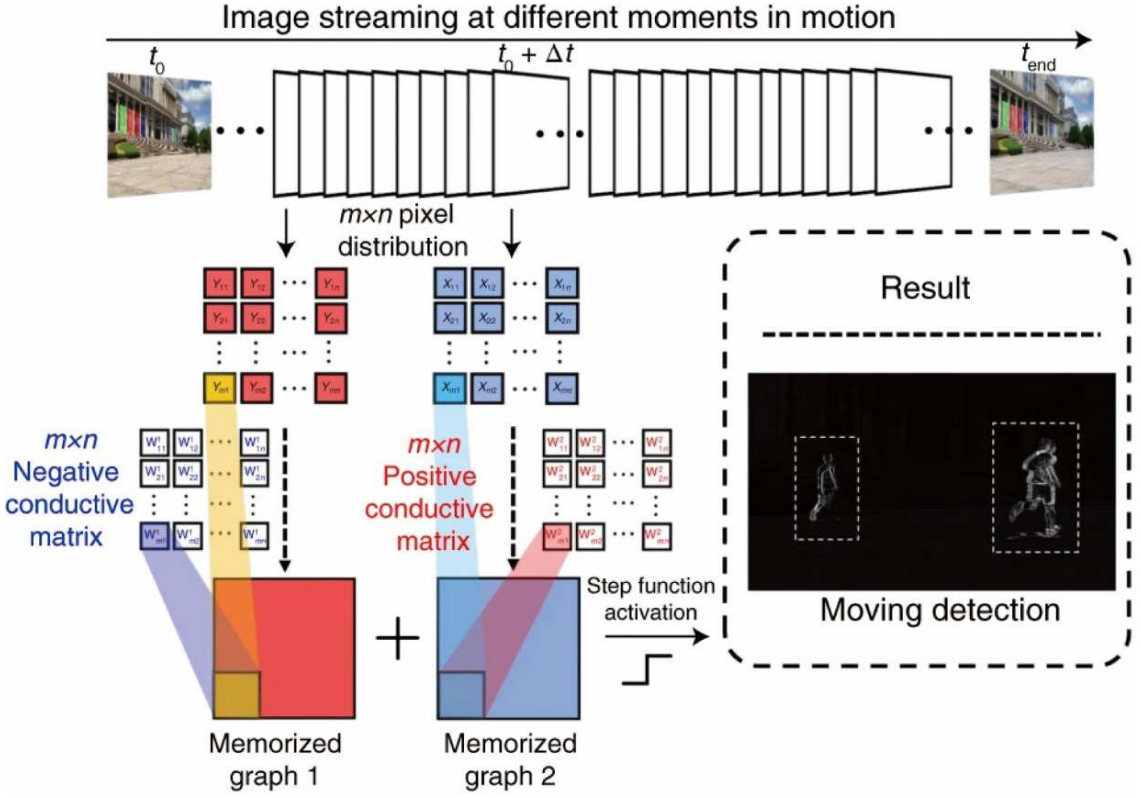


Fig. 13. Method for motion detection implemented by the device array: by detecting and differencing the images at different time points, the motion detection scheme can identify bright spots for moving objects and dark spots for static objects.[152]

5. Conclusion and outlook

After a simple introduction of ambipolar 2D semiconductors, this review provides an overview of the recent progress of their applications on reconfigurable electronic and optoelectronic devices. Ambipolar 2D semiconductors are of excellent gate control capabilities and unique physical properties, allowing for dynamic and reversible modulation of the major charge carriers between holes and electrons via electric field. Such characteristic enables them conductive to develop reconfigurable electronic and optoelectronic devices, including ambipolar FETs for CFET-like inverters working in the first and third quadrants, anti-ambipolar FETs for multi-value logic inverters and frequency doubling circuits, programmable p–n junctions for reconfigurable rectification circuits, reconfigurable logic gates, and reconfigurable optoelectronic devices in neuromorphic circuits. These applications have shown great potential in computing capacity, energy efficiency, time delay and cost, and thus flourished studies in this field. Although a significant progress has been achieved in this field, there are still some crucial challenges that need to be addressed.

(i) From a single-device perspective, device performance needs to be optimized and improved. Material, contact, and interface are three key factors to affect the device's performance. Up to now, over 20 kinds of ambipolar 2D semiconductors have been revealed, part of which have been developed for polarity-controlled devices. With the deepening of the study, more ambipolar 2D semiconductors are expected to be discovered. This will provide an experimental foundation to explore excellent ambipolar devices with wanted functions. In the future, it is necessary to target the application fields and scenarios to exploit suitable ambipolar 2D semiconductors for high-performance devices and chips, and build a database of materials including their device performances and application fields.

For contact, ambipolar-based devices require the transmission of both holes and electrons. The intrinsic property of metal–semiconductor ohmic contact decides that the p-type contact is only conductive to holes, and n-type contact is only beneficial for electrons. The current method adopts Schottky contact to balance the transmission of holes and electrons. It means both holes and electrons have to overcome their corresponding barrier potentials, which hinder the improvement of device performance. Better techniques and theories are required to be developed to address such issues. Recently, Wang *et al.*[155] used van der Waals contact between WSe_2 and Pd/Cr to improve the ambipolar behavior. They found the effective barrier height for holes and electrons in such a configuration can be negligible. Zhang *et al.*[156] defined a feasible strategy for removing the Schottky barrier of metal–semiconductor contact. The full van der Waals barrier-free contact between a p-type Te semiconductor and a layered 1T′-WS_2 semi-metal has been reported, achieving a zero Schottky barrier height of 3 ± 9 meV and a high field-effect mobility of $\approx 1304\ \mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$. These methods provide valuable ways and should be helpful in improving the contact of ambipolar 2D semiconductors. In the future, more methods and theories are urgently needed to resolve the contact issue whether for device performance or large-scale integration.

The interface between 2D materials has a great effect on device performance. Ultrathin 2D materials possess perfect crystalline structures and surfaces. Theoretically, the composed devices should be of clean and sharp interfaces. In real fabrications, the interface is usually affected by many factors like the growing and transferring techniques, which often result in contaminations, wrinkles, and bubbles. An effective process should be developed to resolve such concerns. It is worth noting that it is a systemic issue for contact, material, and interface. To improve the device performance, we should systemically study these concerns in some certain application fields and scenarios.

(ii) From an application perspective, it is still limited by the large-scale high-quality semiconductors, mature process of ambipolar device fabrication and integration, circuit design methodology, and algorithm. Although tens of ambipolar 2D semiconductors have been discovered, current high-quality materials are usually acquired by mechanical exfoliation method from bulk crystals. There is still a big challenge to get high-quality large-scale ambipolar 2D semiconductors. This needs researchers to develop effective, low-cost, and technique-compatible methods, or search around in the conventional material and technique warehouse. In the last decade, great success has been achieved for the growth of 2D materials by some techniques like chemical vapor deposition (CVD), molecular beam evaporation (MBE), and atomic layer deposition (ALD), which should be helpful in the growth of ambipolar 2D semiconductors.

Currently, in pursuit of achieving versatile functionalities, the designed reconfigurable devices often possess intricate structures. However, for practical applications, there is a need to explore device architectures that are suited for integration and miniaturization. For instance, the emerging in-memory computing devices and in-sensor computing devices should be developed in the use of neuromorphic computing systems and numerical computations.[157–159] As neural networks continue to scale up, it is becoming increasingly necessary, from a hardware implementation perspective, to develop device structures that are more suitable for integration to facilitate larger-scale production. Simple and reliable device structures, as well as mature fabrication and integration processes get to be emergent. One possible way is to graft ambipolar 2D semiconductors in the conventional device structures. Another possible way is to develop full 2D devices, which can be assembled by van der Waals force to avoid many problems in conventional routines. Memories based on ferroelectric FETs are of simple device structure. α-In_2Se_3, as

a 2D ferroelectric material (2DFM) with high Curie temperature, has been used to construct a van der Waals (vdW) ferroelectric tunnel junction (FTJ) memory with excellent reliability at both room temperature and high temperatures.[160] The memory has a long retention time at high temperatures and a reliable cycle life, which shows good thermal stability of vdW FTJ memory. 1L-MoS_2/WSe_2/graphene heterostructures with efficient photocarrier collection and gate modulation achieve high EQE (61%) and exhibit ultra-fast optical response (4.1 μs) at the atomic thin limit (8 nm).[161] These exploratory research achievements may be used for reference in the preparation of ambipolar-based simple-structure devices for high-performance applications.

In addition, the composed new-architecture chips are different from the conventional ones, so a new circuit design methodology has to be developed for the large-scale integration. These new-architecture chips often excel at performing multiply accumulate (MAC) operations efficiently, particularly in executing vector-matrix multiplication (VMM). However, they face the challenge of being locked into specific algorithms. The achievement of cooperativity between these structures and algorithms requires further exploration. Considering the foreseeable difficulties of traditional semiconductor devices and computing architectures, it is of great motivation to address such issues.

(iii) Vertical assembling of 2D materials may be a valuable way for further study and applications, which are promising to transcend the chip size limits.[162,163] Vertical heterostructures formed by multiple stacking via van der Waals integration, provide a method for three-dimensional integration of 2D materials at both the device and circuit levels.[164] Due to their extremely thin thickness, 2D vertical heterostructures provide a short diffusion distance for charge carriers.[165,166] In contrast to laterally stacked heterojunctions, vertically stacked heterostructures offer a larger surface area for the interface of layered materials and involve tunneling effect between the two layers, making it highly suitable for photosensitive device applications.[167]

Vertical van der Waals heterostructures combined with ambipolar 2D semiconductors allow for the integration of highly disparate materials with crystal lattice mismatching.[168] They have been employed in the construction of high-performance electronic and optoelectronic devices, such as $ReSe_2$/MoS_2 van der Waals heterostructures, which exhibit ultra-fast and linear polarization-sensitive photodetectors,[169] vertical MoS_2/WS_2 heterostructure with ambipolarity behavior,[170] vertical graphene/WS_2/graphene van der Waals heterostructure with a low off-state current and a high ON/OFF ratio, exhibiting both n-type and bipolar-type conduction,[171] $ReSe_2$/$PtSe_2$ heterojunction for high-performance photodetectors,[172] WSe_2/InSe heterostructure photodetector with ambipolar photoresponsivity,[173] and ambipolar SnO/SnS heterojunction transistors employed to build CMOS inverters.[174] Such investigations indicate that vertical heterostructures hold great potential for use in reconfigurable devices towards high-performance integrated circuits and systems.

We hope this review will help to push forward the studies of ambipolar semiconductors, including the theories, materials, devices, process of integration, circuits methodology, and application algorithm.

Acknowledgments

Project supported by the National Natural Science Foundation of China (Grant No. 62274037), the National Key Research and Development Program of China (Grant No. 2018YFA0703703), the Ministry of Science and Technology of China (Grant No. 2018YFE0118300), and the State Key Laboratory of ASIC & System (Grant No. 2021MS003).

References

[1] Golio M 2015 *Proc. IEEE* **103** 1932
[2] Lundstrom M 2003 *Science* **299** 210
[3] Frank D J, Dennard R H, Nowak E, Solomon P M, Taur Y and Wong H S P 2001 *Proc. IEEE* **89** 259
[4] Theis T N and Wong H S P 2017 *Comput. Sci. Eng.* **19** 41
[5] Mennel L, Symonowicz J, Wachter S, Polyushkin D K, Molina-Mendoza A J and Mueller T 2020 *Nature* **579** 62
[6] Zhou F, Zhou Z, Chen J, Choy T H, Wang J, Zhang N, Lin Z, Yu S, Kang J, Wong H S P and Chai Y 2019 *Nat. Nanotechnol.* **14** 776
[7] LeCun Y, Bengio Y and Hinton G 2015 *Nature* **521** 436
[8] Sangwan V K and Hersam M C 2020 *Nat. Nanotechnol.* **15** 517
[9] Sebastian A, Le Gallo M, Khaddam-Aljameh R and Eleftheriou E 2020 *Nat. Nanotechnol.* **15** 529
[10] Xiong X, Kang J, Hu Q, Gu C, Gao T, Li X and Wu Y 2020 *Adv. Funct. Mater.* **30** 1909645
[11] Boybat I, Le Gallo M, Nandakumar S R, Moraitis T, Parnell T, Tuma T, Rajendran B, Leblebici Y, Sebastian A and Eleftheriou E 2018 *Nat. Commun.* **9** 2514
[12] Meng J L, Wang T Y, He Z Y, Chen L, Zhu H, Ji L, Sun Q Q, Ding S J, Bao W Z, Zhou P and Zhang D W 2021 *Mater. Horizons* **8** 538
[13] Sun Z, Li J, Liu C, Yang S and Yan F 2021 *Nano Lett.* **21** 723
[14] Xia Q and Yang J J 2019 *Nat. Mater.* **18** 309
[15] Hu W, Sheng Z, Hou X, Chen H, Zhang Z, Zhang D W and Zhou P 2021 *Small Methods* **5** 2000837
[16] Novoselov K S, Mishchenko A, Carvalho A and Neto A H C 2016 *Science* **353** aac9439
[17] Seo S, Lee J J, Lee H J, Lee H W, Oh S, Lee J J, Heo K and Park J H 2020 *ACS Appl. Electron. Mater.* **2** 371
[18] Feng X, Sun Z D, Pei K, Han W, Wang F K, Luo P, Su J W, Zuo N, Liu G H, Li H Q and Zhai T Y 2020 *Adv. Mater.* **32** 2003146
[19] Radisavljevic B, Radenovic A, Brivio J, Giacometti V and Kis A 2011 *Nat. Nanotechnol.* **6** 147
[20] Wang X D, Wang P, Wang J L, *et al.* 2015 *Adv. Mater.* **27** 6575
[21] Long M S, Wang P, Fang H H and Hu W D 2019 *Adv. Funct. Mater.* **29** 1803807
[22] Lim S and Suk J W 2023 *J. Phys. D: Appl. Phys.* **56** 063001
[23] Hirakata H, Fukuda Y and Shimada T 2022 *J. Phys. D: Appl. Phys.* **55** 125302
[24] Li D, Xu J R, Ba K, Xuan N, Chen M, Sun Z, Zhang Y Z and Zhang Z 2017 *2D Mater.* **4** 031009
[25] Dong J, Sheng Z, Yu R, Hu W, Wang Y, Sun H, Zhang D W, Zhou P and Zhang Z 2022 *Adv. Electron. Mater.* **8** 2100829
[26] Zong Q J, Zhang Q C, Mei X, Li Q L, Zhou Z Y, Li D, Chen M Y, Shi F Y, Sun J, Yao Y G and Zhang Z X 2018 *ACS Appl. Mater. Interfaces* **10** 37233
[27] Sheng Z, Dong J G, Hu W N, Wang Y, Sun H R, Zhang D W, Zhou P and Zhang Z X 2023 *Nano Lett.* **23** 5242

[28] Sheng Z, Wang Y, Hu W N, Sun H R, Dong J G, Yu R, Zhang D W, Zhou P and Zhang Z X 2023 *Nano Res.* **16** 1252
[29] Li D, Chen M Y, Sun Z Z, Yu P, Liu Z, Ajayan P M and Zhang Z X 2017 *Nat. Nanotechnol.* **12** 901
[30] Pan C, Wang C Y, Liang S J, *et al.* 2020 *Nat. Electron.* **3** 383
[31] Tong L, Peng Z, Lin R, *et al.* 2021 *Science* **373** 1353
[32] Hu W N, Wang H, Dong J G, Sun H R, Wang Y, Sheng Z and Zhang Z X 2023 *ACS Appl. Mater. Interfaces* **15** 18182
[33] Zhang H T, Park T J, Islam A N M N, *et al.* 2022 *Science* **375** 533
[34] Ren Y, Yang X, Zhou L, Mao J Y, Han S T and Zhou Y 2019 *Adv. Funct. Mater.* **29** 1902105
[35] Zhang Z X and Li D 2017 *Acta Phys. Sin.* **66** 217302 (in Chinese)
[36] Bisri S Z, Piliego C, Gao J and Loi M A 2014 *Adv. Mater.* **26** 1176
[37] Beddiar M I, Zhang X K, Liu B S, Zhang Z and Zhang Y 2022 *Small Struct.* **3** 2200125
[38] Li S, Ma Y, Ouedraogo N A N, Liu F, You C, Deng W and Zhang Y 2022 *Nano Res.* **15** 123
[39] Lin C P, Chen P C, Huang J H, Lin C T, Wang D, Lin W T, Cheng C C, Su C J, Lan Y W and Hou T H 2019 *ACS Appl. Electron. Mater.* **1** 684
[40] Gao L, Liao Q, Zhang X, Liu X, Gu L, Liu B, Du J, Ou Y, Xiao J, Kang Z, Zhang Z and Zhang Y 2020 *Adv. Mater.* **32** 1906646
[41] Nipane A, Karmakar D, Kaushik N, Karande S and Lodha S 2016 *ACS Nano* **10** 2128
[42] Chang Y M, Yang S H, Lin C Y, Chen C H, Lien C H, Jian W B, Ueno K, Suen Y W, Tsukagoshi K and Lin Y F 2018 *Adv. Mater.* **30** 1706995
[43] Fang H, Chuang S, Chang T C, Takei K, Takahashi T and Javey A 2012 *Nano Lett.* **12** 3788
[44] Gong Y J, Yuan H T, Wu C L, *et al.* 2018 *Nat. Nanotechnol.* **13** 294
[45] Cristoloveanu S, Lee K H, Park H and Parihar M S 2019 *Solid-State Electron.* **155** 32
[46] Beck M E and Hersam M C 2020 *ACS Nano* **14** 6498
[47] Liu Y, Guo J, He Q Y, Wu H, Cheng H C, Ding M N, Shakir I, Gambin V, Huang Y and Duan X F 2017 *Nano Lett.* **17** 5495
[48] Ma J, Yu Z G and Zhang Y W 2017 *Phys. Rev. B* **95** 165447
[49] Suh J, Park T, Lin D Y, Fu D, Park J, Jung H J, Chen Y, Ko C, Jang C, Sun Y, Sinclair R, Chang J, Tongay S and Wu J 2014 *Nano Lett.* **14** 6976
[50] Zhang K, Bersch B M, Joshi J, *et al.* 2018 *Adv. Funct. Mater.* **28** 1706950
[51] Chen C H, Wu C L, Pu J, Chiu M H, Kumar P, Takenobu T and Li L J 2014 *2D Mater.* **1** 034001
[52] Chang R J, Sheng Y, Ryu G H, Mkhize N, Chen T, Lu Y, Chen J, Lee J K, Bhaskaran H and Warner J H 2019 *ACS Appl. Mater. Interfaces* **11** 24279
[53] Fei W W, Trommer J, Lemme M C, Mikolajick T and Heinzig A 2022 *InfoMat* **4** e12355
[54] Yang S, Chen Y and Jiang C 2021 *InfoMat* **3** 397
[55] Wang J, Fang H, Wang X, Chen X, Lu W and Hu W 2017 *Small* **13** 1700894
[56] Geim A K and Novoselov K S 2007 *Nat. Mater.* **6** 183
[57] Novoselov K S, Geim A K, Morozov S V, Jiang D, Zhang Y, Dubonos S V, Grigorieva I V and Firsov A A 2004 *Science* **306** 666
[58] Xu Y J, Shi X Y, Zhang Y S, Zhang H T, Zhang Q L, Huang Z L, Xu X F, Guo J, Zhang H, Sun L T, Zeng Z M, Pan A L and Zhang K 2020 *Nat. Commun.* **11** 1330
[59] Tao L, Cinquanta E, Chiappe D, Grazianetti C, Fanciulli M, Dubey M, Molle A and Akinwande D 2015 *Nat. Nanotechnol.* **10** 227
[60] Madhushankar B N, Kaverzin A, Giousis T, *et al.* 2017 *2D Mater.* **4** 021009
[61] Qin F L, Hu Y X, Hu P A and Feng W 2020 *Nanotechnology* **31** 115204
[62] Golani P, Yun H, Ghosh S, Wen J, Mkhoyan K A and Koester S J 2020 *Nanotechnology* **31** 405203
[63] Bao W, Cai X, Kim D, Sridhara K and Fuhrer M S 2013 *Appl. Phys. Lett.* **102** 042104
[64] Zhang Y, Ye J, Matsuhashi Y and Iwasa Y 2012 *Nano Lett.* **12** 1136
[65] Braga D, Lezama I G, Berger H and Morpurgo A F 2012 *Nano Lett.* **12** 5218
[66] Jo S, Ubrig N, Berger H, Kuzmenko A B and Morpurgo A F 2014 *Nano Lett.* **14** 2019
[67] Pradhan N R, Garcia C, Isenberg B, *et al.* 2018 *Sci. Rep.* **8** 12745
[68] Gutierrez-Lezama I, Reddy B A, Ubrig N and Morpurgo A F 2016 *2D Mater.* **3** 045016
[69] Song H S, Li S L, Gao L, Xu Y, Ueno K, Tang J, Cheng Y B and Tsukagoshi K 2013 *Nanoscale* **5** 9666
[70] Jung C, Kim S M, Moon H, Han G, Kwon J, Hong Y K, Omkaram I, Yoon Y, Kim S and Park J 2015 *Sci. Rep.* **5** 15313
[71] Pradhan N R, Rhodes D, Xin Y, Memaran S, Bhaskaran L, Siddiq M, Hill S, Ajayan P M and Balicas L 2014 *ACS Nano* **8** 7923
[72] Das S and Appenzeller J 2013 *Appl. Phys. Lett.* **103** 103501
[73] Podzorov V, Gershenson M E, Kloc C, Zeis R and Bucher E 2004 *Appl. Phys. Lett.* **84** 3301
[74] Yu R, Sheng Z, Hu W N, Wang Y, Dong J G, Sun H R, Cheng Z G and Zhang Z X 2023 *Chin. Phys. B* **32** 018505
[75] Jiang W, Wang X, Chen Y, Wu G, Ba K, Xuan N, Sun Y, Gong P, Bao J, Shen H, Lin T, Meng X, Wang J and Sun Z 2019 *InfoMat* **1** 260
[76] Zhao Y D, Qiao J S, Yu Z H, Yu P, Xu K, Lau S P, Zhou W, Liu Z, Wang X R, Ji W and Chai Y 2017 *Adv. Mater.* **29** 1604230
[77] Chow W L, Yu P, Liu F C, *et al.* 2017 *Adv. Mater.* **29** 1602969
[78] Oyedele A D, Yang S, Liang L, *et al.* 2017 *J. Am. Chem. Soc.* **139** 14090
[79] Gu Y, Cai H, Dong J, *et al.* 2020 *Adv. Mater.* **32** 1906238
[80] Fathipour S, Ma N, Hwang W S, Protasenko V, Vishwanath S, Xing H G, Xu H, Jena D, Appenzeller J and Seabaugh A 2014 *Appl. Phys. Lett.* **105** 192101
[81] Lin Y F, Xu Y, Wang S T, Li S L, Yamamoto M, Aparecido-Ferreira A, Li W, Sun H, Nakaharai S, Jian W B, Ueno K and Tsukagoshi K 2014 *Adv. Mater.* **26** 3263
[82] Lee C S, Oh S J, Heo H, Seo S Y, Kim J, Kim Y H, Kim D, Okello O F N, Shin H, Sung J H, Choi S Y, Kim J S, Kim J K and Jo M H 2019 *Nano Lett.* **19** 1814
[83] Zhang E Z, Chen R, Huang C, Yu J H, Zhang K T, Wang W Y, Liu S S, Ling J W, Wan X G, Lu H Z and Xiu F X 2017 *Nano Lett.* **17** 878
[84] Uesugi E, Miao X, Ota H, Goto H and Kubozono Y 2017 *Phys. Rev. B* **95** 245310
[85] Yu P, Lin J H, Sun L F, *et al.* 2017 *Adv. Mater.* **29** 1603991
[86] Jiang J, Wong C P Y, Zou J, Li S, Wang Q, Chen J, Qi D, Wang H, Eda G, Chua D H C, Shi Y, Zhang W and Wee A T S 2017 *2D Mater.* **4** 021026
[87] Higashitarumizu N, Kawamoto H, Nakamura M, Shimamura K, Ohashi N, Ueno K and Nagashio K 2018 *Nanoscale* **10** 22474
[88] Lin C Y, Ulaganathan R K, Sankar R and Chou F C 2017 *AIP Adv.* **7** 075314
[89] Pan D, Fan D X, Kang N, Zhi J H, Yu X Z, Xu H Q and Zhao J H 2016 *Nano Lett.* **16** 834
[90] Cui F F, Zhao X X, Xu J J, Tang B, Shang Q Y, Shi J P, Huan Y H, Liao J H, Chen Q, Hou Y L, Zhang Q, Pennycook S J and Zhang Y F 2020 *Adv. Mater.* **32** 1905896
[91] Zhao M X, Xia W, Wang Y, Luo M, Tian Z, Guo Y F, Hu W D and Xue J M 2019 *ACS Nano* **13** 10705
[92] Kong D S, Chen Y L, Cha J J, *et al.* 2011 *Nat. Nanotechnol.* **6** 705
[93] Wang S, He C, Tang J, Lu X, Shen C, Yu H, Du L, Li J, Yang R, Shi D and Zhang G 2019 *Adv. Electron. Mater.* **5** 1800726
[94] Yao C, Wu G, Huang M, Wang W, Zhang C, Wu J, Liu H, Zheng B, Yi J, Zhu C, Tang Z, Wang Y, Huang M, Huang L, Li Z, Xiang L, Li D, Li S and Pan A 2023 *ACS Appl. Mater. Interfaces* **15** 23573
[95] Jiang Y, Zhang L, Wang R, Li H, Li L, Zhang S, Li X, Su J, Song X and Xia C 2022 *ACS Nano* **16** 11218
[96] Zhu W N, Yogeesh M N, Yang S X, Aldave S H, Kim J S, Sonde S, Tao L, Lu N S and Akinwande D 2015 *Nano Lett.* **15** 1883
[97] Li D, Wang B A, Chen M Y, Zhou J and Zhang Z X 2017 *Small* **13** 1603726
[98] Hu W, Liu Y, Huang Z, Dong J, Wang Y, Chen W, Sheng Z, Sun H, Hu G, Cong C, Zhang D W, Lu Y, Zhou P and Zhang Z 2023 *J. Phys. D: Appl. Phys.* **56** 355106
[99] Yu W J, Kim U J, Kang B R, Lee I H, Lee E H and Lee Y H 2009 *Nano Lett.* **9** 1401
[100] Das S, Demarteau M and Roelofs A 2014 *ACS Nano* **8** 11730
[101] Yao H, Wu E X and Liu J 2020 *Appl. Phys. Lett.* **117** 123103
[102] Lim J H, Shim J, Kang B S, Shin G, Kim H, Andreev M, Jung K S, Kim K H, Choi J W, Lee Y and Park I H 2019 *Adv. Funct. Mater.* **29** 1905540
[103] Geng G Y, Wu E X, Xu L Y, Hu X D, Miao X P, Zou J, Wu S, Liu J, Liu Y and He Z D 2022 *Nanotechnology* **33** 175704
[104] Lee M J, Kim T W, Park C Y, Lee K M, Taniguchi T, Watanabe K, Kim M G, Hwang D and Lee Y T 2023 *Nano-Micro Lett.* **15** 22

[105] Li T Y, Li X F, Tian M C, Hu Q L, Wang X, Li S C and Wu Y Q 2019 *Nanoscale* **11** 4701
[106] Baugher B W H, Churchill H O H, Yang Y F and Jarillo-Herrero P 2014 *Nat. Nanotechnol.* **9** 262
[107] Ross J S, Klement P, Jones A M, Ghimire N J, Yan J Q, Mandrus D G, Taniguchi T, Watanabe K, Kitamura K, Yao W, Cobden D H and Xu X D 2014 *Nat. Nanotechnol.* **9** 268
[108] Pospischil A, Furchi M M and Mueller T 2014 *Nat. Nanotechnol.* **9** 257
[109] Chen J W, Lo S T, Ho S C, *et al.* 2018 *Nat. Commun.* **9** 3143
[110] Wang Y R, Wang F, Wang Z X, Wang J J, Yang J, Yao Y Y, Li N N, Sendeku M G, Zhan X Y, Shan C X and He J 2021 *Nano Res.* **14** 4328
[111] Wu G J, Wang X D, Chen Y, *et al.* 2020 *Adv. Mater.* **32** 1907937
[112] Wu P, Reis D, Hu X B S and Appenzeller J 2021 *Nat. Electron.* **4** 45
[113] Zeng S, Liu C, Huang X, Tang Z, Liu L and Zhou P 2022 *Nat. Commun.* **13** 56
[114] Sun X X, Zhu C G, Yi J L, *et al.* 2022 *Nat. Electron.* **5** 752
[115] Gao S, Liu G, Yang H, Hu C, Chen Q, Gong G, Xue W, Yi X, Shang J and Li R W 2019 *ACS Nano* **13** 2634
[116] Wang C Y, Liang S J, Wang S, *et al.* 2020 *Sci. Adv.* **6** eaba6173
[117] Aftab S and Hegazy H H 2023 *Small* **19** 2205778
[118] Gong C, Zhang Y, Chen W, Chu J, Lei T, Pu J, Dai L, Wu C, Cheng Y, Zhai T, Li L and Xiong J 2017 *Adv. Sci.* **4** 1700231
[119] Lv Z, Zhou Y, Han S T and Roy V A L 2018 *Mater. Today* **21** 537
[120] Cheng Z, Rios C, Pernice W H P, Wright C D and Bhaskaran H 2017 *Sci. Adv.* **3** e1700160
[121] Ho V M, Lee J A and Martin K C 2011 *Science* **334** 623
[122] Martin S J, Grimwood P D and Morris R G M 2000 *Annu. Rev. Neurosci.* **23** 649
[123] Zhang L, Zhang P, Wang G, Zhang H, Zhang Y, Yu Y, Zhang M, Xiao J, Crespo P, Hell J W, Lin L, Huganir R L and Zhu J J 2018 *Neuron* **98** 783
[124] Gao J, Lian X, Chen Z X, Shi S, Li E L, Wang Y A, Jin T Y, Chen H P, Liu L, Chen J S, Zhu Y and Chen W 2022 *Adv. Funct. Mater.* **32** 2110415
[125] Sun Y, Li M, Ding Y, Wang H, Wang H, Chen Z and Xie D 2022 *InfoMat* **4** e12317
[126] Wan Q, Sharbati M T, Erickson J R, Du Y and Xiong F 2019 *Adv. Mater. Technol.* **4** 1900037
[127] Lee Y, Oh J Y, Xu W, Kim O, Kim T R, Kang J, Kim Y, Son D, Tok J B H, Park M J, Bao Z and Lee T W 2018 *Sci. Adv.* **4** eaat7387
[128] Romeira B, Javaloyes J, Ironside C N, Figueiredo J M L, Balle S and Piro O 2013 *Opt. Express* **21** 20931
[129] Wang H, Zhao Q, Ni Z, Li Q, Liu H, Yang Y, Wang L, Ran Y, Guo Y, Hu W and Liu Y 2018 *Adv. Mater.* **30** 1803961
[130] Shen Z J, Zhao C, Kang L X, Sun Y, Liu Y N, Mitrovic I Z, Yang L, Lim E G, Zeng Z M and Zhao C Z 2022 *Adv. Intell. Syst.* **4** 2100236
[131] Yoo C, Ko T J, Kaium M G, Martinez R, Islam M M, Li H, Kim J H, Cao J, Acharya M, Roy T and Jung Y 2022 *APL Mater.* **10** 070702
[132] Xia Z, Wang J and Fei Z 2019 *Phys. Status Solidi-Rapid Res. Lett.* **13** 1900082
[133] Nur R, Tsuchiya T, Toprasertpong K, Terabe K, Takagi S and Takenaka M 2022 *Nanoscale* **14** 2013
[134] Oh S, Lee J J, Seo S, Yoo G and Park J H 2021 *NPJ 2D Mater. Appl.* **5** 95
[135] Li R L, Wang W X, Li Y, Gao S, Yue W J and Shen G Z 2023 *Nano Energy* **111** 108398
[136] Kwon K C, Baek J H, Hong K, Kim S Y and Jang H W 2022 *Nano-Micro Lett.* **14** 58
[137] Xu M J, Xu T F, Yu A Q, *et al.* 2021 *Adv. Opt. Mater.* **9** 2100937
[138] Li D, Zhu C G, Liu H W, Sun X X, Zheng B Y, Liu Y, Liu Y, Wang X W, Zhu X L, Wang X and Pan A L 2020 *Sci. Bull.* **65** 293
[139] Zhu C G, Liu H W, Wang W Q, Xiang L, Jiang J, Shuai Q, Yang X, Zhang T, Zheng B Y, Wang H, Li D and Pan A L 2022 *Light-Sci. Appl.* **11** 337
[140] Sun X X, Zhu C G, Liu H W, Zheng B Y, Liu Y, Yi J L, Fang L Z, Liu Y, Wang X W, Zubair M, Zhu X L, Wang X, Li D and Pan A L 2020 *Sci. Bull.* **65** 2007
[141] Abdolrasol M G M, Hussain S M S, Ustun T S, *et al.* 2021 *Electronics* **10** 2689
[142] Yamashita R, Nishio M, Do R K G and Togashi K 2018 *Insights Imaging* **9** 611
[143] Kuzum D, Yu S M and Wong H S P 2013 *Nanotechnology* **24** 382001
[144] Tan H W, Liu G, Yang H L, Yi X H, Pan L, Shang J, Long S B, Liu M, Wu Y H and Li R W 2017 *ACS Nano* **11** 11298
[145] Luo Z D, Zhang S Q, Liu Y, Zhang D W, Gan X T, Seidel J, Liu Y, Han G Q, Alexe M and Hao Y 2022 *ACS Nano* **16** 3362
[146] Kim M K and Lee J S 2019 *Nano Lett.* **19** 2044
[147] Luo Z D, Xia X, Yang M M, Wilson N R, Gruverman A and Alexe M 2020 *ACS Nano* **14** 746
[148] Dong Z, Zhou Z, Li Z F, Liu C, Huang P, Liu L F, Liu X Y and Kang J F 2019 *IEEE Trans. Electron Devices* **66** 793
[149] Seo S, Jo S H, Kim S, Shim J, Oh S, Kim J H, Heo K, Choi J W, Choi C, Oh S, Kuzum D, Wong H S P and Park J H 2018 *Nat. Commun.* **9** 5106
[150] Pi L J, Wang P F, Liang S J, Luo P, Wang H Y, Li D Y, Li Z X, Chen P, Zhou X, Miao F and Zhai T Y 2022 *Nat. Electron.* **5** 248
[151] Jang H, Hinton H, Jung W B, Lee M H, Kim C, Park M, Lee S K, Park S and Ham D 2022 *Nat. Electron.* **5** 519
[152] Zhang Z H, Wang S Y, Liu C S, Xie R Z, Hu W D and Zhou P 2022 *Nat. Nanotechnol.* **17** 27
[153] Meng Y, Li F, Lan C, Bu X, Kang X, Wei R, Yip S, Li D, Wang F, Takahashi T, Hosomi T, Nagashima K, Yanagida T and Ho J C 2020 *Sci. Adv.* **6** eabc6389
[154] Choo K D, Xu L, Kim Y, Seol J H, Wu X, Sylvester D and Blaauw D 2019 *IEEE J. Solid-State Circuits* **54** 2921
[155] Wang Y, Sun H, Sheng Z, Dong J, Hu W, Tang D and Zhang Z 2023 *Nano Res.* **16** 12713
[156] Zhang X, Yu H, Tang W, Wei X, Gao L, Hong M, Liao Q, Kang Z, Zhang Z and Zhang Y 2022 *Adv. Mater.* **34** 2109521
[157] Sun Z, Pedretti G, Bricalli A and Ielmini D 2020 *Sci. Adv.* **6** eaay2378
[158] Wang R, Shi T, Zhang X, Wei J, Lu J, Zhu J, Wu Z, Liu Q and Liu M 2022 *Nat. Commun.* **13** 2289
[159] Wang C, Ruan G J, Yang Z Z, Yangdong X J, Li Y, Wu L, Ge Y, Zhao Y, Pan C, Wei W, Wang L B, Cheng B, Zhang Z, Zhang C, Liang S J and Miao F 2023 *Nat. Electron.* **6** 381
[160] Tang W, Zhang X, Yu H, Gao L, Zhang Q, Wei X, Hong M, Gu L, Liao Q, Kang Z, Zhang Z and Zhang Y 2022 *Small Methods* **6** 2101583
[161] Liu B, Zhang X, Du J, Xiao J, Yu H, Hong M, Gao L, Ou Y, Kang Z, Liao Q, Zhang Z and Zhang Y 2022 *InfoMat* **4** e12282
[162] Xiao J, Chen K, Zhang X, Liu X, Yu H, Gao L, Hong M, Gu L, Zhang Z and Zhang Y 2023 *Small Methods* 2300611
[163] Gao L, Zhang X, Yu H, Hong M, Wei X, Chen Z, Zhang Q, Liao Q, Zhang Z and Zhang Y 2023 *ACS Appl. Mater. Interfaces* **15** 38603
[164] Liu L, Kong L, Li Q, *et al.* 2021 *Nat. Electron.* **4** 342
[165] Wang L, Xu K, Cui W, Lv D, Wang L, Ren L, Xu X, Dong F, Dou S X, Hao W and Du Y 2019 *Adv. Funct. Mater.* **29** 1808084
[166] Zhang X, Zhang Y, Yu H, Zhao H, Cao Z, Zhang Z and Zhang Y 2023 *Adv. Mater.* 2207966
[167] Yao H, Guo X, Bao A, Mao H, Ma Y and Li X 2022 *Chin. Phys. B* **31** 038501
[168] Yan X, Zhang D W, Liu C, Bao W, Wang S, Ding S, Zheng G and Zhou P 2018 *Adv. Sci.* **5** 1700830
[169] Li K, Wang W, Du C, Gao H, Yin T and Yu Y 2022 *J. Materiomics* **8** 1158
[170] Acar M, Ertugrul M and Gur E 2022 *Nanotechnology* **33** 475201
[171] Bai Z, Xiao Y, Luo Q, Li M, Peng G, Zhu Z, Luo F, Zhu M, Qin S and Novoselov K 2022 *ACS Nano* **16** 7880
[172] Song Y, Li M, Chen J, Du Y, Qin Q, Du Z, Zou F, Ma X, Li L and Li G 2023 *ACS Appl. Electron. Mater.* **5** 2748
[173] Lei T, Tu H, Lv W, Ma H, Wang J, Hu R, Wang Q, Zhang L, Fang B, Liu Z, Shi W and Zeng Z 2021 *ACS Appl. Mater. Interfaces* **13** 50213
[174] Zhang T, Liu Y, Wang F, Pan X and Ye Z 2023 *Adv. Electron. Mater.* **9** 2201203