

Ferroelectric domain wall memory

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Citation: Chin. Phys. B, 2023, 32 (**12**): 128504. DOI: 10.1088/1674-1056/ace4b6
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TOPICAL REVIEW — Post-Moore era: Materials and device physics

Ferroelectric domain wall memory

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(Received 11 May 2023; revised manuscript received 6 July 2023; accepted manuscript online 6 July 2023)

Ferroelectric domain walls appear as sub-nanometer-thick topological interfaces separating two adjacent domains in different orientations, and can be repetitively created, erased, and moved during programming into different logic states for the nonvolatile memory under an applied electric field, providing a new paradigm for highly miniaturized low-energy electronic devices. Under some specific conditions, the charged domain walls are conducting, differing from their insulating bulk domains. In the past decade, the emergence of atomic-layer scaling solid-state electronic devices is such demonstration, resulting in the rapid rise of domain wall nano-electronics. This review aims to the latest development of ferroelectric domain-wall memories with the presence of the challenges and opportunities and the roadmap to their future commercialization.

Keywords: domain wall, memory, ferroelectric

PACS: 85.50.–n, 72.20.–i, 77.80.–e, 77.84.–s **DOI:** 10.1088/1674-1056/ace4b6

1. Introduction

A wealth of phenomena have been emerging at the interfaces of ferroelectric hetero-oxides due to their distinct performance from bulk materials, providing broad prospects for basic research and application in the fields such as electromagnetism and optics, which was described as Kroemer's well-known saying "The interface is the device".[1–5] The interfaces separating different polarizations in ferroelectric homo-oxides are domain walls (DWs) that appear as two-dimensional topological defects with a width of approximately 1 nm–10 nm.[6] The DWs have changed spatial symmetry and band structure,[7–9] and are rich with mobile defects,[10–12] resulting in new functional properties including optical,[13–15] electrical,[16–22] and magnetic[23–26] properties that do not exist in the bulk. The emerging functionalities lead to the worldwide exploration of new DW nanodevices and their applications.[27–32]

Racetrack memory based on moving magnetic DWs driven by a magnetic or an electric field has attracted widespread attention in recent years, where nonvolatile data storage and computation can be achieved by controlling the injection, motion and erasure of magnetic DWs.[33–36] Identically, ferroelectric DWs can also be operated in a similar way by an applied electric field as needed.[37–40] Typically, ferroelectric DWs are one to two orders of magnitude narrower than that of magnetic DWs,[6,41] providing significant advantage in the device scalability and low energy consumption. However, as shown in Fig. 1, research in the field of ferroelectric DWs has been progressing slowly for the past decades until the turn of this century, when various electronic nanodevices have been successfully implemented and demonstrated for their potential applications, especially for nonvolatile memories with non-destructive operations and ultra-low energy consumption. These memories are superior to other transitional metal oxide-based resistance random access memories (RRAMs) in better reliability.

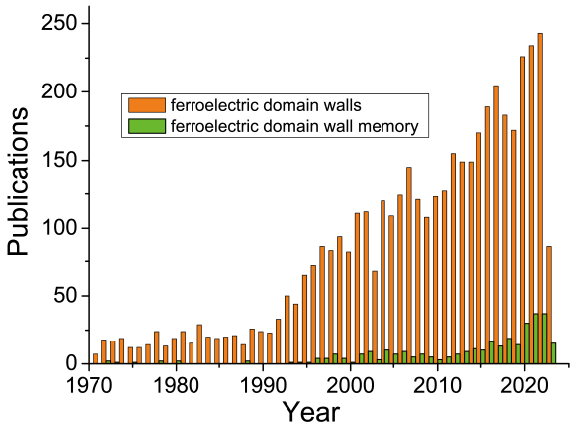


Fig. 1. Annual publications on ferroelectric DWs since the 1970s (SEARCH KEY: TITLE-ABS-KEY (ferroelectric domain walls); source: SCOPUS).

In the past ten years, various prototype DW memory devices have been demonstrated with capacitor geometries as shown in Fig. 2, which have coplanar electrodes,[42–46] nanoislands,[47–49] mesa-type cells,[50–53] and parallel-plate like capacitors in the top and bottom electrodes[54–59] among $BiFeO_3$ (BFO), $LiNbO_3$ (LNO), $BaTiO_3$ (BTO) epitaxial thin films, etc. In this article, we classify such novel DW memories with the brief discussion of their working principles, cell structures, performance, and the prospects in the future.

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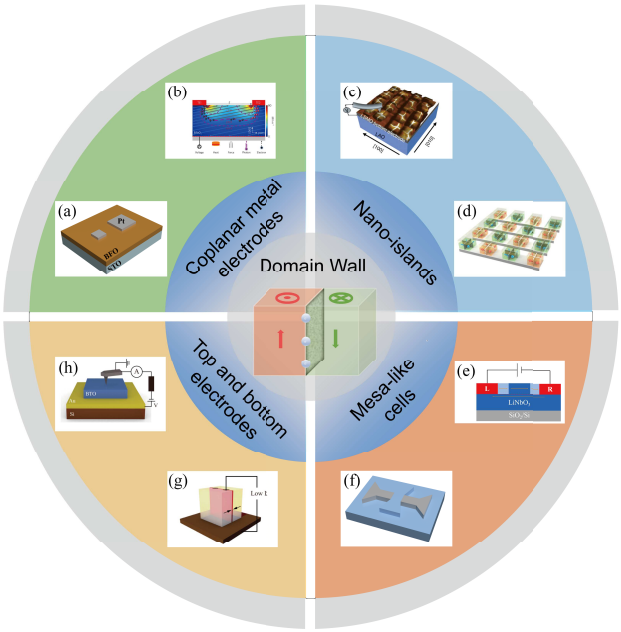


Fig. 2. DW memories in various structures: (a) and (b) DW memories with coplanar electrodes. Reproduced with permission from Ref. [43] (Copyright 2017, Springer *Nature*). (c) and (d) DW memory in nano-islands. Reproduced with permission from Ref. [47] (Copyright 2018, Springer *Nature*). (e) and (f) Planar mesa-type DW memory. (g) and (h) Out-of-plane DW memory with top and bottom electrodes. Reproduced with permission from Ref. [59] (Copyright 2022, Springer *Nature*).

2. Prototype DW memory devices

2.1. DW memories with coplanar electrodes

Since conducting ferroelectric DWs were found to be useful in ferroelectric memories in 2009,[18] a decade has passed over the fabrication and demonstration of solid-state prototype devices through the precise injection and control of reconfigurable DWs.[60] Among these works, Seidel *et al.* firstly implemented coplanar metal electrodes fabricated at the nanoscale on the surface of a $BiFeO_3$ (BFO) thin film. The programming of data is based on the creation and erasure of conductive DWs via the hierarchical evolution of the 71°, 109°, and 180° domains within the interspace.[42] Figure 3(a) shows a typical structure of the memory. When an electric field is applied to two top electrodes, DWs can be written or deleted via the repetitive inversion of the interdomains (the storage cell) in contrast to the peripheral unswitched domains in the generation of low and high resistance states. The two states encode logic 1 (on state) and 0 (off state) information, respectively. After removal of the applied field, the on/off states can persist stably over retention time and can be discerned under the application of a smaller read voltage less than the coercive voltage of domain switching. At the early stage of the research, the DW currents are stable over a retention time more than several hours in an on/off ratio exceeding 10^3 at 2 V and endurance cycles of more than 10^3. The main challenge of the application is the deposition of an epitaxial ferroelectric thin film on the large-area Si wafer in a single domain pattern.

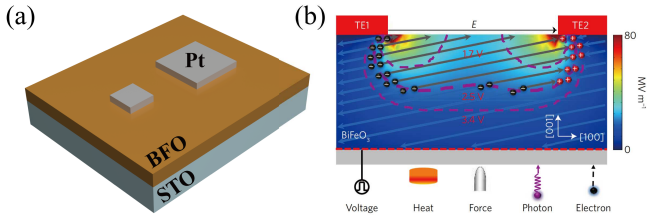


Fig. 3. The working principle of DW memory with coplanar electrodes: (a) typical structure of the prototype device, (b) creation of charged DWs on a $BiFeO_3$ thin film. Reproduced with permission from Ref. [43] (Copyright 2017, Springer *Nature*).

To overcome this shortcoming, Jiang *et al.* sought for non-destructive readout method of the memory using the coplanar electrodes integrated on the BFO surface. The coplanar electrodes were fabricated by electron-beam lithography (EBL) and physical vapor deposition (PVD), and the BFO thin films were deposited by pulsed laser deposition (PLD) in multidomain patterns.[43] The multidomains within each cell can be polarized into a single domain after a write operation, and the written polarization direction can be read out through on/off currents generated between two coplanar electrodes deposited at the top of each cell upon interdomain inversion at a small applied voltage. Figure 3(b) shows the cell structure and creation of charged domain walls (CDWs) during reading. They find that the coercive voltage (DW current) decreased (increased) with the shortened gap distance between two coplanar electrodes, and the maximum DW current can highly reach 14 nA, i.e., the current density of about 0.028 μA/μm, enabling fast operation speeds (about 100 ns at 4 V) and high endurance cycles ($\sim 10^7$). However, the read current of 14 nA is still far from the demand of driving high-speed circuits (1 μA–10 μA). Later, they wisely construct a head-to-head (H–H) DW by changing the relative direction of the initial polarization against the applied field at the angle of $\alpha = 90°$, where a read current can significantly increase to 300 nA (the current density of 2 μA/μm) in comparison to 1 nA–8 nA of the formed neutral domain wall (NDW) when $\alpha = 0°$.[44] The angular dependence of the wall current can be understood from the carrier transport across the n-type channel of the head-to-head wall with the projected domain boundary charge of $2P\sin\alpha$, where P is the spontaneous polarization. After lowering of the oxygen vacancy content through thermal annealing of BFO thin films at the oxygen atmosphere, the current density can be further increased up to 11 μA/μm.[45] The achievement is unprecedented and promotes the development of high-power DW nanodevices, especially for ultra-high density ferroelectric memories.

Though the coplanar DW memory has a big step forward the increase of the wall current, there is a problem regarding to the depolarization field that may reduce retention time. Generally, a higher operating voltage can achieve a longer retention time, which may contradict the requirements of low power

consumption and high reliability of the memory at low operation voltages. This could be correlated with charge injection and defect histories of the film. For example, though the conductive DWs in BFO show an interest in high-density logic or data storage, significant changes occur in the striped domains within the BFO films where the inverted polarization is instable without specific defect pinning,[61–63] in contrast to the highly stable conductive DWs observed in hexagonal manganites that are hardly manipulated.[64,65] In addition, the coplanar electrode configuration of the devices generally has low density integration, while vertical structures are highly preferred for high-density integration in the future, including ferroelectric random-access memory (FRAM) and resistance random-access memory (RRAM).[48] In this sense, controllable conductive DWs with topological protection have the advantage for realization of the 3D integration.

2.2. DW memory in nanoislands

With the discovery of new physical phenomena and functions in ferrous topological domain structures including vortex and skyrmion, electrical conduction in a low dimension caused by topological defects such as polarized DWs and vortex centers, as well as the field modulated magnetic skyrmion in multiferro nanostructures tackle new topological electronic devices.[66–70] The big achievement by Ma *et al.* is the fabrication of self-assembled ferroelectric BFO nanoisland arrays in a large area and high density, as shown in Fig. 4(a).[47] The cross-shaped DWs are topologically constrained due to the electrostatic and geometric boundary conditions of four polarization vectors pointing towards or away from the center and can be used for the binary information storage: the two stable center-convergent and center-divergent structures of vertex-like domain are switched reversibly under an applied electric field, changing the conductivity of confined DWs by three orders of magnitude, and the written DWs remain unchanged for several months. For the massive production, a schematic of envisaged cross-bar memory arrays was proposed, which can achieve high storage density by reducing the lateral sizes of the islands, as shown in Fig. 4(b).

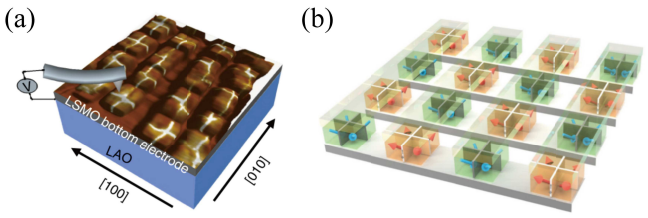


Fig. 4. DW memory in nanoislands: (a) a sketch of the BFO nanoislands on (La, Sr)MnO_3 (LSMO) buffered $LaAlO_3$ (LAO) substrates and (b) conceptual cross-bar memory. Reproduced with permission from Ref. [47] (Copyright 2018, Springer *Nature*).

Similarly, Gao *et al.* fabricated large arrays of BFO nanoislands using polystyrene nano-sphere templates, where DWs in different conductivities were measured via the conductive atomic force microscopy (c-AFM).[48] The H–H CDWs show a remarkably high current in the order of nA characteristic of the quasi-two-dimensional electron gas, while the NDW current is two orders lower ($\sim$ 10 pA). All currents show the thermally activated conduction behavior. Electrical regulations under different applied scanning bias voltages allow various types of DWs in distinct conductivities. Subsequently, they proposed a scheme to improve the performance of the DW memory by configuring complex topological domain structures through coaxial electrodes.[49] Different from nano-islands, ring-shaped electrodes are introduced onto BFO films for better creation and confinement of topological domain structures. The reciprocating switching of two topological states 0 and 1 is achieved stably with a high on/off ratio above 10^4 and a read current of 40 nA. More importantly, the prime endurance performance of more than 10^8 cycles is achieved due to the confined domains in the topological structure, which has been setting up a new pathway for the integration of multilevel DW memory devices in ultra-high density, especially for the compatibility of crossbar arrays integrated into a vertical structure. However, the readout current ranging from pA to tens of nA is still insufficient to drive high-speed memory circuits according to the Johnson–Nyquist limit.[71,72] Therefore, it is crucial to develop new materials and structures to increase the wall current further.

2.3. Planar mesa-type DW memory

Commercial FRAM uses electrically switchable bistable polarizations in ferroelectric materials for digital data storage, while its read principle is based on charge integration resulting in a limited storage density.[73] For the integration of high-density memories, the traditional crossbar scheme is used, where discrete transistors or bipolar selectors are needed in serial connection with each cell to reduce the leakage current from neighboring cells. This arouses the burden of the cost and reliability.[74,75] Fortunately, the unipolar DW currents may provide a good solution to this problem. Jiang *et al.* fabricated mesa-type DW cells on the surface of single-crystal $LiNbO_3$ (LNO) thin films.[50] The thin film has a single domain pattern and can be peeled off a LNO single crystal after ion implantation and bonded to the large-area SiO_2/Si wafers (LOI) for mass production. Figures 5(a) and 5(b) show the working principle of the mesa-like cells. For each LNO cell, there are two kinds of domains, and the interfacial domains near two side electrodes are volatile and can serve as an embedded selector to rectify a unipolar DW current, unlike the inner domains that are nonvolatile for information storage. Once the interface layer is removed, the embedded selectors will no longer exist, resulting in bidirectional conduction of DW current, as shown in Fig. 5(b). The interfacial layers ap-

pear to be universal in ferroelectrics due to the polarization termination. With the creation and erasure of intrinsic non-volatile inner DWs and volatile interfacial DWs independently, a diode-like DW memory exhibits a high on/off ratio over 10^6, endurance cycling number up to 10^{10}, and the current density of up to 90 μA/μm, illustrating the possibility for the commercialization of DW memories in the near future.

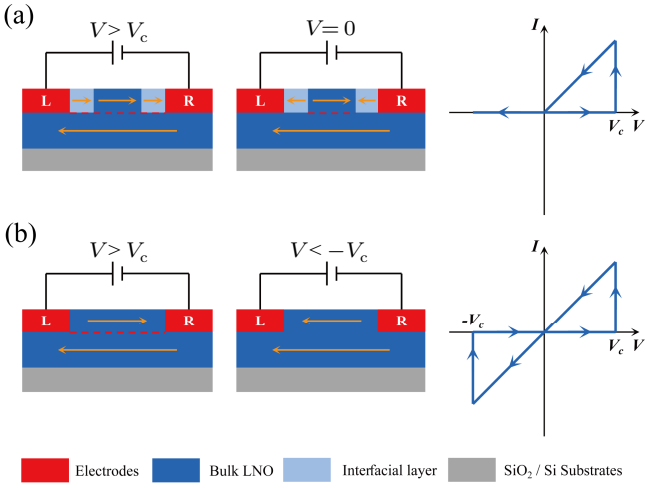


Fig. 5. The working principle of DW memory in mesa-like cells. (a) Structure and current–voltage (I–V) curves of DW memories with interfacial layers, where V is the applied voltage and V_c is the coercive voltage. (b) Structure and I–V curves of ideal DW memories without interfacial layers. The conductive DWs are shown in dashed red lines.

The mesa-like memory also has good scalability. Lian *et al.* fabricated 15 nm-sized LNO cells using the same fabrication technologies, and found that the onset voltages decreased almost linearly with the shrinking cell size due to the thinner interfacial layer, in contrast to the DW current that increased 25 times than that of a 106 nm-sized cell.[51] The memory has nanosecond operation speeds (5 ns at 4 V) after the optimization of the LNO etching process. For the improvement, Ao *et al.* invented a new etching technology of the LNO using CMOS-compatible SiO_2 masks, which can maintain high-precision fidelity of patterns in promoting massive production of LNO memories on the Si substrates.[76] The improved manufacturing process in high reliability is foreseeable during tailoring dual functions of storage and selector with an adjustable onset voltage. During the cell scaling study, Hu *et al.* found the existence of a critical size depending on the strain mismatching between the LNO film and the substrate, leading to higher readout wall current and good polarization retention.[77] Finally, Zhang *et al.* demonstrated a 4×4 crossbar array on LNO single crystal substrates, where the embedded selector allows read and write operations unaffected by the crosstalk problem.[78] Theoretically, the cell size can be reduced to the order of the DW thickness that generally does not exceed 1 nm, demonstrating the high-density integration using the standard CMOS processes.

Different types of DWs can be created with manipulated inclined angles, leading to various conductions of DW currents. Chai *et al.* found that electrical conductivity across the H–H DW is more than 4 orders of magnitude higher than that across the T–T DW, which is attractive for the fabrication of high-power nanodevices.[79] Wang *et al.* could lower the DW current during the write by creating the NDW and increase the DW current during the read by creating the H–H CDW, thereby meeting the low power consumption requirements of the DW memory.[80] With the controlled DW angle α with respect to the surface in off-X-cut LNO substrates, Sun *et al.* created H–H CDWs and found the huge DW current density higher than 1 mA/μm when $\alpha = 15°$, which is 3–4 orders of magnitude higher than that of the tail-to-tail DW.[53] The off-X-cut cells not only enable a fast speed operation of high density non-volatile DW memories with low energy consumption, but also serve as a high power half wave rectifier in modern nanocircuits. Another key concern is the performance of the DW memories at high temperature of 450 K that maintain a large on/off current ratio of $\sim 10^4$ without obvious degradation with respect to retention time, attractive for automotive and space applications under some extremely harsh conditions.[81]

2.4. Out-of-plane DW memory with top and bottom electrodes

Since the discovery of conductive DWs, the parallel-plate capacitor-like structure is firstly proposed, as shown in Fig. 6(a).[60] Schröder *et al.* investigated the conductive DWs in LNO single crystals coated with Cr/Au bottom electrodes, where a Pt-coated c-AFM tip worked as a movable top electrode.[82] They created conductive DWs within millimeter-thick single crystals, where the DW current can be regulated through super-bandgap illumination and DW inclination at off-axis angles between DWs and polarization. Thereafter, the on/off states of the memories were successfully deployed.[55–58,60] McConville *et al.* even developed multi-level ferroelectric DW memristors using LNO thin films under controlling of the inclined angles of conducting DWs, where the resistance spanning over twelve orders of magnitude at various write voltages was realized, as shown in Fig. 6(b).[55] However, the write voltage for the injection and annihilation of the DWs is too high (up to 40 V) to meet the demand of low-power applications. Therefore, Chaudhary *et al.* explored the modulation of conductance via sub-coercive voltages from −3 V to 8 V.[56] With a poly-domain structure created by a super-coercive bias firstly, distinct voltage pulses with various amplitudes and widths were applied without changing the generated domain structure, leading to the electrically induced DW bending[57] and modulated the resistance spanning 1–2 orders of magnitude, as shown in Fig. 6(c). However, the tunable voltages (up to 33 V) are still too high to generate

poly-domain structure and require the reduction in the future, besides the stabilization of poly-domain and metastable conductance for the achievement of long-term retention.

Though the LOI has been proven to be feasible with CMOS-based integration technology, more studies should be given for the deposition of other epitaxial ferroelectric thin films on the Si substrates. DW memories integrated with the silicon have emerged for industrial and commercial applications. As a first step effort, Sun *et al.* synthesized high-quality self-supporting BTO thin films on $Sr_3Al_2O_6/SrTiO_3$ substrates, and the BTO was later transferred onto the Si substrate after desolving the $Sr_3Al_2O_6$ buffer layer in water.[59] Completely different from the out-of-plane single domain polarization when constrained by the substrate, the BTO film integrated on the Si substrate shows in-plane ferroelectric polarization due to the synergistic effect of strain relaxation and depolarizing field during transferring, offering an optimized way to create and regulate conductive DWs. With top and bottom electrodes prepared based on the BTO/Si heterojunction, H–H DWs with high conductivity ($\sim$ nA) can be generated and erased via a scanning probe, as shown in Fig. 6(d), advancing the DW memory integration on Si.

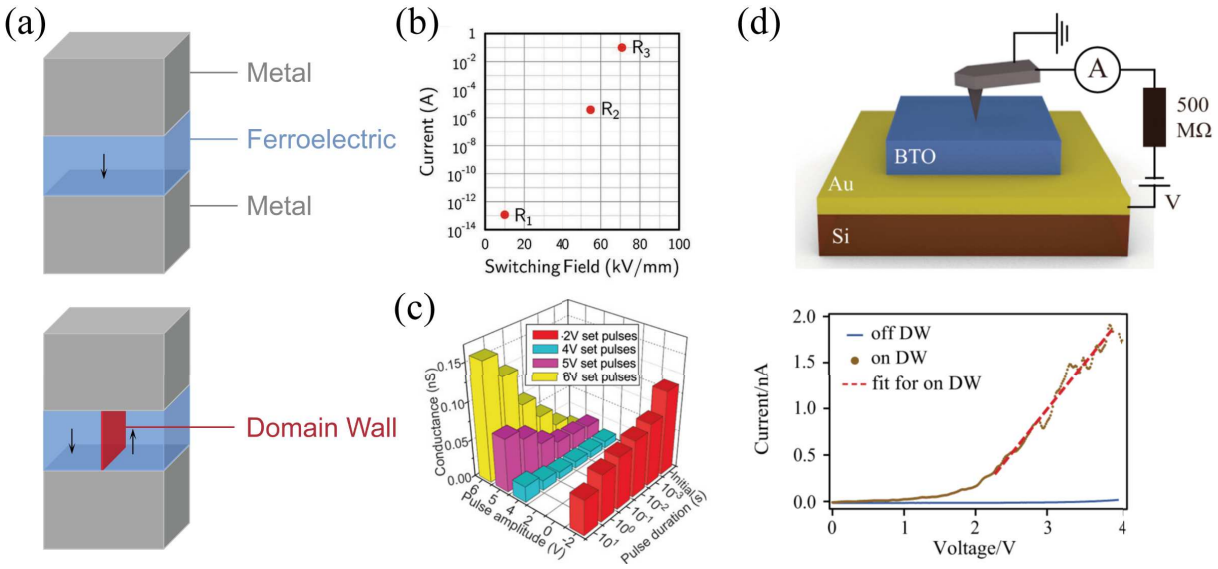


Fig. 6. Out-of-plane DW memory with top and bottom electrodes. (a) Conceptual diagram of a capacitor-like DW memory with a ferroelectric layer between metal electrodes. (b) Distinct resistances under various applied switching voltages. Reproduced with permission from Ref. [55] (Copyright 2020, John Wiley & Sons). (c) Conductance modulated by pulse amplitude and duration. Reproduced with permission from Ref. [56] (Copyright 2020, *Am. Chem. Soc.*). (d) Typical structure of device and measured *I*–*V* curves. Reproduced with permission from Ref. [59] (Copyright 2022, Springer *Nature*).

3. Discussion

In the past decade or so, ferroelectric DW memories have exhibited the prosperity with the development of various prototype devices. Among these efforts, researchers pay more attention to the cell structure and performance, including precise control of DW positions, large readout currents with high on/off ratios, cell scalability and compatibility with the CMOS technologies, and so on. However, there are still other urgent issues required to be addressed before the commercialization, mainly given as follows.

Endurance and retention Although the LNO mesa-like DW memory has exhibited switching endurance of 10^{10} cycles at room temperature,[50] it is still insufficient to meet the commercialization requirement of 10^{13} to 10^{17} cycles in contrast to the FRAM and DRAM over a wide temperature range (-40 °C to 85 °C). Therefore, further improvement in the endurance at different temperatures is needed. The strategy to enhance the endurance cycles may reduce the coercive field of DW memories and mitigate charge injection at high electric fields through the selection of suitable electrode materials and decoration of interfacial layers. In addition, the poor retention for DW memories either with planar electrodes or with top and bottom electrodes are also an obstacle, especially for nonvolatile in-memory computing.

High DW current at a low read voltage Firstly, the driving of high-speed circuits in ns–ps timescale requires a large read current ($>$ 10 μA) due to the Johnson–Nyquist limit, while most of present works are in the orders of about $\sim$ nA or $\sim$ pA apart from BFO and LNO, and a small read voltage and a large μA current are needed in consideration of efficient energy consumption and cost savings. In addition, the high DW current in LNO was most found within the H–H DW at present, where the high depolarization energy could destabilize the switched domains, leading to the limited retention time and the worsened reliability of DW devices.[53,79] With the advanced modern microelectronic technology, the scalability of the devices is critically important, since the smaller device can have a lower operation voltage and higher integration density. Therefore, an approach is needed to resolve the

dilemma of high readout DW current realized at a small read voltage. One possible approach is to increase the DW conductivity, such as through the adjustment of the DW inclination angle, which has been proven to be effective within off-X-cut LNO memory cells.[75,83] In addition, improving the fabrication process to minimize the number of defects that affect the coercive field of materials is also beneficial for the achievement of a low voltage operation. Presently, the operating time of mesa-like LNO memories can be lower than 5 ns, and the estimated power consumption can reach 10 fJ per bit with a wall current of ~ 1 μA at a write voltage of 1 V–3 V.[44]

Compatibility with the standard CMOS process Though extensive research has been conducted on ferroelectric DW memories with various materials and structures, it is insufficient to meet the need of practical applications using the CMOS fabrication technologies due to the incompatibility, despite their promising performance using individual academic facilities, which has become a top concern limiting the further development of ferroelectric materials based solid-state electronic devices towards commercialization and industrialization.[84] For example, the growth temperature of BFO thin film is relatively high (~ 650), resulting in the compatibility issue with the Si back-of-end process residing in the back channels. Besides, the polycrystalline BFO thin film has multidomains that are harmful to the stability of DWs as well as the uniformity of high-density cells. Although BTO has shown excellent ferroelectric properties and has the potential to be integrated with CMOS technology, the limited readout current ($\sim$ nA) indicates that there is still a long way to go. Similarly, other perovskite oxides also have the same problem to be integrated with Si in high quality, due to the high deposition temperature and oxidation growing environment that may oxidize the surface of Si wafer. It is worth mentioning that LNO has good reputation as optical silicon, and a LNO single crystal film can be exfoliated from the surfaces via ionic implantation and chemically bonded to SiO_2/Si wafers, of which the batch production in 8 inch-sized wafers has been realized, promising the prospects for further applications. Different from multidomain BFO thin films, a monoclinic LNO single crystal film has a single domain pattern that is convenient for precise regulation of the DWs. Apart from the outstanding performance in DW memories, other excellent optical properties of LNO are also attracting considerable attention in wider applications such as sensors and electro-optic modulators.[85]

4. Outlook

Besides the demonstration of ferroelectric DW memories, further excavation in DW based nanodevices is required to deal with the growing performance gap between the central processing unit and the computer memory in traditional von Neumann architecture, the so-called memory wall.[86] A notable step is the development of logic-in-memory DW devices. Although DW logic has been proposed in nanomagnetic materials recently, where logic and cascading functions have been exhibited by current-driven DWs,[25] it is still challenging for the implementation of similar functions using a ferroelectric DW logic before several critical issues are considered: independent regulation of each CDW in the integrated CDW network[87] and low threshold losses when cascading various logic gates.[88] There have appeared some solutions in the literature. For example, the precise control of DWs can be realized via the confinement of topological domains, which has been proven feasible for ferroelectric DW logic.[87] Alternative optoelectronics engineering including laser-writing technique may provide a new way of DW manipulation at the nanoscale.[89] To reduce the latent threshold losses of logic gates, the further increase of readout currents of DWs is needed through the optimization of DW inclined angles. Nowadays, multi-bit nonvolatile DW memories can be used for brain-inspired neuromorphic computing that can break through the limitations of memory wall, and frontier researches based on DWs are burgeoning.[52,55,56] All in all, research focusing on DW nanoelectronics has been flourishing with the emergence of new devices in manifold structures and functions.[90–92] Apart from DW memories, new challenges and opportunities coexist, and more in-depth research of the DW physics is required in steering the direction of the new device development during their rapid expansion.

Acknowledgments

Project supported by the National Key Basic Research Program of China (Grant Nos. 2019YFA0308500 and 2022YFA1402900) and the National Natural Science Foundation of China (Grant No. 61904034).

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