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Improving dynamic characteristics for IGBTs by using interleaved trench gate

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A novel trench insulated gate bipolar transistor (IGBT) with improved dynamic characteristics is proposed and investigated. The poly gate and poly emitter of the proposed IGBT are arranged alternately along the trench. A self-biased p-MOSFET is formed on the emitter side. Owing to this unique three-dimensional (3D) trench architecture, both the turn-off characteristic and the turn-on characteristic can be greatly improved. At the turn-off moment, the maximum electric field and impact ionization rate of the proposed IGBT decrease and the dynamic avalanche (DA) is suppressed. Comparing with the carrier-stored trench gate bipolar transistor (CSTBT), the turn-off loss ($E_{\rm off}$) of the proposed IGBT also decreases by 31% at the same ON-state voltage. At the turn-on moment, the built-in p-MOSFET reduces the reverse displacement current ($I_{\rm G_dis}$), which is conducive to lowing $\mathrm{d}I_{\rm C}/\mathrm{d}t$. As a result, compared with the CSTBT with the same turn-on loss ($E_{\rm on}$), at $I_{\rm C} = 20$ A/cm^2, the proposed IGBT decreases by 35% of collector surge current ($I_{\rm surge}$) and 52% of $\mathrm{d}I_{\rm C}/\mathrm{d}t$.

Keywords: insulated gate bipolar transistor (IGBT), dynamic avalanche (DA), $\mathrm{d}I_{\rm C}/\mathrm{d}t$

PACS: 85.30.De, 85.30.Tv, 85.30.Pq **DOI:** 10.1088/1674-1056/ace15d

1. Introduction

Insulated gate bipolar transistors (IGBTs) are widely used in medium- and high-voltage power applications, such as smart grid, industrial motor drives, automotive, *etc*.[1–3] In order to improve the trade-off between ON-state voltage drop ($V_{\rm on}$) and turn-off loss ($E_{\rm off}$), many techniques have been proposed, such as field stop IGBT (FS-IGBT),[4] injection enhanced gate transistor (IEGT),[5–7] carrier stored trench-gate bipolar transistor (CSTBT),[8–10] super junction (SJ) trench IGBT.[11,12] With the decrease of turn-off loss, IGBTs are increasingly used in high frequency applications. However, high frequency is accompanied by high $\mathrm{d}V/\mathrm{d}t$, which can induce voltage overshoot and dynamic avalanche (DA) during turn-off.[13] The trench clustered IGBT (TCIGBT) structure has been proposed to eliminate DA by using a self-biased built-in p-MOSFET to divert the hole current.[14,15] Besides, high switching frequency can also lead to high $\mathrm{d}I_{\rm C}/\mathrm{d}t$.[16] To suppress $\mathrm{d}I_{\rm C}/\mathrm{d}t$ without sacrificing the turn-on loss, some IGBTs with unique gate geometry were proposed, such as the split-gate IGBT[17,18] and the fin p-body IGBT.[19] Furthermore, clamping the floating p-body adjacent to the trench gate also helps improve the trade-off relationship between $\mathrm{d}I_{\rm C}/\mathrm{d}t$ and $E_{\rm on}$.[20,21]

In this work, a novel trench-gate IGBT is proposed to obtain better switching characteristics. The proposed IGBT features a split-gate architecture. The poly gate and poly emitter are alternately arranged along the trench. Some paralleled self-biased p-MOSFETs are formed on the emitter side. During turn-off operation, the p-MOSFET turns on adaptively and provides an additional path for the hole current. The maximum electric field and impact ionization rate decrease greatly, thereby improving the ability to withstand the dynamic avalanche. During turn-on operation, the potential of the p-ring region below the trench gate is clamped. This can reduce the self-charging displacement current ($I_{\rm G_dis}$) of the gate capacitor and the $\mathrm{d}I_{\rm C}/\mathrm{d}t$ as well. Moreover, the interleaved gate architecture can reach a 67% reduction in Miller capacitance and a 34% increase in input capacitance, leading the turn-off loss to decrease and $\mathrm{d}I_{\rm C}/\mathrm{d}t$ to lower.

2. Device structure and mechanism

Figure 1(a) shows the schematic diagram of the proposed IGT IGBT. The poly gate and poly emitter are alternately arranged in the trench along the z direction as shown in Fig. 1(b). Figure 1(c) shows the built-in p-MOSFET, which is composed of the p-body, n-CS layer, p-ring region, and trench emitter. The source region of p-MOSFET is the p-ring region. The p-channel is the n-CS layer. The gate and the drain of the p-MOSFET are both grounded. Figure 1(d) shows cross-section of the IGT IGBT along the cutline along BB′. Figure 2 shows the conventional CSTBT and the p-ring IGBT.[22,23] The key parameters of three IGBT structures are listed in Table 1. The models used in simulations include Philips unified mobility model, high-field saturation model, Enormal model, Slotboom model, Shockley–Read–Hall model, Auger model, and Lackner's avalanche generation model.

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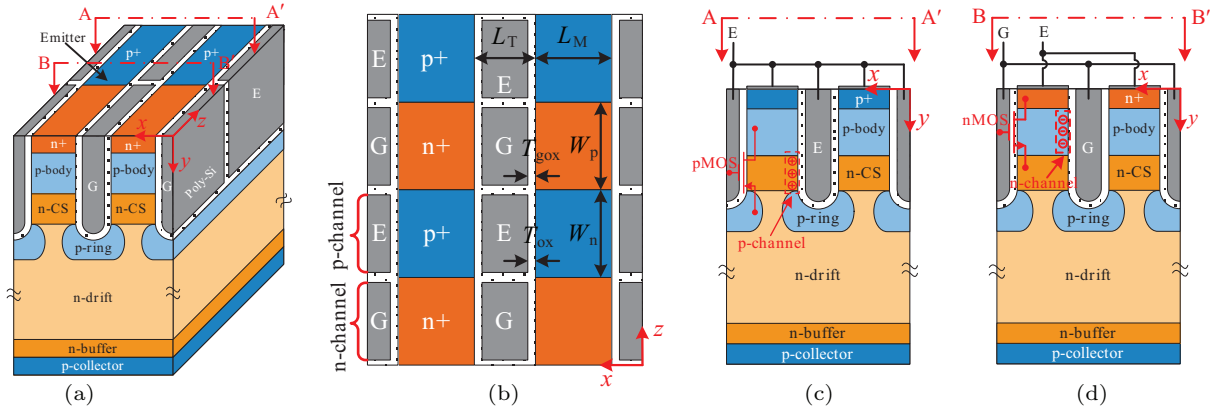


Fig. 1. (a) Schematic diagram of proposed IGT IGBT, (b) top view of IGT IGBT, (c) cross-section along cutline AA′, and (d) cross-section along cutline BB′.

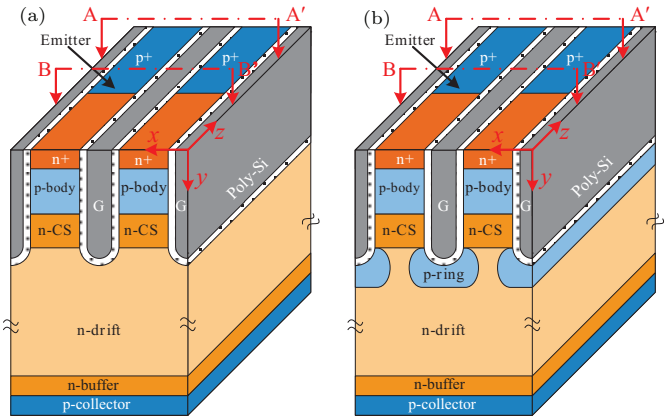


Fig. 2. Schematic diagram of (a) CSTBT and (b) p-ring IGBT.

Table 1. Device parameters.

Parameters	CSTBT	p-ring	IGT
Cell pitch L_C (μm)	6	6	6
Mesa width L_M (μm)	4	4	4
Trench width L_T (μm)	2	2	2
p-ring spacing (μm)		1.5	1.5
Trench depth (μm)	6	6	6
W_p/W_n (μm)	1.5/1.5	1.5/1.5	1.5/1.5
Gate oxide T_{gox} (μm)	0.1	0.1	0.1
p-body doping (cm^{-3})	2×10^{17}	2×10^{17}	2×10^{17}
n-CS doping N_{CS} (cm^{-3})	1×10^{15}	3.5×10^{16}	6×10^{16}
n-CS thickness (μm)	2	2	2
Substrate doping/thickness	8×10^{13}/112	8×10^{13}/112	8×10^{13}/112
n-buffer doping/thickness	2×10^{16}/1	2×10^{16}/1	2×10^{16}/1
p-collector doping/thickness	1×10^{17}/0.5	1×10^{17}/0.5	1×10^{17}/0.5
Carrier lifetime (μs)	1	1	1

Figure 3(a) shows the *BV* characteristic curves of three IGBT structures. The *BV* values of all three devices reach values higher than 1300 V.

The inset in Fig. 3(a) shows the electric field distributions of the three devices at breakdown. Figure 3(b) compares the curves of leakage current (I_L) versus temperature of three IGBT structures. And the leakage current for the IGT IGBT is almost similar to that for the CSTBT and p-ring IGBT.

Figure 4(a) shows the curves of *BV* and V_{on} versus N_{CS} for three IGBT structures. The *BV* of CSTBT is lower than 1300 V when N_{CS} is higher than 1.0×10^{15} cm^{-3}. Compared with the CSTBT, both the p-ring IGBT and the IGT IGBT can increase doping concentration of the n-CS layer (N_{CS}) without any penalty on *BV*. This is because the p-ring region can effectively alleviate the electric field at the bottom of the trench. However, with the increase of N_{CS}, the safe-operating area (SOA) of p-ring IGBT degrades. The saturation current of p-ring IGBT is extremely sensitive to N_{CS} as shown in Fig. 4(b). To achieve wide forward biased (FB) SOA, the N_{CS} of p-ring IGBT should be limited below 3.5×10^{16} cm^{-3}. Comparing with the CSTBT, The saturation current of IGT IGBT is reduced by 27% owing to the addition of p-channel and the decrease of n-channel width.

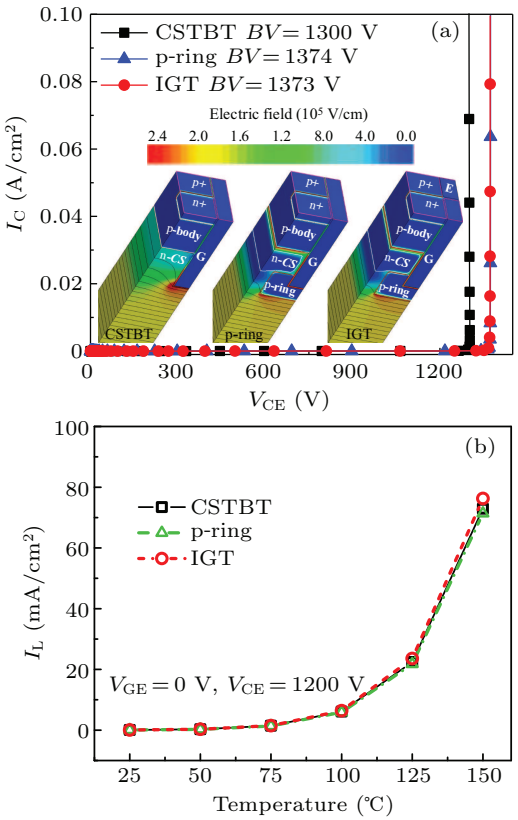


Fig. 3. (a) *BV* characteristics of three IGBT structures, with inset showing electric field distributions of three IGBT structures at breakdown. (b) Comparison of temperature-dependent leakage current among three IGBT structures.

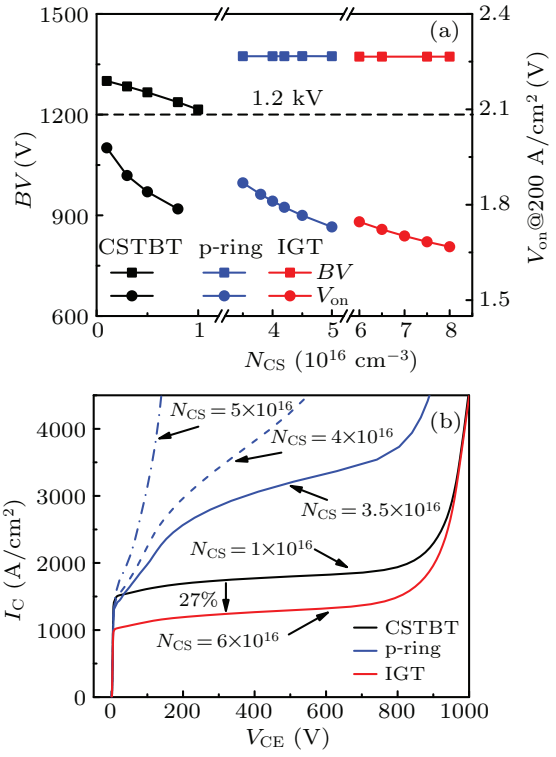


Fig. 4. (a) Variations of BV and V_{on} with N_{CS} for three IGBT structures. (b) I_C–V_{CE} curves for three IGBT structures with different N_{CS} values (V_{GE} = 15 V).

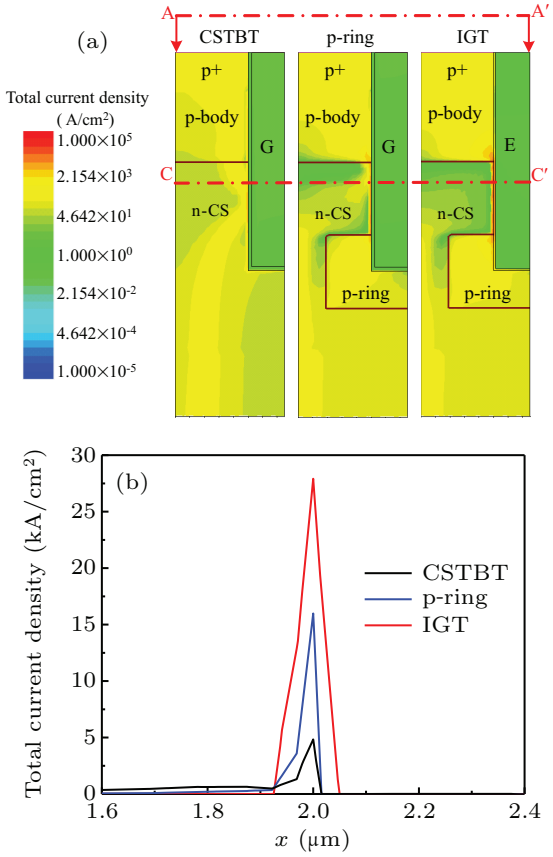


Fig. 5. Simulated total current density distributions along (a) cutline AA′ and (b) cutline CC′ for three IGBT structures when bus voltage rises to 600 V during turn-off.

Figure 5 shows the total current density distributions along cutline AA′ and cutline CC′ for three IGBT structures when bus voltage rises to 600 V during turn-off. The current density near the trench of the IGT IGBT is approximately six times higher than that of the CSTBT as shown in Fig. 5(b). This means that the built-in p-MOSFET is turned on and provides a p-channel for extracting most of the holes. This reduces the hole current flowing through the main junction. The hole current flowing through the p-channel does not increase the electric field in the y direction. This is because the electric flux emitted from the hole inversion layer ends at the poly emitter in the x direction. For the IGT IGBT, the extraction of holes by the built-in p-MOSFET alleviates the electric field at the p-body–n-CS junction and suppresses the dynamic avalanche.

Figure 6(a) shows the test circuit for inductive switching. For the IGT IGBT, the built-in p-MOSFET is already turned on before the turn-on moment. A large number of holes injected from p-collector can be extracted through the p-channel quickly. The potential of the p-ring region for the IGT structure shows no sharp increase owing to the absence of hole accumulation therein. Figure 6(b) shows the curves of the potential of the p-ring region below the trench gate and V_{GE} at the turn-on moment. A small V_P of 3.4 V and a small dV_P/dt of 11.4 V/μs are obtained in the IGT IGBT. The feature of the IGT IGBT is that its dV_P/dt is 60% smaller than that of the p-ring IGBT. Low dV_P/dt leads to low dV_{GE}/dt, which further results in low dI_C/dt. Thus, a lower dI_C/dt and a smaller surge current (I_{surge}) can be achieved in the IGT IGBT.

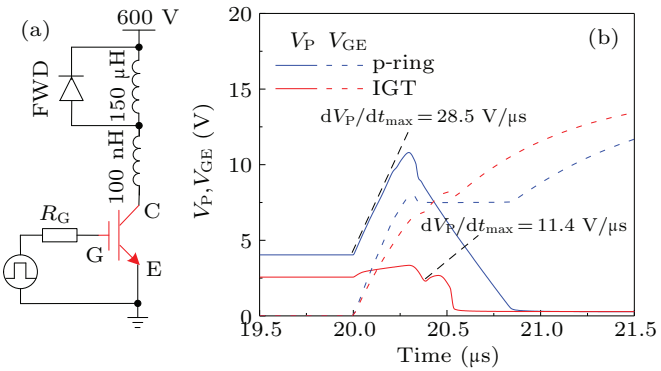


Fig. 6. (a) Inductive load circuit for switching characteristics analysis. (b) Curves of V_P (the potential of p-ring region below trench gate) and V_{GE} in turn-on process of p-ring IGBT and IGT IGBT under small-current condition (R_G = 10 Ω, I_C = 20 A/cm^2).

Figure 7(a) shows the comparison of capacitance among three IGBT structures. The overlap between gate and collector for the IGT IGBT decreases greatly, thus the gate-to-collector capacitance (C_{GC}) decreases by 67% compared with the counterpart of the CSTBT. In addition, the gate-to-emitter capacitance (C_{GE}) for the IGT IGBT is increased by 34% due to an increase in the overlap between the gate and emitter ($C_{iss} \gg C_{GC}$, so C_{GE} dominates in the input capacitance). Figure 7(b) shows that the gate-to-collector charge (Q_{GC}) of the IGT IGBT is 20% that of the CSTBT. All the characteristics are simulated at room temperature unless otherwise stated.

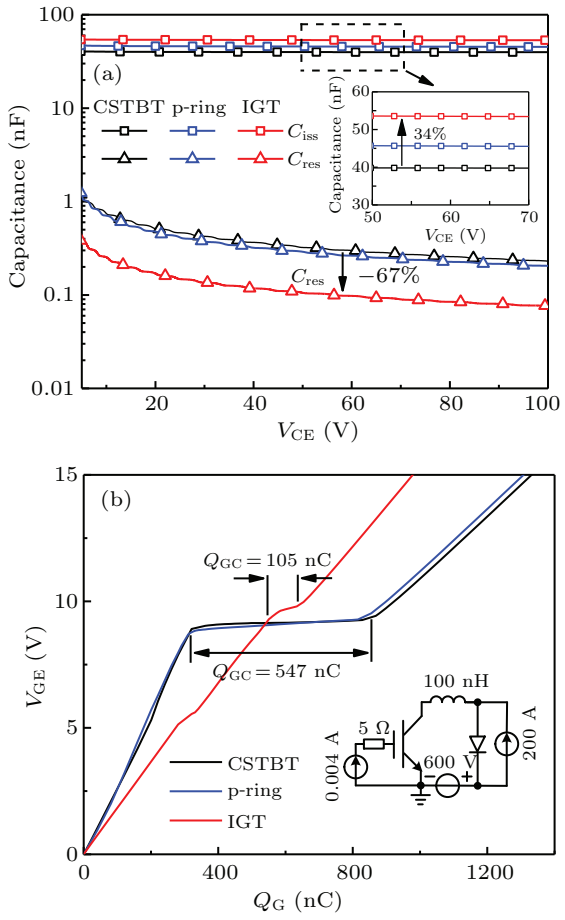


Fig. 7. (a) The *C*–*V* characteristics of three IGBT structures. (b) Gate charge characteristics of three IGBT structures.

3. Results and discussion

3.1. ON-state voltage

Figure 8 shows the ON-state characteristics for three IGBT structures. The N_{CS} for CSTBT, p-ring IGBT, and IGT IGBT is 1×10^{15} cm^{-3}, 3.5×10^{16} cm^{-3}, and 6×10^{16} cm^{-3}, respectively. The IGT IGBT obtains the enhanced conductivity modulation caused by increasing N_{CS}. When $I_C = 200$ A/cm^2, the V_{on} at room temperature for IGT IGBT, p-ring IGBT, and CSTBT is 1.75 V, 1.87 V, and 1.98 V, respectively.

3.2. Turn-off characteristics

The simulated turn-off characteristics of three IGBT structures as a function of gate resistance (R_G) are shown in Fig. 9. The CSTBT and p-ring IGBT show a decrease in surge voltage when $R_G < 5$ Ω. This indicates the occurrence of DA within the CSTBT and p-ring IGBT.[14] The turn-off curves of IGT IGBT show that surge voltage does not decrease with R_G lowering.

Figure 10 shows electric field distributions and impact ionization rate distributions for three IGBT structures when bus voltage rises to 600 V during turn-off. Owing to the increased N_{CS}, the p-ring IGBT presents significantly higher E_{max} and impact ionization rate than the CSTBT. For the IGT IGBT, the electric flux generated by the holes through the p-channel is dispersed in the *x* direction. This reduces the vertical electric field and the impact ionization rate at the turn-off moment. Consequently, the maximum impact ionization rate for the IGT IGBT is lowest.

Figure 11(a) shows the turn-off waveforms of three IGBT structures. Both devices are turned off at $t = 52$ μs. To make a comparison of turn-off loss among three IGBT structures, the turn-off process is divided into two phases as shown in Fig. 11(b). The first phase is the voltage rising phase (E_{vr}). The E_{vr} for the IGT IGBT (3.5 mJ/cm^2) is much smaller than that for the CSTBT (6.7 mJ/cm^2) owing to the lower Miller capacitance and the fast extraction of holes caused by self-biased p-channels. The second phase is the current decreasing phase (E_{cd}). The values of E_{cd} for all devices are similar, because of the same carrier lifetime and backside design of IGBTs.

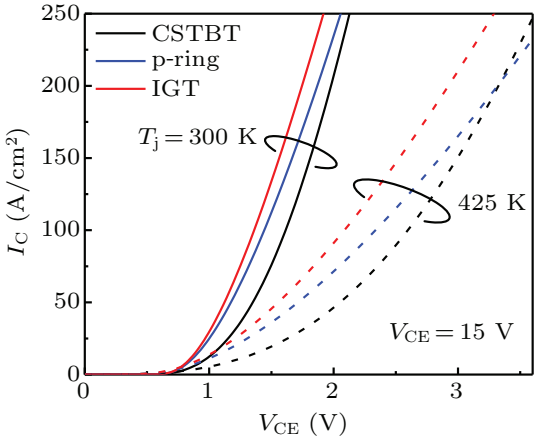


Fig. 8. The I_C–V_{CE} characteristics of three IGBT structures.

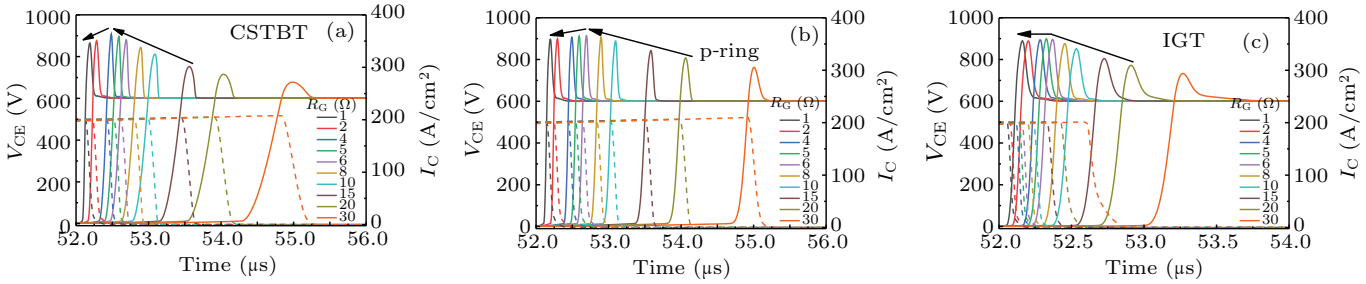


Fig. 9. Turn-off characteristics of (a) CSTBT, (b) p-ring IGBT, and (c) IGT IGBT with different values of R_G.

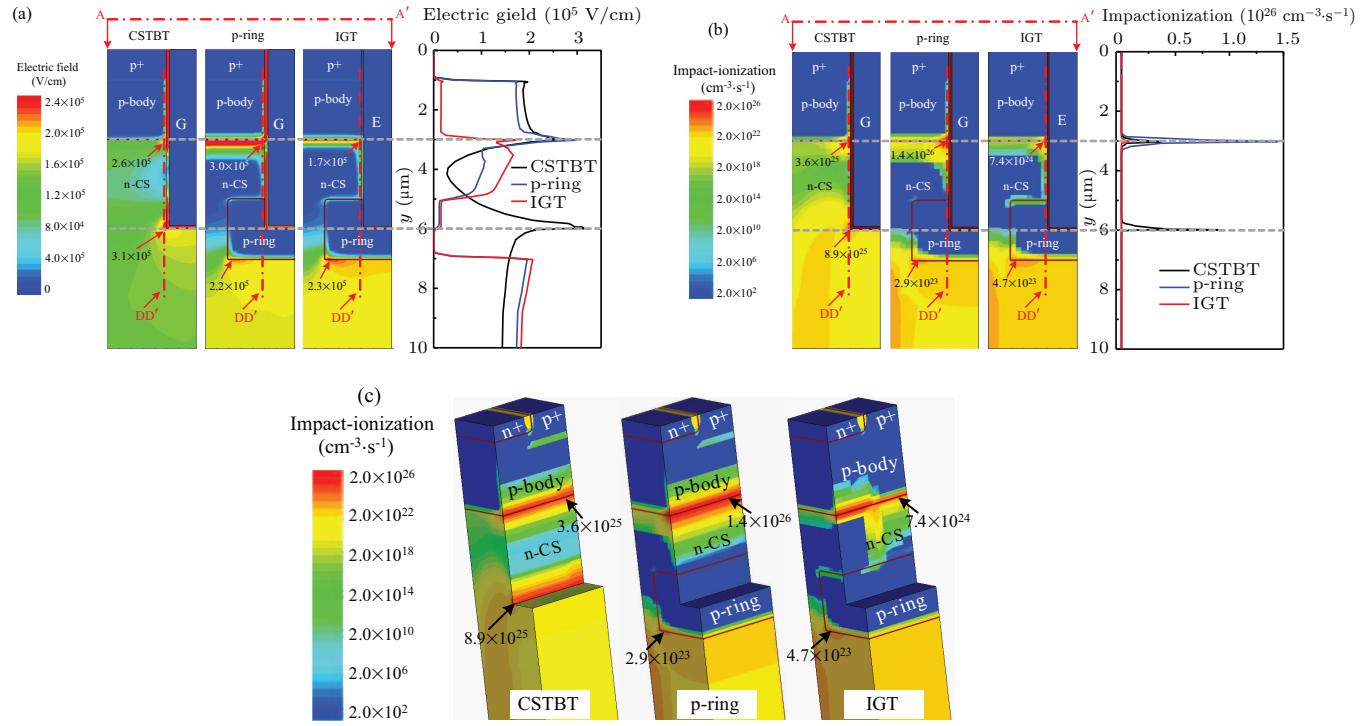


Fig. 10. (a) Simulated electric field distributions, (b) simulated impact ionization rate distributions along cutline AA′ and cutline DD′ for three IGBT structures, and (c) simulated impact ionization rate distributions for three IGBT structures, with $V_{CE} = 600$ V and $I_C = 200$ A/cm^2.

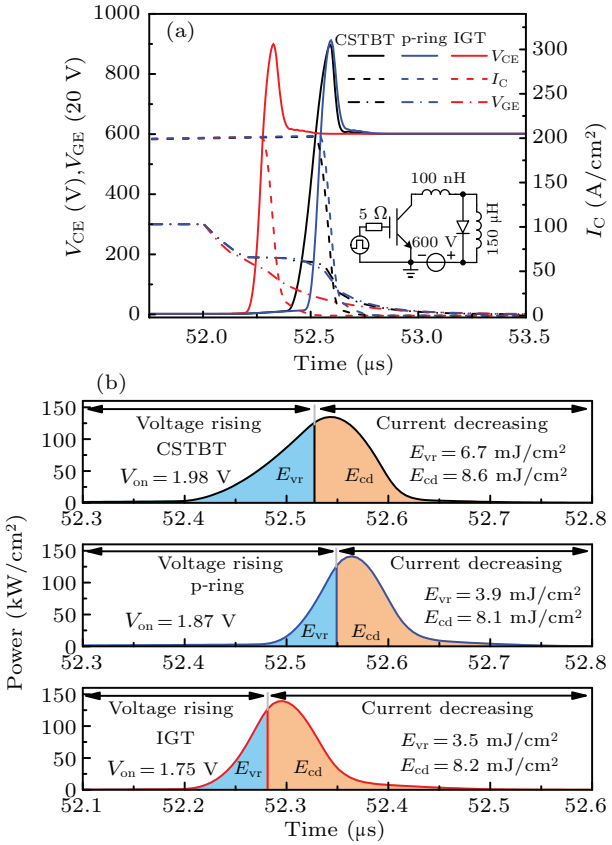


Fig. 11. (a) Turn-off waveforms for three IGBT structures and (b) turn-off power analyses for three IGBT structures.

Figure 12 shows that the IGT IGBT has the best trade-off relationship between V_{on} and E_{off}. For the same V_{on}, the E_{off} of the IGT IGBT is reduced by 31% compared with that of the CSTBT. This is because of the increased N_{CS} and the built-in self-biased p-MOSFET.

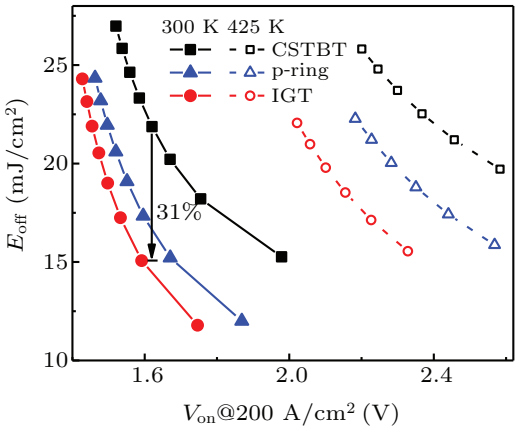


Fig. 12. The V_{on}–E_{off} trade-off relationships for three IGBT structures.

3.3. Turn-on characteristics

Figure 13 shows the turn-on waveforms of the three IGBTs with different values of R_G under a small current. The IGT IGBT has lower dI_C/dt and I_{surge} when compared with the CSTBT and p-ring IGBT. The IGT IGBT exhibits better controllability of I_{surge} and turn-on dI_C/dt than the CSTBT and p-ring IGBT. Figure 14 shows the influences of R_G on dI_C/dt and I_{surge} of three IGBT structures. Of the three IGBTs at the same R_G value, the IGT IGBT possesses the smallest dI_C/dt and I_{surge}. Figure 14(a) shows that the dI_C/dt and I_{surge} of the IGT IGBT decrease respectively by 62% and 35% compared with those of the p-ring IGBT, at a current density of 20 A/cm^2 and $R_G = 20$ Ω.

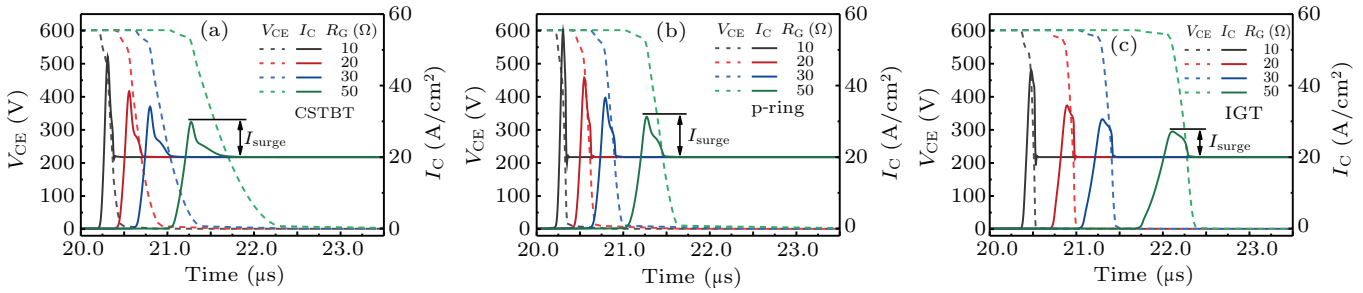


Fig. 13. Turn-on characteristics of (a) CSTBT, (b) p-ring IGBT, and (c) IGT IGBT with different values of R_G.

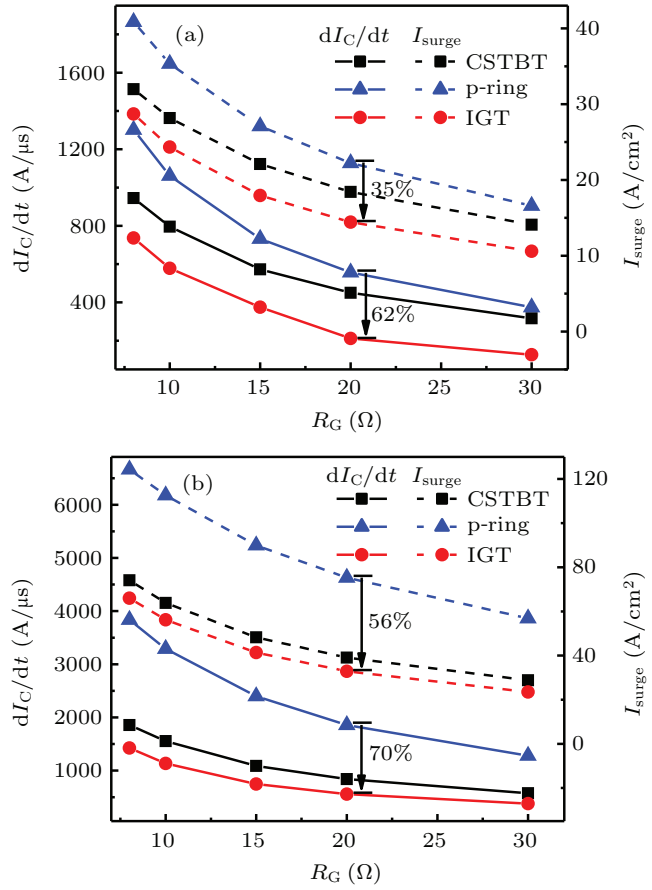


Fig. 14. Variations of dI_C/dt and I_{surge} with R_G for three IGBT structures at a current density of (a) 20 A/cm^2 and (b) 200 A/cm^2.

Figure 15(a) shows the dI_C/dt–E_{on} and I_{surge}–E_{on} tradeoff relationships for the three IGBT structures at a small current density of 20 A/cm^2 (1/10 rated current). The turn-on losses are calculated under R_G values of 8 Ω, 10 Ω, 15 Ω, 20 Ω, and 30 Ω, respectively. The IGT IGBT achieves better tradeoff relationships between E_{on} and dI_C/dt, E_{on} and I_{surge} than the CSTBT and p-ring IGBT. For the same value of E_{on}, the dI_C/dt and I_{surge} of the IGT IGBT decreases by 52% and 35% compared with those of the CSTBT. At a higher current density of 200 A/cm^2, the IGT IGBT still shows the suppressed dI_C/dt and I_{surge} compared with the CSTBT and p-ring IGBT at the same vale of E_{on} as shown in Fig. 15(b). At a higher current density of 200 A/cm^2, the p-ring IGBT has the worst trade-off relationships between E_{on} and dI_C/dt, E_{on} and I_{surge}. This is due to the increased self-charging displacement current flowing through the capacitor formed by the p-ring region, the gate oxide and the trench gate. Comparing with the p-ring IGBT, the dI_C/dt and I_{surge} of the IGT IGBT decrease by 39% and 25%, respectively.

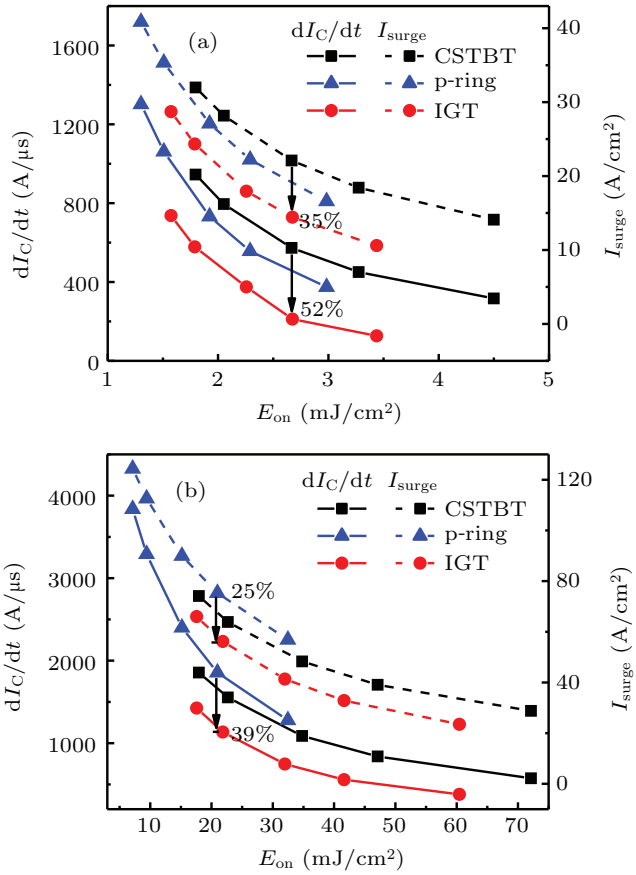


Fig. 15. The dI_C/dt–E_{on} and I_{surge}–E_{on} trade-off relationships for three IGBT structures at current density of 20 A/cm^2 (a) and 200 A/cm^2 (b).

4. Fabrication and process

The fabrication process of the proposed IGBT is shown in Fig. 16. The p-ring regions are formed by boron implantation at the trench bottom. The trench is then filled with poly-Si. Thereafter, the poly-Si is etched back using a mask. Next, the sidewall oxide is removed, followed by gate oxide growth and poly-Si refilling. Afterwards, the n+ region and p+ region are formed. Finally, the backside process is carried out and the metal electrodes are formed.

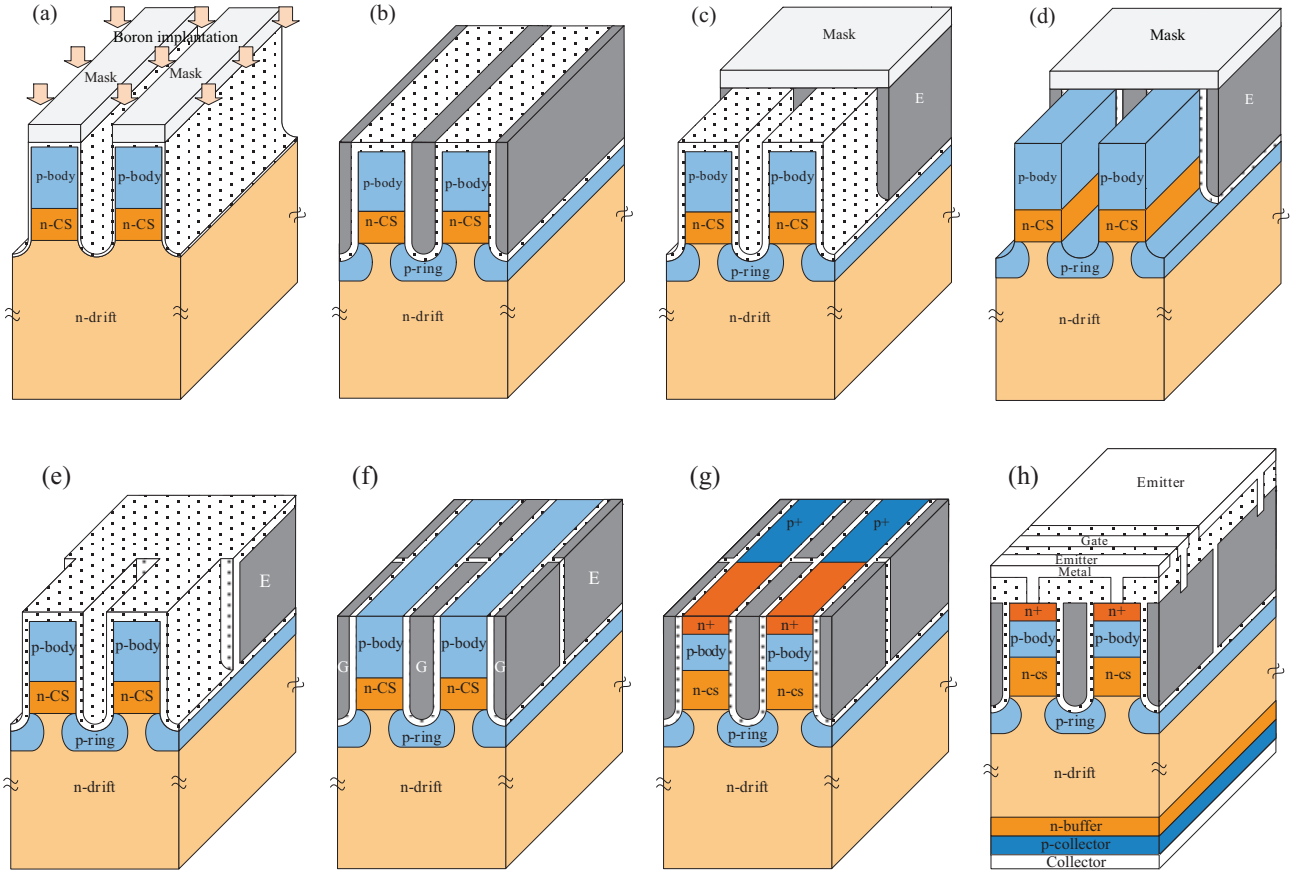


Fig. 16. Key process steps for the proposed IGT IGBT, showing (a) boron implantation at trench bottom, (b) poly-Si filling, (c) poly-Si etching, (d) oxide removal, (e) gate oxide growing, (f) poly-Si refilling, (g) n+ region and p+ region forming, and (h) metalization.

5. Conclusions

An IGBT with interleaved trench-gate is proposed and investigated via numerical analysis. Owing to the interleaved trench gate architecture, the Miller capacitance of the proposed IGBT decreases by 67% compared with that of the CSTBT. The proposed IGT IGBT also shows the improved V_{on}–E_{off} trade-off. Comparing with the CSTBT, the E_{off} of the proposed IGBT decreases by 31% with the same value of V_{on}. Furthermore, the proposed IGBT obtains a better turn-on dI_C/dt controllability and improves the trade-off relationship between E_{on} and dI_C/dt. For the same value of E_{on} at a current density of 20 A/cm^2, I_{surge} and dI_C/dt of the proposed IGBT decrease by 35% and 52% compared with those of the CSTBT.

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