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SiC trench MOSFET with dual shield gate and optimized JFET layer for improved dynamic performance and safe operating area capability

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A novel silicon carbide (SiC) trench metal–oxide–semiconductor field-effect transistor (MOSFET) with a dual shield gate (DSG) and optimized junction field-effect transistor (JFET) layer (ODSG-TMOS) is proposed. The combination of the DSG and optimized JFET layer not only significantly improves the device's dynamic performance but also greatly enhances the safe operating area (SOA). Numerical analysis is carried out with Silvaco TCAD to study the performance of the proposed structure. Simulation results show that comparing with the conventional asymmetric trench MOSFET (Con-ATMOS), the specific on-resistance ($R_{on,sp}$) is significantly reduced at almost the same avalanche breakdown voltage (BV_{av}). Moreover, the DSG structure brings about much smaller reverse transfer capacitance (C_{rss}) and input capacitance (C_{iss}), which helps to reduce the gate–drain charge (Q_{gd}) and gate charge (Q_g). Therefore, the high frequency figure of merit (HFFOM) of $R_{on,sp} \cdot Q_{gd}$ and $R_{on,sp} \cdot Q_g$ for the proposed ODSG-TMOS are improved by 83.5% and 76.4%, respectively. The switching power loss of the proposed ODSG-TMOS is 77.0% lower than that of the Con-ATMOS. In addition, the SOA of the proposed device is also enhanced. The saturation drain current ($I_{d,sat}$) at a gate voltage (V_{gs}) of 15 V for the ODSG-TMOS is reduced by 17.2% owing to the JFET effect provided by the lower shield gate (SG) at a large drain voltage. With the reduced $I_{d,sat}$, the short-circuit withstand time is improved by 87.5% compared with the Con-ATMOS. The large-current turn-off capability is also improved, which is important for the widely used inductive load applications.

Keywords: SiC trench MOSFET, switching power loss, figure of merit, safe operating area

PACS: 85.30.De, 73.40.Qv, 85.30.Tv, 51.50.+v **DOI:** 10.1088/1674-1056/acdc8d

1. Introduction

Silicon carbide metal–oxide–semiconductor field-effect transistor (SiC MOSFET) is suitable for high frequency and high voltage applications owing to its material properties.[1,2] It opens the ways to diverse industries, including new energy vehicles, rail transit, and smart grids. In these applications, it is necessary to deal with short circuit, high temperature, and other extreme cases, which requires SiC MOSFET to be improved not only in performance, but also in reliability. SiC planar gate MOSFET demonstrates good reliability and has been commercialized for a long time. Compared with the planar counterparts, SiC trench gate MOSFETs (TMOSs) are preferred to further improve the device performance, owing to higher channel density and absence of junction field-effect transistor (JFET) region.[3] However, in the case of conventional TMOS, the high electric field present in the trench oxide during the blocking state leads to premature breakdown prior to the drain bias reaching an avalanche breakdown voltage (BV_{av}).

With the development of the material and device manufacturing technology, many methods to optimize the SiC MOSFET structure have been proposed. Rohm *et al.* proposed an SiC double trench MOSFET (DTMOS) with a heavily doped p-type shielding region (P+SLD) at the sidewall and bottom of the source trench.[4,5] The DTMOS achieves an ultra-low specific on-resistance ($R_{on,sp}$). However, its large gate capacitance causes high switching power loss (P_{sw}). In comparison with the DTMOS, the asymmetric TMOS (ATMOS) proposed in Refs. [6,7] shows better robustness, owing to the shielding effect provided by the half-surrounded P+SLD.[8] However, the inherently large MOS channel density of the trench structures results in a large saturation drain current ($I_{d,sat}$), which reduces the short-circuit (SC) withstand time (t_{sc}) and limits the improvement of the short circuit safe operating area (SCSOA). To further improve the switching characteristics and reduce the P_{sw}, split/shield gate (SG) is introduced in Refs. [9–11]. Introducing SG is an effective way to reduce gate–drain capacitance (C_{gd}). Moreover, unlike the Si counterpart, a thicker shield gate oxide thickness (T_{sgox}) is conducive to alleviating the maximum electric field in the gate oxide ($E_{ox,peak}$) for the SiC SG-TMOS, which improves the gate oxide reliability. However, the coupling between the gate and source electrode still brings about large gate–source capacitance (C_{gs}) and the switching speed improvement is lim-

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In this paper, a novel SiC trench MOSFET with a dual shield gate (DSG) and optimized JFET layer (ODSG-TMOS) is proposed. Compared with the conventional ATMOS (Con-ATMOS), the proposed structure shows good trade-off among the $R_{on,sp}$, breakdown voltage (BV), and gate oxide reliability. The DSG structure reduces not only C_{gd} but also C_{gs} significantly. Therefore, the gate–drain charge (Q_{gd}) and gate charge (Q_g) are both reduced. As a result, the switching speed is improved and the P_{sw} is reduced, which significantly improves the dynamic performance. In addition, the t_{sc} is increased with $I_{d,sat}$ decreasing and the large-current turn-off capability is also enhanced substantially.

2. Device structure and mechanism

Figures 1(a) and 1(b) show schematic cross-sectional view of the proposed ODSG-TMOS and Con-ATMOS, respectively. Both devices have an asymmetric trench gate structure on the surface. Compared with the Con-ATMOS, the proposed device features a fin-shaped gate which is surrounded by dual source-connected SGs and an L-shaped JFET layer. The shielding effect provided by the lower SG conduces to reducing the C_{gd} and the reduced overlapping area between the narrower fin-shaped gate and lower SG creates reduced C_{gs}. Apart from that, the interaction between the gate and the side wall of the source-connected P+SLD for the Con-ATMOS is transformed into the interaction between the fin-shaped gate and fin-shaped source-connected SG. Since the oxide layer between the two fin-shaped electrodes is much thicker than that at the side wall of the gate trench, the interaction between them is greatly decoupled, which can further reduce the C_{gs} of the proposed structure. Therefore, the reverse transfer capacitance (C_{rss}), input capacitance (C_{iss}), gate charge (Q_g) as well as gate–drain charge (Q_{gd}) are reduced, which improve the dynamic performance of the device. Furthermore, the thicker oxide layer of the DSG reduces the peak electric field at the trench corner, and combined with an optimized JFET layer, $R_{on,sp}$ is reduced without sacrificing the BV. In addition, since the lower SG is connected to the source, its potential remains 0 V instead of the gate drive voltage of 15 V or 18 V when the ODSG-TMOS is under saturation. Therefore, electrons do not gather near the side wall nor in corner of the lower SG. The depletion region is expanded widely in that region, which reduces the width of electron conduction path and enhances the JFET effect. As a result, the $I_{d,sat}$ is reduced and the t_{sc} is increased. By using the Silvaco TCAD with the modified models used in our previous work, such as band gap narrowing (BGN), CONSRH, CONWELL, SULFMOB, incomplete ionization, Auger and analytic models, the performance of the device is simulated.[11–13] The device parameters used in the simulation are shown in Table 1. The parameters not listed are the same for the two structures. The device areas used in this work for the two devices are both 1 cm^2, unless otherwise mentioned.

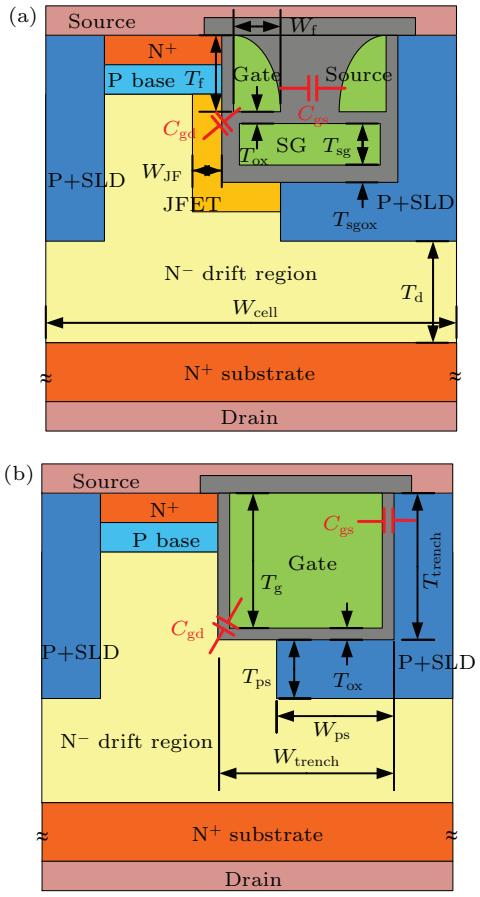


Fig. 1. Cross-section view of (a) proposed ODSG-TMOS and (b) Con-ATMOS.

Table 1. Main device parameters used in simulation.

Parameters	Con-ATMOS	ODSG-TMOS
Gate oxide thickness, T_{ox} (nm)	50	50
Trench width, W_{trench} (μm)	1	1
Trench depth, T_{trench} (μm)	1.15	1.15
P$^+$ region width under trench, W_{ps} (μm)	0.7	0.7
P$^+$ region thickness under trench, T_{ps} (μm)	0.4	0.4
N$^-$ drift region thickness, T_d (μm)	11	11
Gate depth, T_g (μm)	1.1	–
Shield gate thickness, T_{sg} (μm)	–	0.4
Shield gate oxide thickness, T_{sgox} (μm)	–	0.1
Control gate width, W_f (μm)	–	0.2
Control gate thickness, T_f (μm)	–	0.6
JFET region width, W_{JF} (μm)	–	0.3
Cell width, W_{cell} (μm)	2.5	2.5
N$^-$ drift region concentration, N_d (cm^{-3})	1×10^{16}	1×10^{16}
N$^+$ region concentration, N_{N^+} (cm^{-3})	3×10^{19}	3×10^{19}
P$^+$ channel region concentration, N_{PC} (cm^{-3})	3×10^{17}	3×10^{17}
P$^+$ shielding region concentration, N_{PS} (cm^{-3})	5×10^{18}	5×10^{18}
JFET region concentration, N_{JF} (cm^{-3})	–	4×10^{16}

3. Results and discussion

Figure 2(a) shows conduction I–V curves and blocking I–V curves for the proposed ODSG-TMOS and Con-ATMOS, respectively. Even with the source-connected SGs, the $R_{on,sp}$ is 1.99 mΩ·cm^2 for the Con-ATMOS and 1.69 mΩ·cm^2 for the ODSG-TMOS. It is improved by 15.1% owing to the introduction of the additional JFET layer. Owing to the fact that the JFET layer has high doping concentration (N_{JF}), at low drain–source voltage (V_{ds}) the lateral expansion of the depletion region formed in the drift region is limited. Therefore, the conducting path for electrons moving from the channel to the drift region is widened and has a low-resistance. Contributed by the thicker T_{sgox}, the BV_{av} of the ODSG-TMOS is 1215 V, which is only 3% lower than that of the Con-ATMOS. The electric field contours at avalanche breakdown are shown in Fig. 2(b). The maximum electric field in the gate oxide ($E_{ox,peak}$) for the Con-ATMOS is 3.29 MV/cm, which is higher than that for the ODSG-TMOS. It exceeds 3 MV/cm, a recognized value commonly used to define the gate oxide breakdown (BV_{ox}) from the perspective of long-term reliability. Further investigation results show that the BV_{ox} of the Con-ATMOS is only 960 V, at which the $E_{ox,peak}$ reaches 3 MV/cm. The limiting factor to determine the device breakdown is changed and it shifts from the avalanche breakdown for the proposed ODSG-TMOS to the gate oxide breakdown for the Con-ATMOS. Compared with the Con-ATMOS, the proposed structure demonstrates good trade-off among the $R_{on,sp}$, BV, and gate oxide reliability.

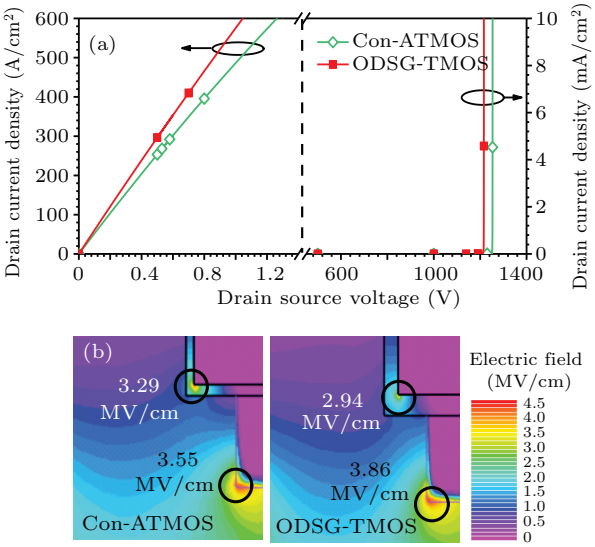


Fig. 2. (a) Conduction and blocking I–V characteristics. (b) Electric field contours at avalanche breakdown of the two structures.

The transfer characteristics of the two structures are shown in Fig. 3. The V_{ds} remains 0.1 V when the gate voltage (V_{gs}) increases. It can be seen that the values of drain-source current (I_{ds}) of both structures increase quickly when the V_{gs} is larger than 5 V. The threshold voltage (V_{th}) extracted at I_{ds} = 10 mA/cm^2 is 5.6 V for the ODSG-TMOS and 5.7 V for the Con-ATMOS. The slight difference in V_{th} is due to the decreased $R_{on,sp}$ and alleviative JFET effect caused by the highly doped JFET region at low V_{ds}.

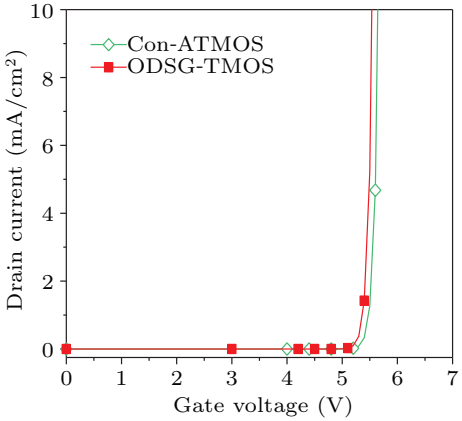


Fig. 3. Transfer characteristics of the two structures.

Figure 4 shows the dependence of the extracted C_{iss}, C_{rss}, and output capacitance (C_{oss}) on V_{ds} for the two structures. It can be seen that as V_{ds} increases, C_{iss} remains almost unchanged, while C_{oss} and C_{rss} show obvious nonlinear characteristics. The two parameters for the proposed device at the V_{ds} of about 5 V change suddenly, which is caused by the depletion of the heavily doped JFET layer. In the V_{ds} range from 0 V to 1000 V, the C_{iss} and C_{rss} of the proposed ODSG-TMOS structure are both smaller than those of the Con-ATMOS structure. The values extracted at the V_{ds} of 600 V are shown in Fig. 4. At the V_{ds} of 600 V, the C_{oss} of the two structures are almost the same, while the C_{iss} and C_{rss} of the ODSG-TMOS decrease by 69.3% and by an order of magnitude when compared to those of the Con-ATMOS, respectively. It can be concluded that the reduced gate depth as well as decoupled interaction between the gate and drain/source introduced by the DSG structure results in the improvement of the C_{iss} and C_{rss}. The C_{iss} and C_{rss} for a power switching device are of particular importance since it has a great influence on the P_{sw}. Moreover, the smaller ratio of C_{rss} to C_{iss} for the proposed structure is of benefit to suppressing the false turn-on of the device. Considering that the capacitance characteristics at a certain terminal voltage cannot fully reflect the influence of the parasitic capacitance on the switching characteristic of a device, the gate charging characteristic is studied. Figure 5 shows the comparison of gate charging characteristic between the two structures. The test circuit is also shown in the inset. Smaller C_{iss} and C_{rss} enable faster charging speed and also improve the Q_{gd} and Q_g. With V_{gs} in a range from 0 V to 15 V, the Q_{gd} and Q_g are 144 nC/cm^2 and 1330 nC/cm^2 for the Con-ATMOS, and 28 nC/cm^2 and 370 nC/cm^2 for the ODSG-TMOS, respectively. The Q_{gd} and Q_g for the ODSG-TMOS are reduced by 80.6% and 72.2% compared with those for Con-ATMOS, respectively. The high frequency figure of merit (HFFOM,

$R_{on} \cdot Q_{gd}$) of the Con-ATMOS is 286.56 mΩ·nC while that of the ODSG-TMOS is only 47.32 mΩ·nC. In addition, another widely used HFFOM, the $R_{on} \cdot Q_g$, is 2646.70 mΩ·nC for the Con-ATMOS and 625.30 mΩ·nC for the ODSG-TMOS. They are improved by 83.5% and 76.4%, respectively. To better demonstrate the advantage of the ODSG-TMOS, the HHFOMs of the reported devices are also compared. The $R_{on} \cdot Q_{gd}$ and $R_{on} \cdot Q_g$ for the device in Ref. [14] are 438 mΩ·nC and 1722.8 mΩ·nC while those for the device proposed in Ref. [15] are 449 mΩ·nC and 2094 mΩ·nC, respectively. It is obvious that the performance of the ODSG-TMOS is improved significantly.

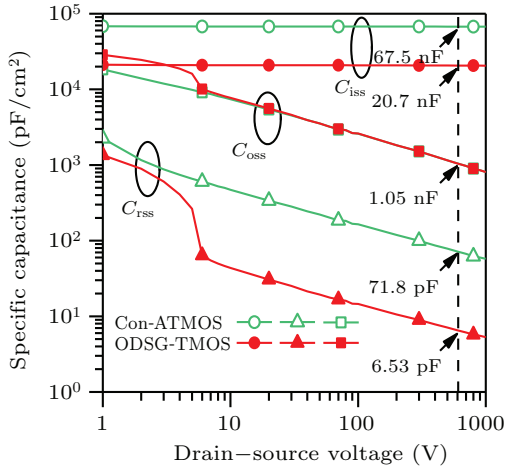


Fig. 4. Extracted C_{iss}, C_{rss}, and C_{oss} at different drain voltages.

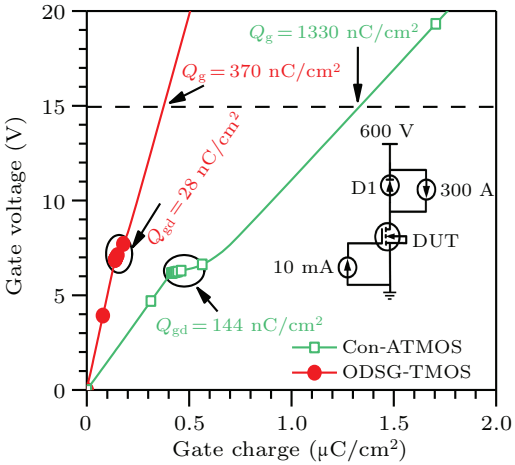


Fig. 5. Gate charging characteristics of the two structures.

The switching waveforms with inductive load for the two devices are plotted in Fig. 6(a). The V_{gs} is turned on at $t = 0$ μs and turned off at $t = 20$ μs. It is obvious in Fig. 6(a) that the Miller platform of the proposed ODSG-TMOS is significantly shortened, which is consistent with the result mentioned above. Owing to the reduced C_{iss} and C_{rss}, the switching delay time of the ODSG-TMOS decreases significantly and the switching speed increases. The turn-on delay time and the turn-off delay time of the Con-ATMOS are 1.92 μs and 3.24 μs while those of the ODSG-TMOS are only 540 ns and 920 ns, they decreasing by 71.9% and 71.6%, respectively. In addition, power loss of the proposed ODSG-TMOS also decreases. The total power loss, including the conduction power loss (P_{con}) and P_{sw} of the two structures at different frequencies are depicted in Fig. 6(b). The P_{con} and P_{sw} of the ODSG-TMOS are 15.6% and 77.0% lower than those of the Con-ATMOS, respectively. As frequency increases, the P_{con} remains constant, with the same duty cycle of 50%, but the difference in P_{sw} becomes greater. Benefiting from the higher switching speed and lower P_{sw}, the ODSG-TMOS is more promising to high frequency applications than the Con-ATMOS.

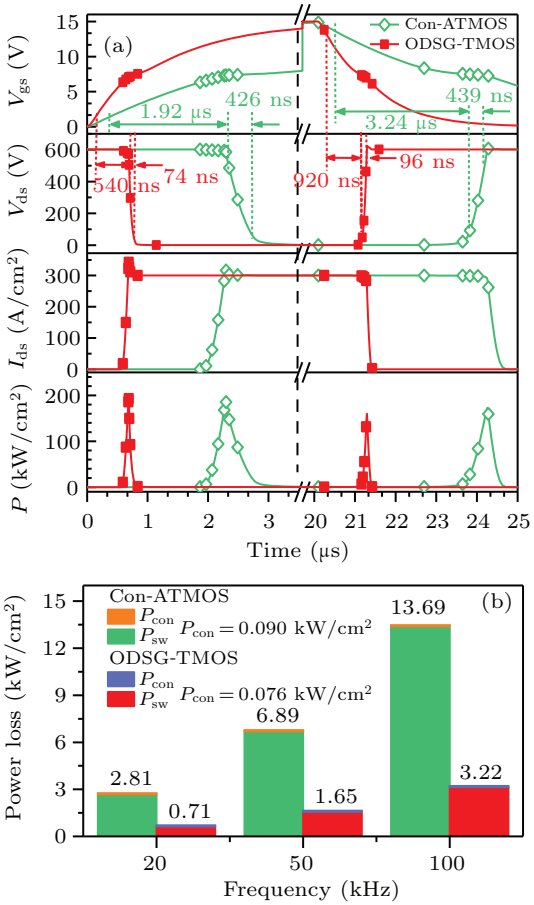


Fig. 6. (a) Waveforms of switching process and (b) power losses at different frequencies, with duty cycle being 50% and inductive load used.

Figure 7(a) shows *I*–*V* characteristic curves varying with drain voltage till saturation for the two structures under different values of V_{gs}. It can be seen that when the $V_{gs} = 8$ V and 10 V, the values of $I_{d,sat}$ for the Con-ATMO and the ODSG-TMOS are almost the same. However, when the $V_{gs} = 15$ V and 18 V, the values of $I_{d,sat}$ of the ODSG-TMOS are much smaller than those of the Con-ATMOS, owing to the lateral depletion effect provided by the lower SG under gate as shown in Fig. 7(b). The black lines in the figures are depletion edges of the two structures at the V_{ds} of 600 V with $V_{gs} = 15$ V. It is obvious that the depletion region of the ODSG-TMOS expands widely, thus reducing the width of electron conduction path. Smaller $I_{d,sat}$ conduces to reducing the power density

when the device is under the short-circuit condition. Therefore, a longer t_{sc} is obtained for the ODSG-TMOS as shown in Fig. 8. For the SC simulation, a V_{gs} of 15 V, a gate resistor of 1 Ω and a bus voltage of 600 V with electrothermal coupling models are used. The dotted current curves represent the critical time at which the devices can be turned off normally. On the contrary, the solid current curves refer to the case where the devices fail in a longer short-circuit operation time. It can be seen that the t_{sc} is 1.6 μs for the Con-ATMOS and 3.0 μs for the ODSG-TMOS. It is improved by 87.5%, with the $I_{d,sat}$ reduced. Once the two MOSFETs are turned on, their SC currents rapidly increase and reach the corresponding values of $I_{d,sat}$. After that, the saturation currents of the two structures start to decrease owing to the self-heating effect as well as

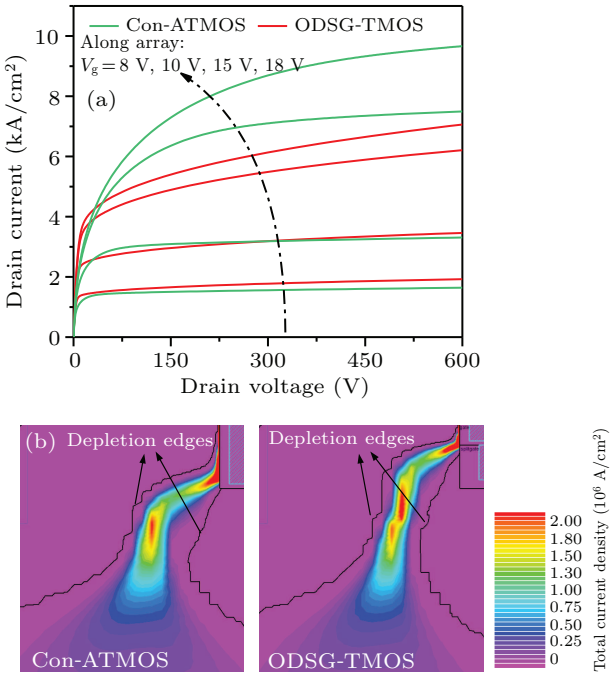


Fig. 7. (a) The *I*–*V* characteristic curves with V_{ds} varying from 0 V to 600 V and (b) current density and depletion edges at V_{ds} of 600 V with V_{gs} = 15 V.

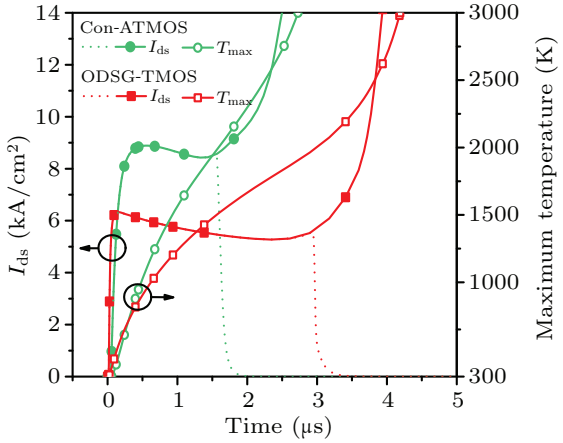


Fig. 8. Short circuit waveforms of the two structures, with dotted current curves representing the critical time at which the devices can be normally turned off, and solid current curves referring to the condition where the devices fail in a longer short-circuit operation time.

reduced carrier mobility in the inversion MOS channel and drift region with the increase of junction temperature. Owing to the large power loss under the SC condition, once the junction temperature reaches the intrinsic temperature limit, the current increases rapidly and then thermal runaway occurs.

To evaluate the reverse-biased SOA (RBSOA) of the proposed device, the large-current turn-off capability with an inductive load is discussed in Fig. 9. In the simulation, an initial junction temperature of 448 K, a bus voltage of 1200 V and a large current of 1800 A (6 times the nominal current) are used, with the electro-thermal coupling model adopted. The values of V_{gs} of the two devices both turn from 15 V to 0 V at $t = 2$ μs. After a delay of a few microseconds, the ODSG-TMOS is normally turned off while the Con-ATMOS cannot. It can be found that for the Con-ATMOS, after the V_{ds} reaches the bus voltage of 1200 V, the I_{ds} starts to drop normally. However, after a short drop, the I_{ds} recovers to 1800 A again and the V_{ds} of the Con-ATMOS starts to drop. The Con-ATMOS fails in the large-current turn-off process and losses blocking capability. The junction temperatures of the two devices in the turn-off process are also shown in the figure. It is found that the junction temperature of the Con-ATMOS increases to about 2000 K while the proposed ODSG-TMOS shows much less temperature rise. Like the results shown in Fig. 6, the slower turn-off speed and higher P_{sw} for the Con-ATMOS contribute to the rapid rise of the junction temperature.

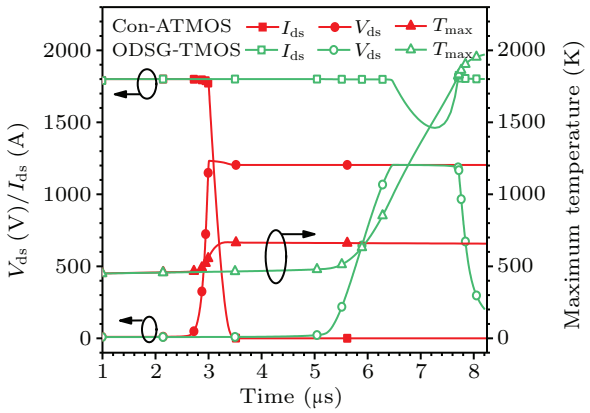


Fig. 9. Waveforms of large-current turn-off characteristics.

The influence of the fin-shaped control gate width (W_f) on the performance of the ODSG-TMOS at 50 kHz is shown in Fig. 10. In the simulation, the fin-shaped source-connected SG keeps the width identical with that of the fin-shaped gate. It can be seen in Fig. 10(a) that the C_{gd} keeps almost unchanged owing to good shielding effect provided by the lower SG while the C_{gs} significantly increases as the W_f increases from 0.1 μm to 0.4 μm. Accordingly, the Q_{gd} shown in Fig. 10(b) keeps almost unchanged while the Q_g and P_{sw} increase with W_f increasing. The smaller the W_f, the better performance can be obtained. Further research results show that the smaller W_f not only reduces the overlapping area between the gate and lower

SG, but also increases the thickness of the oxide layer between the fin-shaped gate and the fin-shaped source-connected SG, which both decouple the interaction between the gate and source, and therefore, significantly reducing the C_{gs} of the device. It shows that the C_{gs} affects not only the switching speed but also the switching power loss, especially when the C_{gd} is small enough.

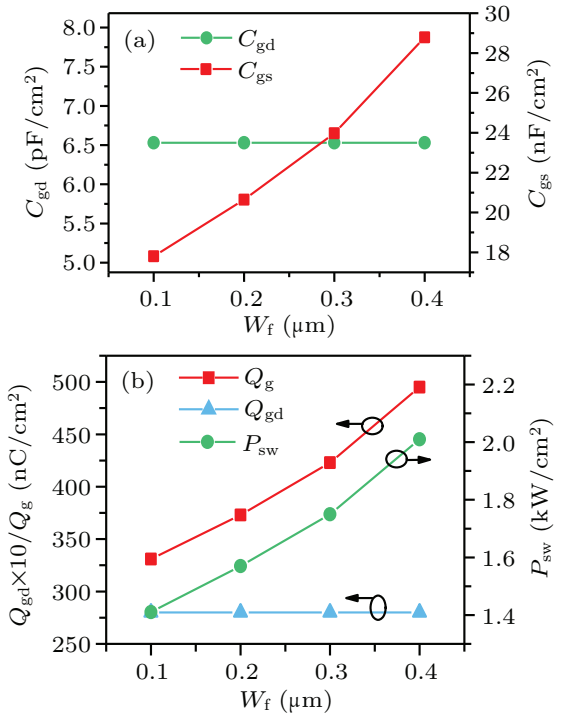


Fig. 10. Influence of W_f on performance of the proposed ODSG-TMOS (a) for C_{gd} and C_{gs} at $V_{ds} = 600$ V and (b) for Q_g, Q_{gd}, and P_{sw}.

Figures 11(a) and 11(b) show the relationship between $I_{d,sat}$ and $R_{on,sp}$, and the relationship between BFOM and N_{JF} for different values of JFET layer width (W_{JF}), respectively . It can be seen from Fig. 11(a) that with the same W_{JF}, the $R_{on,sp}$ decreases and $I_{d,sat}$ increases with the increase of the N_{JF}. Similarly, the $R_{on,sp}$ decreases and $I_{d,sat}$ increases with the increase of the W_{JF} when the N_{JF} is kept unchanged. The reason is that increasing N_{JF} and/or W_{JF} of the JFET layer provides a low resistance path for electrons in the conduction state at lower V_{ds} regime. However, the JFET effect provided by the lower SG at large V_{ds} is also attenuated since the JFET layer is more difficult to deplete. Figure 11(b) shows the influence of the W_{JF} and N_{JF} on the Baliga's figure of merit (BFOM, $BV^2/R_{on,sp}$) for the proposed device. As mentioned above, the blocking capability of the device is determined by the lower one of the BV_{av} and BV_{ox}. When the N_{JF} is low, the BV_{av} is a lower one and the BFOM increases as the N_{JF} increases, owing to $R_{on,sp}$ decreasing. However, the BV_{ox} decreases rapidly with the increase of N_{JF}, owing to $E_{ox,peak}$ increasing in the trench corner. The BV_{ox} becomes lower than BV_{av} when the N_{JF} is greater than a certain value. And after that, the BFOM decreases rapidly with the increase of N_{JF}, owing to the BV_{ox} decreasing. Therefore, considering the influence of the W_{JF} and N_{JF}, there appears a balance after the conduction performance, BFOM and SCSOA for the proposed ODSG-TMOS have been optimized.

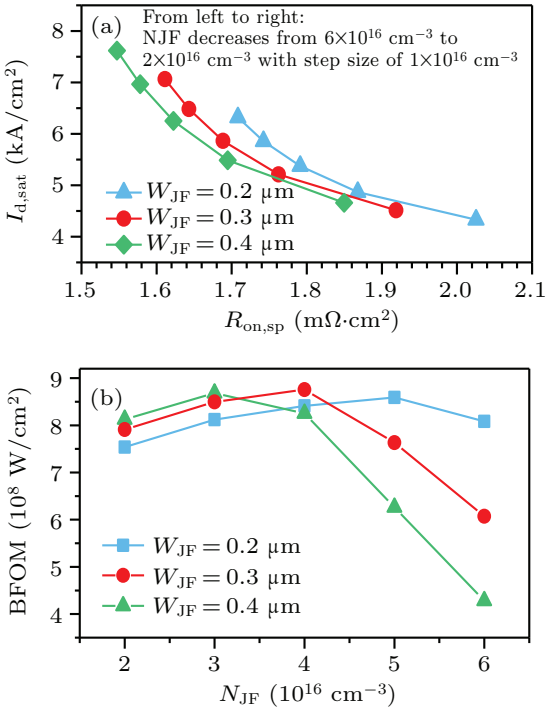


Fig. 11. (a) Trade-off relationship between $R_{on,sp}$ and $I_{d,sat}$ with influence of the W_{JF} and N_{JF}, and (b) influence of W_{JF} and N_{JF} on BFOM for the proposed ODSG-TMOS.

Figure 12 shows the influence of concentration of the N$^-$ drift region (N_d) on the BV and $R_{on,sp}$, respectively. As expected, the two parameters both decrease with the increase of N_d. When N_d increases from 7×10^{15} cm^{-3} to 1.3×10^{16} cm^{-3}, BV decreases from 1559 V to 938 V and $R_{on,sp}$ declines from 2.21 mΩ·cm^2 to 1.44 mΩ·cm^2. It can be found that to ensure that the BV is larger than 1200 V, the N_d must be kept less than or equal to 1×10^{16} cm^{-3}. Therefore, the optimized $R_{on,sp}$ is obtained when the N_d is equal to 1×10^{16} cm^{-3}. In this case, the BV of the ODSG-TMOS is almost the same as that of the Con-ATMOS while the $R_{on,sp}$ is 15.1% lower.

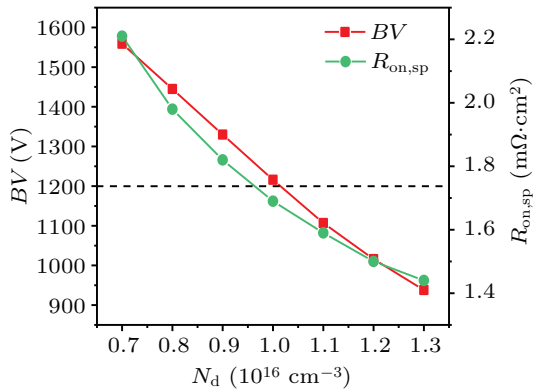


Fig. 12. Influence of N_d on BV and $R_{on,sp}$.

In order to show the feasibility of the proposed ODSG-TMOS structure, a possible manufacturing process flowchart is shown in Fig. 13. Firstly, an epitaxial lightly doped N$^-$ drift

layer is grown on an N^+ substrate. After forming the epitaxial layer, the P+SLD, N^+ source region and P-base form via multiple ion implantation as shown in Fig. 13(b). After the gate trench is etched, an L-shaped JFET area forms through tilted multiple ion implantation as shown in Figs. 13(c)–13(d). Using thermal oxidation to form an oxide layer on the surface and the bottom and sidewalls of the trench, the gate trench is filled with polysilicon and then etched to form the lower split gate as shown in Figs. 13(e)–13(g). Similarly, the fin-shaped gate and source also form by filling and etching process as shown in Figs. 13(h)–13(j).[14,15] The process of forming fin-shaped gate is a self-aligned process and W_f is determined by the deposited thickness of the polysilicon film and subsequent etching process. After that, dielectric is deposited and metal process is utilized to form the source and drain electrode. The final structure fabricated is shown in Fig. 13(l).

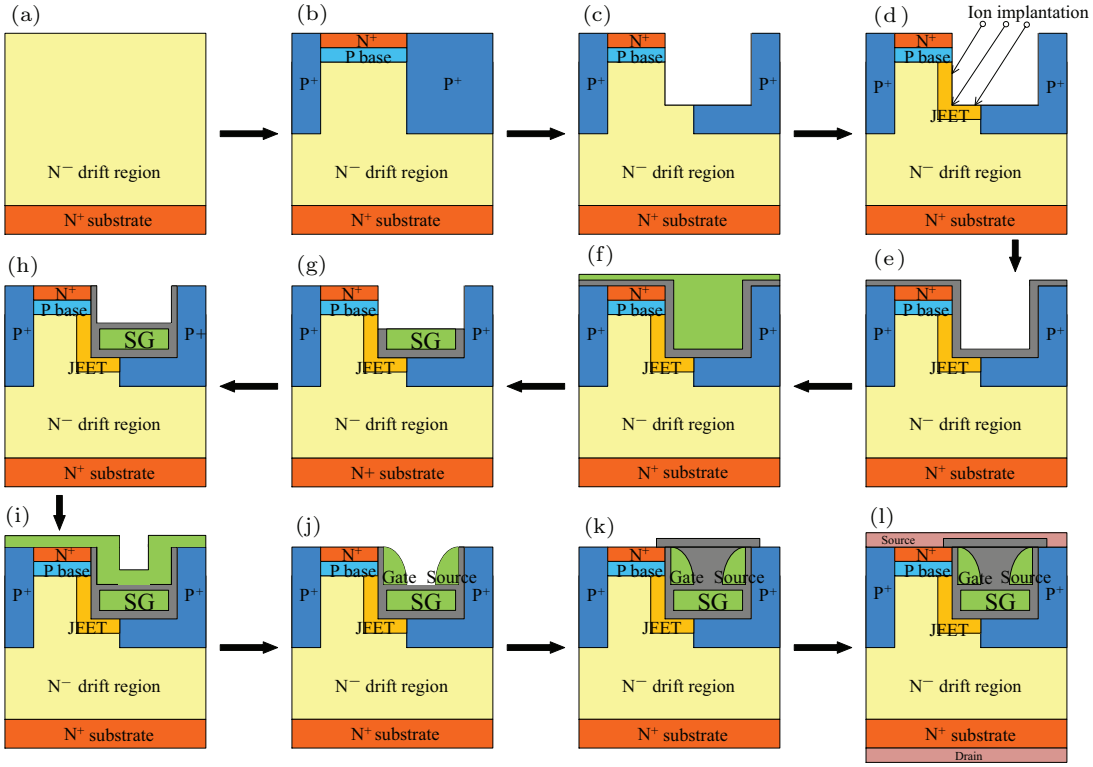


Fig. 13. Proposed manufacturing process of ODSG-TMOS.

4. Conclusions

A novel SiC ODSG-TMOS structure is proposed and investigated in this work. Comparing with the Con-ATMOS, BV_{av} keeps almost unchanged while the $E_{ox,peak}$ becomes 3.29 MV/cm for the Con-ATMOS, and 2.94 MV/cm for the proposed ODSG-TMOS, which improves the BV_{ox} and gate oxide reliability. And the $R_{on,sp}$ is also improved by 15.1% due to the introduction of the highly doped JFET layer. More importantly, compared with the Con-ATMOS, the ODSG-TMOS shows high dynamic performance and improved SOA capability. The C_{iss} and C_{rss} of the ODSG-TMOS decrease by 69.3% and by an order of magnitude when compared to those of the Con-ATMOS, respectively. The value of Q_{gd} and Q_g are reduced by 80.6% and 72.2%, respectively. Therefore, the HF-FOM of $R_{on,sp} \cdot Q_{gd}$ and $R_{on,sp} \cdot Q_g$ for the proposed ODSG-TMOS are improved by 83.5% and 76.4%, respectively. The P_{sw} of the proposed ODSG-TMOS is 77.0% lower than that of the Con-ATMOS. In addition, the SCSOA and RBSOA are also improved. With a significantly reduced $I_{d,sat}$, the t_{sc} is 87.5% longer than that of the Con-ATMOS at the V_g of 15 V. The ODSG-TMOS can be normally turned off under a bus voltage of 1200 V and a large current of 1800 A while the Con-ATMOS fails in the turn-off process. The key parameters that have a strong influence on performance of the ODSG-TMOS are discussed, which presents a further improvement direction for the proposed structure. Considering the improved switching performance and enhanced SOA, the ODSG-TMOS is a promising candidate for high-frequency and high-power applications.

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References

[1] Kimoto T 2015 *Jpn. J. Appl. Phys.* **54** 040103
[2] Ryu S H, Krishnaswami S, O'Loughlin M, Richmond J, Agarwal A, Palmour J and Hefner A R 2004 *IEEE Electron Dev. Lett.* **25** 556

[3] Baliga B J 2008 *Fundamentals of Power Semiconductor Devices* (New York: Springer-Science)
[4] Nakano Y, Nakamura R, Sakairi H, Mitani S and Nakamuraet T 2012 *Mater. Sci. Forum* **717–720** 1069
[5] Nakamura T, Nakano Y, Aketa M, Nakamura R, Mitani S, Sakairi H and Yokotsuji Y 2011 *IEDM*, December 5–7, 2011, Washington, USA, p. 26.5.1
[6] Peters D, Basler T, Zippelius B, Aichinger T, Bergner W, Esteve R, Kueck D and Siemieniec R 2017 *PCIM Europe*, May 16–18, 2017, Nuremberg, Germany. p. 1
[7] Siemieniec R, Peters D, Esteve R, Bergner W, Kück D, Aichinger T, Basler T and Zippelius B 2017 *EPE'17 ECCE Europe*, September 11–14, 2017, Warsaw, Poland, p. 1
[8] Deng X C, Zhu H, Li X, Tong X, Gao S F, Wen Y, Bai S, Chen W J, Zhou K and Zhang B 2020 *IEEE Trans. Power Electron* **35** 8524
[9] Wu Z, Xia C, Yi B, Cheng J J, Huang H M, Kong M F, Yang H Q and Shi W K 2021 *ASICON*, October 26–29, 2021, Kunming, China, p. 1
[10] Jiang J, Huang C, Wu T and Zhao F 2019 *EDTM*, March 12–15, 2019, Singapore, p. 401
[11] Zhang J P, Chen Z X, Tu Y Y, Deng X C and Zhang B 2021 *IEEE J. Electron Dev. Soc.* **9** 713
[12] Zhang J P, Tu Y Y, Luo J Y, Peng Z F, Deng X C and Zhang B 2021 *Mater. Sci. Semicond Proc.* **134** 106026
[13] *ATLAS User's Manual: Device Simulation Software*, Silvaco Inc., Santa Clara, CA, USA, 2015
[14] Jiang H, Wei J, Dai X, Ke M, Deviny I and Mawby P 2016 *IEEE Electron Dev. Lett.* **37** 1324
[15] Zhang M, Wei J, Jiang H, Chen K J and Cheng C H 2017 *IEEE Trans. Dev. Mater. Reliab.* **17** 432
[16] Wang R D, Li Z X, Qiao M, Zhou X, Wang T Q and Zhang B 2020 *IEEE Trans. Nucl. Sci.* **67** 2009
[17] Wang Z K, Qiao M, Fang D, Wang R D, Qi Z, Li Z and Zhang B 2020 *IEEE Electron Dev. Lett.* **41** 749