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Improved RF power performance of InAlN/GaN HEMT by optimizing rapid thermal annealing process for high-performance low-voltage terminal applications

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Improved radio-frequency (RF) power performance of InAlN/GaN high electron mobility transistor (HEMT) is achieved by optimizing the rapid thermal annealing (RTA) process for high-performance low-voltage terminal applications. By optimizing the RTA temperature and time, the optimal annealing condition is found to enable low parasitic resistance and thus a high-performance device. Besides, compared with the non-optimized RTA HEMT, the optimized one demonstrates smoother ohmic metal surface morphology and better heterojunction quality including the less degraded heterojunction sheet resistance and clearer heterojunction interfaces as well as negligible material out-diffusion from the barrier to the channel and buffer. Benefiting from the lowered parasitic resistance, improved maximum output current density of 2279 mA·mm^{-1} and higher peak extrinsic transconductance of 526 mS·mm^{-1} are obtained for the optimized RTA HEMT. In addition, due to the superior heterojunction quality, the optimized HEMT shows reduced off-state leakage current of 7×10^{-3} mA·mm^{-1} and suppressed current collapse of only 4%, compared with those of 1×10^{-1} mA·mm^{-1} and 15% for the non-optimized one. At 8 GHz and V_{DS} of 6 V, a significantly improved power-added efficiency of 62% and output power density of 0.71 W·mm^{-1} are achieved for the optimized HEMT, as the result of the improvement in output current, knee voltage, off-state leakage current, and current collapse, which reveals the tremendous advantage of the optimized RTA HEMT in high-performance low-voltage terminal applications.

Keywords: InAlN/GaN, rapid thermal annealing, low voltage, RF power performance, terminal applications

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1. Introduction

With the booming development of wireless communication systems, the demand for high-performance low-voltage terminal equipment is surging, where radio-frequency (RF) power devices of power amplifiers (PAs) are required to operate at low voltage to deliver high power-added-efficiency (PAE) and moderate output power density (P_{OUT}).[1] Traditional GaAs technology has been widely adopted in low-voltage terminal applications. Nevertheless, compared with GaAs technology, GaN technology is able to deliver better PAE at the same P_{OUT} or higher P_{OUT} at the same PAE, which is conducive to realizing lower power consumption and a smaller area of the chip.[2–4] In addition, GaN technology also has superior bandwidth, which is beneficial to enable a significant reduction in the number and area of PA as well as high-speed broadband communication.[5] Thus, GaN technology has great potential for high-performance low-voltage terminal applications.

Most GaN-based RF power devices are fabricated on a mature AlGaN/GaN heterojunction to achieve high-voltage and high-power characteristics.[6–8] Besides, considering the convenience of the fabrication and relatively low cost, the formation of ohmic contacts is mainly achieved by performing rapid thermal annealing (RTA),[9–13] after the evaporation of Ti/Al/Ni/Au ohmic metals, whose RTA temperature is usually higher than 800 °C.[12,13] However, due to the limitation of relatively large sheet resistance for AlGaN/GaN heterojunction, the maximum output current density ($I_{D.MAX}$) is generally lower than 1500 mA·mm^{-1} and the knee voltage (V_{KNEE}) is also quite large, which makes it difficult to obtain high device performance at low operating voltage.[14,15] In order to enable higher $I_{D.MAX}$ and lower V_{KNEE}, both of which are important for the device to operate at low voltage, the parasitic resistance must be reduced.[16] Thus, device fabrication should be performed on a more strongly polarized heterojunction with low sheet resistance, such as an InAlN/GaN heterojunction.[17,18] On the basis of an InAlN/GaN heterojunction, the RTA process must be carefully designed because both the higher RTA temperature and longer time will cause the rough ohmic metal surface morphology and degraded heterojunction quality to induce a series of negative effects on device performance and reliability,[19–21] in spite of the lower ohmic contact resistance (R_C). As a consequence, for the InAlN/GaN heterojunction, it is vital to optimize the RTA condition and explore the appropriate one, which may be different from the optimal annealing condition for a conventional AlGaN/GaN heterojunction.

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In this work, by optimizing the RTA process including annealing temperature and time, the optimized RTA InAlN/GaN high electron mobility transistor (HEMT) exhibits lower parasitic resistance, smoother ohmic metal surface morphology, less degraded heterojunction sheet resistance, and clearer heterojunction interfaces as well as negligible material out-diffusion, which contribute to the improvement in output current, knee voltage, peak transconductance, off-state leakage current, and current collapse. Due to the improved DC and pulsed *I*–*V* characteristics, an obviously increased PAE of 62% and P_{OUT} of 0.71 W·mm^{-1} are achieved for the optimized HEMT at 8 GHz and V_{DS} of 6 V, compared with those of 51% and 0.49 W·mm^{-1} for the non-optimized one, to satisfy high-performance low-voltage terminal applications.

2. Device fabrication

The lattice-matched $In_{0.17}Al_{0.83}N$/GaN heterojunction was adopted in this work to fabricate high-performance low-voltage HEMT, whose schematic cross section is shown in Fig. 1(a). The epilayers were grown on a semi-insulating SiC substrate by metal–organic chemical vapor deposition, consisting of a 2 nm GaN cap, an 8 nm InAlN barrier, a 1 nm AlN spacer, and a GaN buffer. Room-temperature Hall measurement showed the two-dimensional electron gas (2DEG) density of 1.65×10^{13} cm^{-2} and mobility of 1512 cm^2/V·s, leading to the sheet resistance (R_{SH}) of 251 Ω/sq.

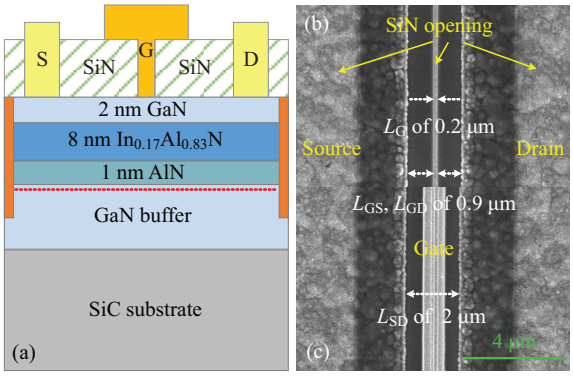


Fig. 1. (a) Schematic cross section of low-voltage InAlN/GaN HEMT. SEM characterization of the fabricated InAlN/GaN HEMT (b) before and (c) after the gate metals evaporation in the top view to determine the device size.

The fabrication process started with device isolation via boron ion implantation, followed by deposition of Ti/Al/Ni/Au ohmic metals via electron beam evaporation. Given that there exists a trade-off among low ohmic contact resistance, excellent heterojunction quality, and smooth ohmic metal surface morphology in the RTA process for the InAlN/GaN heterojunction, the RTA condition must be carefully optimized to guarantee the lowest parasitic resistance together with smoother ohmic metal surface morphology and negligible material out-diffusion. Consequently, the whole wafer was sliced into several pieces. As a reference, the optimal RTA condition for the conventional AlGaN/GaN heterojunction on our production line (860 °C, 30 s) was applied to one of the InAlN/GaN samples. And the exploration of the appropriate RTA condition for the InAlN/GaN heterojunction was based on the remaining samples. First, at a fixed RTA time of 30 s, the RTA temperature was investigated by annealing five samples in the temperature range of 800 °C–880 °C, with a temperature step of 20 °C. After that, the five annealed samples were passivated by a 120 nm SiN via PECVD, followed by the evaluation of R_C and R_{SH} via transmission-line-model (TLM) measurement. According to the TLM measurement, ohmic contact resistance is defined as the resistance between the ohmic metal and 2DEG channel, and the associated sheet resistance is regarded as the sheet resistance of the 2DEG channel. After preliminarily finding the optimal RTA temperature of 840 °C, which yields the lowest parasitic resistance among the five samples mentioned above, the RTA time was studied at the fixed temperature of 840 °C by annealing the other five samples with the time in the range of 20–60 s, with a time step of 10 s. Likewise, following the deposition of the SiN passivation layer, TLM measurement was performed to preliminarily determine the optimal RTA time of 40 s, which produces the lowest parasitic resistance among the ten samples mentioned above. However, such a two-step optimization process does not definitely lead to the most optimal RTA parameters. In order to improve the total optimization procedure, on the basis of the two-step optimization, another two optimizations of annealing time were performed at annealing temperatures of 830 °C and 850 °C, which were relatively close to the previous optimal temperature of 840 °C. With the comparison of the parasitic resistance among the samples with temperatures of 830 °C, 840 °C, and 850 °C, and various times, it is found that the lowest parasitic resistance is achieved for the annealing condition of 840 °C for 40 s, which will be shown hereinafter. Compared with the reference sample (non-optimized RTA sample), the optimized RTA sample showed lower parasitic resistance. Besides, a smoother ohmic metal surface morphology and clearer heterojunction interfaces as well as negligible material out-diffusion were also achieved for the optimized RTA sample, which will be demonstrated hereinafter. For convenience, the subsequent process was only carried out on the optimized RTA sample and the reference one. After the definition of the gate foot region via electron beam lithography, the SiN on the gate foot region was removed by CF_4 plasma dry etching. Eventually, Ni/Au gate metals were deposited via electron beam evaporation after gate head lithography. As shown in Figs. 1(b) and 1(c), a T-shaped gate was formed with a gate length (L_G) of 0.2 μm and gate width (W_G) of 2×50 μm. The source–drain spacing (L_{SD}) was 2 μm with equal gate–source and gate–drain spacing (L_{GS}, L_{GD}) of 0.9 μm.

3. Results and discussion

As mentioned above, there exists a trade-off between the lower ohmic contact resistance and less degraded heterojunction sheet resistance in the RTA process of the InAlN/GaN heterojunction,[20] both of which determine the parasitic resistance and thus the device's electrical performance. In order to lower the parasitic resistance, both the RTA temperature and time have been optimized, whose process details are described in Section 2.

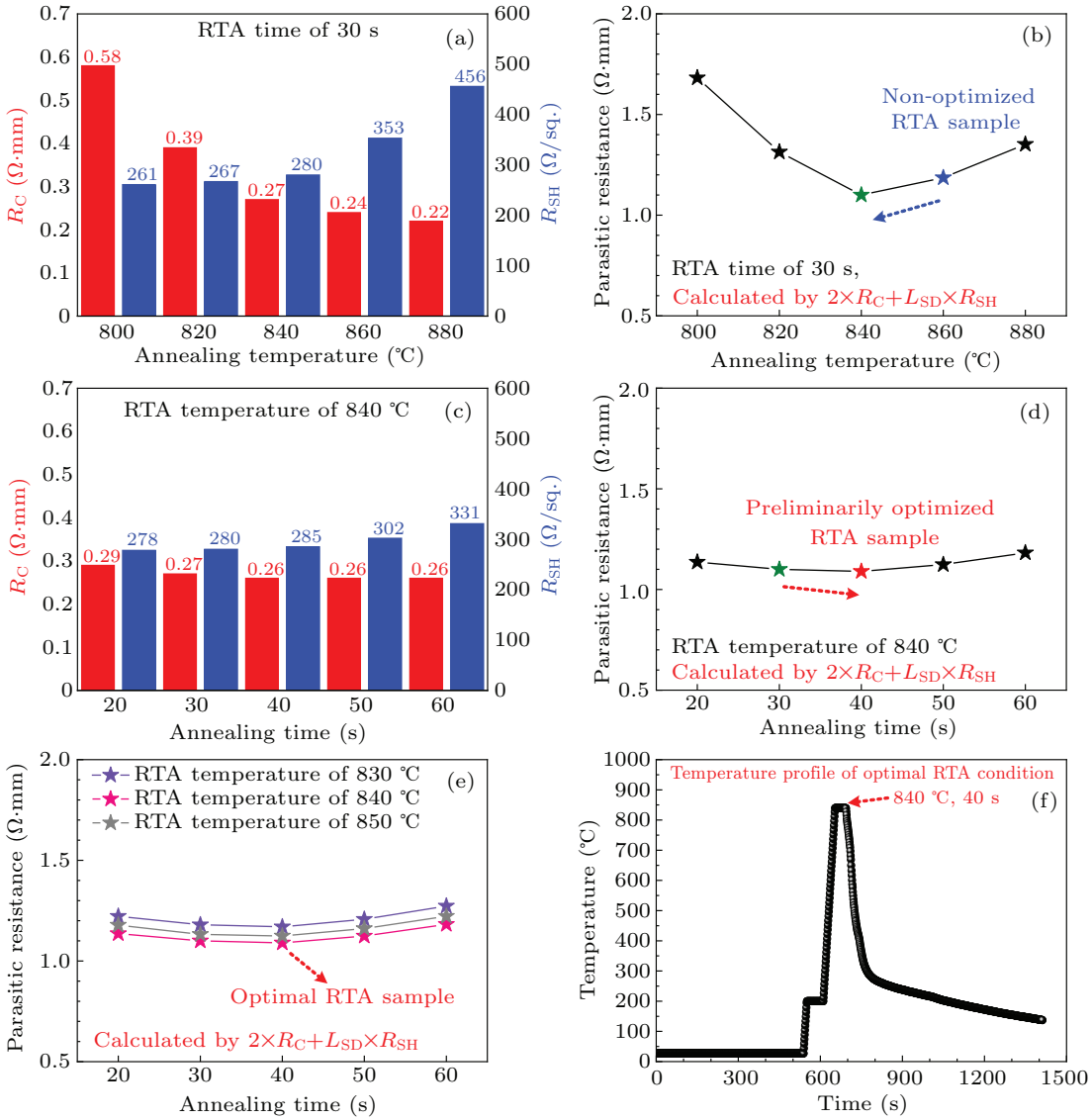


Fig. 2. Influence of RTA temperature on (a) R_C and R_{SH} as well as (b) the calculated parasitic resistance, to preliminarily determine the optimal temperature. Effect of RTA time on (c) R_C and R_{SH} as well as (d) the calculated parasitic resistance, to preliminarily determine the optimal time. (e) Comparison of the parasitic resistance among samples with temperatures of 830 °C, 840 °C, 850 °C, and various times, to finally determine the optimal RTA condition. (f) The actual temperature profile of the optimal RTA condition (840 °C, 40 s).

The corresponding TLM measurements are demonstrated in Fig. 2, to ascertain the optimal RTA condition. As shown in Fig. 2(a), as the temperature increases, the ohmic contact resistance gradually decreases, while the heterojunction sheet resistance degrades by degrees. Such two contradictory trends preliminarily determine an optimal temperature of 840 °C to yield the lowest parasitic resistance among those five samples, as shown in Fig. 2(b). On this basis, the optimal time is further investigated. As demonstrated in Fig. 2(c), the influence of time is slightly different from that of temperature. The gradual saturation of ohmic contact resistance is exhibited with the increase in time, while the heterojunction sheet resistance still degrades continuously. Similar contradictory trends preliminarily lead to an optimal time of 40 s to deliver the lowest parasitic resistance among the ten samples, as shown in Fig. 2(d). In order to more reasonably explore the optimal RTA parameters, on the basis of the previous two-step optimization process, another two optimizations of annealing time were performed at annealing temperatures of 830 °C and 850 °C, which were relatively close to the temporarily optimal temperature of 840 °C. As shown in Fig. 2(e), the sample annealed at 840 °C for 40 s shows the lowest parasitic resis-

tance. Thus, we basically reckon that the annealing condition of 840 °C for 40 s should be or very close to the most optimal one. In addition, what is noteworthy is that RTA temperature has a much stronger effect than RTA time on R_C, R_{SH}, and parasitic resistance, according to the TLM measurements. In a word, compared with the reference sample annealed at 860 °C for 30 s, the parasitic resistance is decreased as much as we can for the optimized RTA sample annealed at 840 °C for 40 s to guarantee a high-performance device. Considering that there inevitably exists a control error in temperature and time for the RTA furnace, this optimal RTA condition should be further adjusted to 840±10 °C with 40±10 s.

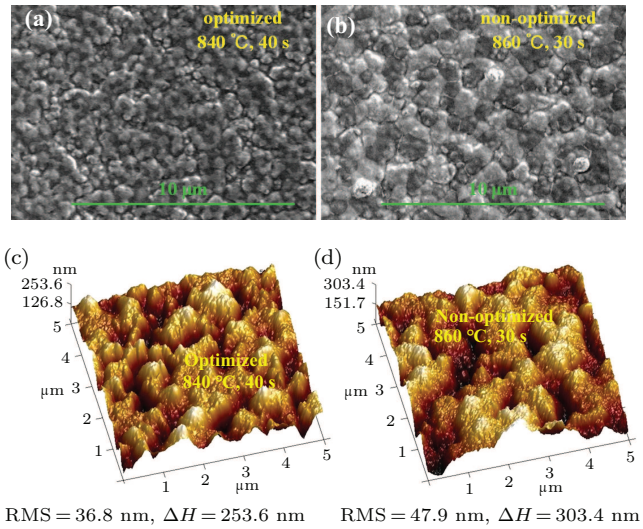


Fig. 3. (a) and (b) Qualitative characterization of the ohmic metal surface morphology by SEM as well as (c) and (d) quantificational characterization of the ohmic metal surface morphology by AFM for the optimized and non-optimized RTA samples.

Except for the evaluation of parasitic resistance, the comparison of the ohmic metal surface morphology and other heterojunction quality is performed between the optimized and non-optimized RTA samples. Figure 3 demonstrates the ohmic metal surface morphology of both samples, characterized by scanning electron microscopy (SEM) and atomic force microscopy (AFM). Similar to the cases reported in other works, the bumpy ohmic metal surface with bulges of various sizes is shown for both samples, which is an inevitable annoying phenomenon in the RTA process.[12,22,23] However, compared with the non-optimized RTA sample, the optimized one has smoother ohmic metal surface morphology whose root-mean-square (rms) surface roughness and maximum height variation of bulges (ΔH) are obviously reduced, which is attributed to the less Ni-Al alloy aggregation by relatively lower RTA temperature.[12,21] Besides the evaluation of the degradation for heterojunction sheet resistance mentioned above, another heterojunction quality of both samples is compared in Fig. 4. By high-resolution transmission electron microscopy (HRTEM) measurement, clearer heterojunction interfaces are shown for the optimized RTA sample. More importantly, due to the relatively low annealing temperature, there is negligible element out-diffusion from the barrier to the channel and buffer for the optimized one, which is characterized by an energy dispersive spectrometer (EDS) and indicates the better material quality and fewer defects introduced during the optimized RTA process. The fewer defects imply the suppressed off-state leakage current and current collapse for the optimized RTA condition, which will be shown hereinafter. On the contrary, the reference annealing condition (860 °C for 30 s) indeed causes more severe heterojunction quality degradation. However, such degradation contributes to the reduction in ohmic contact resistance, probably due to the introduction of more defects to facilitate the electron transition.

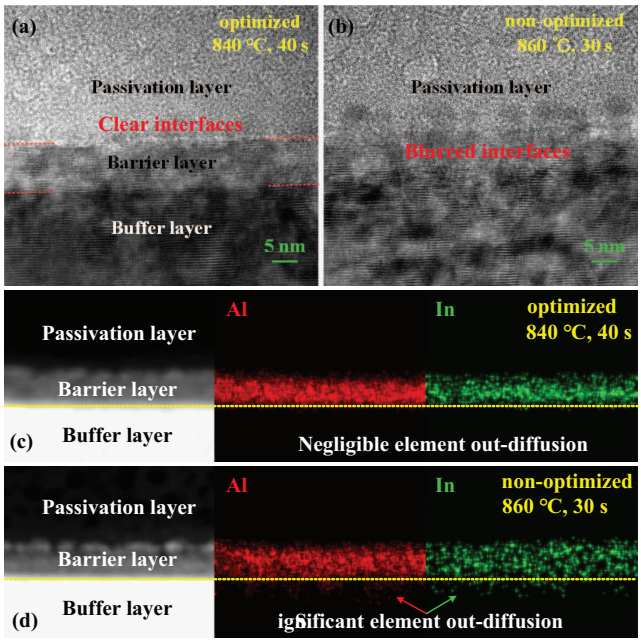


Fig. 4. (a) and (b) HRTEM characterization of the heterojunction structure as well as (c) and (d) EDS analysis of element out-diffusion for the optimized and non-optimized RTA sample.

A Keithley 4200 semiconductor parameter analyzer was used for DC and pulsed I–V measurements. A comparison of transfer characteristics at V_{DS} of 6 V is shown in Fig. 5(a), demonstrating the peak extrinsic transconductance ($g_{m.peak}$) of 526 mS·mm^{-1} and 473 mS·mm^{-1} for the optimized and non-optimized RTA HEMT, respectively. Besides, compared with the reference HEMT with off-state drain leakage current ($I_{d.off}$) of 1×10^{-1} mA·mm^{-1}, the $I_{d.off}$ of 7×10^{-3} mA·mm^{-1} is achieved for the optimized RTA HEMT. Figure 5(b) demonstrates the output characteristics of both devices, showing that the higher $I_{D.MAX}$ of 2279 mA·mm^{-1} and lower V_{KNEE} of 3.8 V are obtained for the optimized HEMT, compared with those of 2066 mA·mm^{-1} and 4.2 V for the non-optimized one. As demonstrated in Figs. 5(c) and 5(d), the pulsed I–V characteristics are characterized at gate voltages of 2 V and 0 V, with quiescent bias points of (V_{GSQ}, V_{DSQ} = 0 V, 0 V) and (V_{GSQ}, V_{DSQ} = −6 V, 10 V). The optimized HEMT exhibits the current collapse ratio of 4%, compared with that of 15% for the non-optimized one. For the optimized RTA HEMT,

the increased $I_{D.MAX}$ and $g_{m.peak}$ as well as reduced V_{KNEE} are attributed to the lowered parasitic resistance. In addition, the better heterojunction quality contributes to the suppression of off-state leakage current and current collapse.

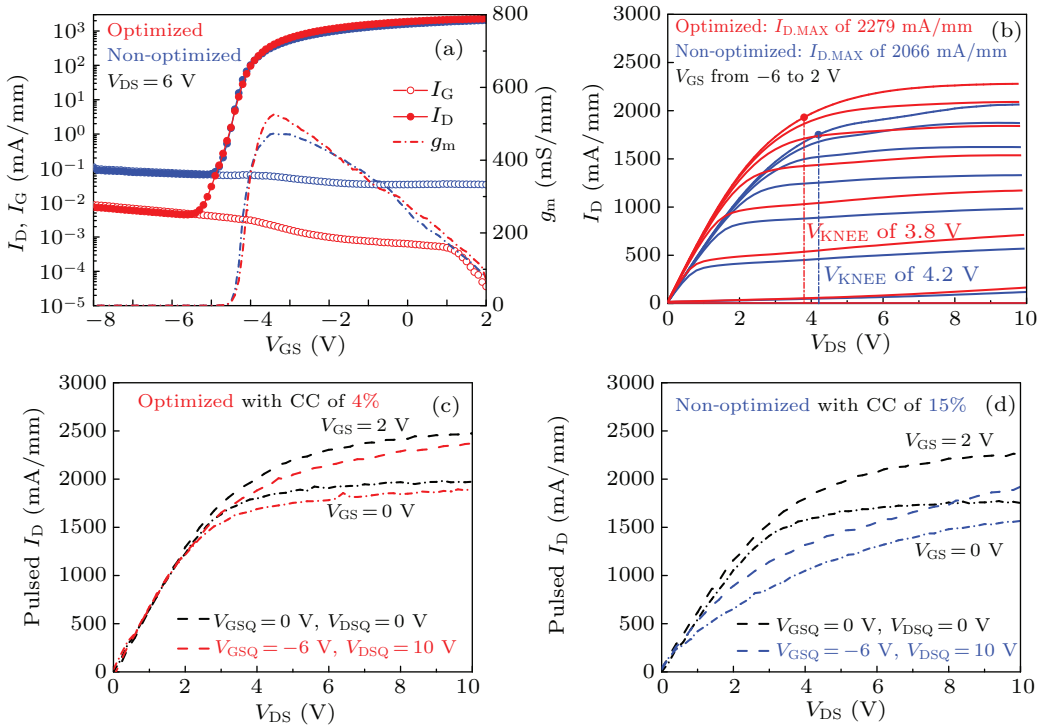


Fig. 5. Comparison of (a) transfer characteristics and (b) output characteristics between the optimized and non-optimized RTA HEMT. Pulsed *I*–*V* characteristics of the (c) optimized and (d) non-optimized device.

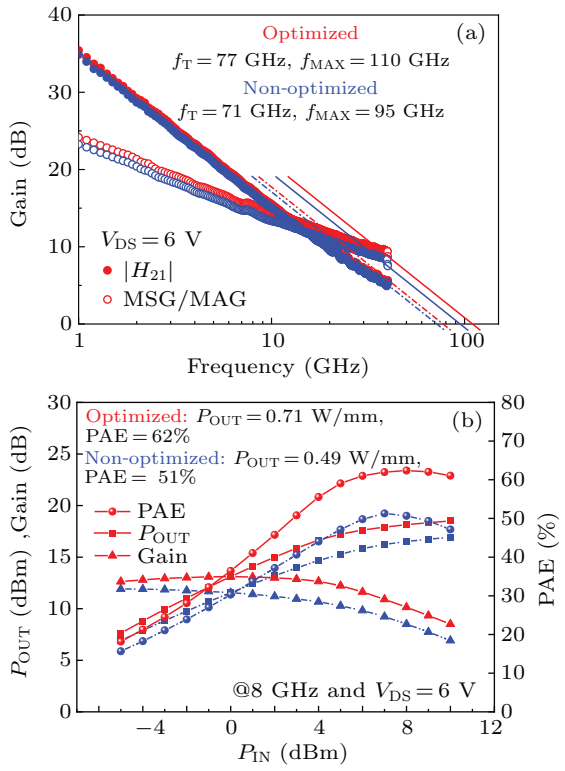


Fig. 6. Comparison of (a) small signal characteristics and (b) low-voltage large signal characteristics between the optimized and non-optimized RTA HEMT.

The small signal characteristics were characterized from 1–40 GHz for both devices, using an Agilent 8363B vector network analyzer calibrated with a short-open through calibration standard. As shown in Fig. 6(a), by extrapolating of the short circuit current gain ($|H_{21}|$) and the maximum stable gain/maximum available gain (MSG/MAG) curves using −20 dB/decade slopes, f_T/f_{MAX} values of 77/110 GHz and 71/95 GHz are achieved for the optimized and non-optimized RTA HEMT biased at V_{DS} of 6 V, respectively. The low-voltage large signal characterization was performed in a continuous wave using an on-wafer load-pull system. Both the source and the load impedance were tuned to maximize PAE. At 8 GHz and V_{DS} of 6 V, an improved PAE of 62% together with an increased P_{OUT} of 0.71 W·mm^{-1} is achieved for the optimized RTA HEMT, as shown in Fig. 6(b), as a result of the improvement in output current, knee voltage, off-state leakage current, and current collapse.

Finally, the comparison of ohmic contact resistance, off-state leakage current, current collapse, P_{OUT} and PAE between our fabricated InAlN/GaN HEMT and the state-of-the-art ones is performed, which can be seen in the table below. Obviously, our fabricated InAlN/GaN HEMT demonstrates lower ohmic contact resistance as well as suppressed off-state leakage current and current collapse. More importantly, a decent PAE and P_{OUT} are achieved at a low operating voltage for this InAlN/GaN HEMT, appealing to low-voltage terminal applications.

Table 1. Comparison of ohmic contact resistance, off-state leakage current, current collapse, PAE, and P_{OUT} for InAlN/GaN HEMTs.

Ref.	Organization	R_C (Ω·mm)	Off-state leakage (mA·mm^{-1})	Current collapse	Operating voltage (V) /frequency (GHz)	PAE	P_{OUT} (W·mm^{-1})
[24]	III–V Laboratory	0.15	–	6%	30 / 10	51%	10.3
[25]	ETH	0.48	3	–	–	–	–
[26]	Lille University of Science and Technology	0.59	3.78×10^{-1}	16%	10 / 18 15 / 18	34% 26%	2.4 2.9
[27]	University of Notre Dame	0.38	1	16%	–	–	–
[28]	MIT	0.6–0.7	7	–	–	–	–
[29]	ETH	0.3	4.4×10^{-3}	–	–	–	–
[30]	BAE Systems	0.2	3×10^{-2}	–	10 / 86	12.7%	–
[31]	NTU	0.2	1	–	–	–	–
[32]	NTU	0.2	3	15%	–	–	–
[33]	University of Delaware	0.6	2.41×10^{-2}	–	–	–	–
[34]	Xidian University	0.4	6×10^{-3}	4%	–	–	–
This work	**Xidian University**	**0.26**	$\mathbf{7\times10^{-3}}$	**4%**	**6/8**	**62%**	**0.71**

4. Conclusions

In conclusion, improved low-voltage RF power performance of InAlN/GaN HEMT is realized via an optimized RTA process to satisfy high-performance terminal applications. This optimal annealing condition (840 °C with 40 s) is explored via adjusting the RTA temperature and time to achieve the lowest parasitic resistance, which leads to the improved output current density and higher peak transconductance as well as reduced knee voltage. Moreover, compared with the reference HEMT, the optimized one demonstrates smoother ohmic metal surface morphology and better heterojunction quality including the less degraded heterojunction sheet resistance and clearer heterojunction interfaces as well as negligible material out-diffusion, which contributes to the suppression of off-state leakage current and current collapse. Due to the improved DC and pulsed *I*–*V* characteristics, an obviously enhanced PAE of 62% and P_{OUT} of 0.71 W·mm^{-1} are achieved at V_{DS} of 6 V for the optimized RTA HEMT, indicating the great potential of the optimized RTA HEMT in high-performance low-voltage terminal applications. Considering that there inevitably exists a control error in the temperature and time for the RTA furnace, this optimal RTA condition should be further adjusted to 840±10 °C with 40±10 s. RTA temperature or time beyond the upper limit of this optimal condition leads to severer degradation of heterojunction quality (including the substantially degraded heterojunction sheet resistance, blurred heterojunction interfaces as well as significant material out-diffusion) and rougher ohmic metal surface morphology, and RTA temperature or time not reaching the lower limit of this optimal condition causes higher ohmic contact resistance. However, a decent balance among low ohmic contact resistance, excellent heterojunction quality, and smooth ohmic metal surface morphology is enabled by this optimal RTA condition, thus achieving the improvement in DC, pulsed *I*–*V*, and RF power performance.

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