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Design and investigation of doping-less gate-all-around TFET with Mg_2Si source material for low power and enhanced performance applications

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Metal–oxide–semiconductor field-effect transistor (MOSFET) faces the major problem of being unable to achieve a subthreshold swing (SS) below 60 mV/dec. As device dimensions continue to reduce and the demand for high switching ratios for low power consumption increases, the tunnel field-effect transistor (TFET) appears to be a viable device, displaying promising characteristic as an answer to the shortcomings of the traditional MOSFET. So far, TFET designing has been a task of sacrificing higher ON state current for low subthreshold swing (and *vice versa*), and a device that displays both while maintaining structural integrity and operational stability lies in the nascent stages of popular research. This work presents a comprehensive analysis of a heterojunction plasma doped gate-all-around TFET (HPD-GAA-TFET) by making a comparison between Mg_2Si and Si which serve as source materials. Charge plasma technique is employed to implement doping in an intrinsic silicon wafer with the help of suitable electrodes. A low-energy bandgap material, *i.e.* magnesium silicide is incorporated as source material to form a heterojunction between source and silicon-based channel. A rigorous comparison of performance between Si-based GAA-TFET and HPD-GAA-TFET is conducted in terms of electrical, radio frequency (RF), linearity, and distortion parameters. It is observable that HPD-GAA-TFET outperforms conventional Si-based GAA-TFET with an ON-state current (I_{ON}), subthreshold swing (SS), threshold voltage (V_{th}), and current switching ratio being 0.377 mA, 12.660 mV/dec, 0.214 V, and 2.985×10^{12}, respectively. Moreover, HPD-GAA-TFET holds faster switching and is more reliable than Si-based device. Therefore, HPD-GAA-TFET is suitable for low-power applications.

Keywords: subthreshold, Mg_2Si, heterojunction, charge plasma, gate-all-around (GAA)

PACS: 73.40.Lq **DOI:** 10.1088/1674-1056/acd5c0

1. Introduction

The tunnel field-effect transistor (TFET) uses quantum tunneling to yield a promising path through the roadblocks in the semiconductor device domain, bypassing the Boltzmann limit of subthreshold swing (SS), i.e., the restraint enforced on traditional metal–oxide–semiconductor field-effect transistor (MOSFET) by the equation $2.3 \times kT/q$.[1] Today' technology benefits from very-large-scale integration (VLSI). Semiconductor electronic devices, from trivial power supply devices like child's toys to giant structures orbiting the planet, are collecting information vital to human functions with an accuracy that was never dreamed of decades ago.

It has been widely introduced and studied in academic circles, and the SS value displayed by TFETs is lower than 60 mV/dec, which is the trend that the device introduced in this paper can keep pace with. This is possible because the "tunneling mechanism" TFETs are used for carrier transportation, which is completely different from what happens in MOSFETs. MOSFETs use thermionic emission as their carrier transportation mechanism, while TFETs take band-to-band tunneling as their carrier transportation mechanism,[1] where there is no potential barrier needed to overcome for an electron to move from valence band to conduction band.[2] The only parameter we care about is the probability density of the particle being found on the other side of the potential barrier, which passes through the barrier via 'tunneling effect'. For all practical purposes, indirect semiconductor carriers will undergo indirect tunneling.[1] Therefore, replication of the BTBT phenomenon is realized by superimposing a cylindrical mesh to simulate the current. It is notable that BTBT is effectively observable at the source channel junction but not at the entire channel.[3]

It is worthwhile to note that the modifications we have made to the basic TFET, which are discussed briefly and in greater detail further in the work, have led to our device having a rather low operating range, along with a substantially high value of ON-current, which is of particular interest to us. The usual results render TFETs incapable of driving other devices. The results obtained from our device are an encouraging step towards improving the driving factor for TFETs.

This paper also describes the adoption of two quite new design factors (with respect to TFETs). Firstly, plasma doping is used to replace other traditional doping methods and secondly, Si and Mg_2Si are used as source material for our device. The material used and doping method are discussed in detail in Section 3. What is followed is a detailed study of

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the overall physical construction of the HPD-GAA-TFET concluded in Section 3, containing a detailed technical review of all device parameters essential to prove the feasibility of this construction.

The conventional TFETs are found to have a low ON-state current, which falls short of the ITRS requirement.[4] Vishnoi and Kumar[5] proposed an analytical model of GAA-TFET but the problem of delayed saturation still pertains.[5] Madan *et al.*[6] reported the influence of hetero-dielectric behavior in GAA-TFET that enhances the ON-state current; but incorporation of hetero-dielectric degrades parasitic capacitance.

Magnesium silicide (Mg_2Si) is a naturally occurring non-toxic compound with a relatively low band gap, making it a promising candidate for using source material in TFETs[7] and also for thermoelectric applications.[8] The ability to effectively dope Mg_2Si for n-type or p-type conductivity makes it a suitable material for forming heterojunctions with silicon. Furthermore, the unique properties of Mg_2Si make it an attractive material for addressing environmental challenges, such as reducing greenhouse gas emissions and mitigating the influence of limited energy resources.[8] The energy band-gap of Mg_2Si is 0.77 eV lower than other silicide's, which is attributed to several factors. One contributing factor is the energy band alignment with respect to the vacuum level. Additionally, there are discontinuities in the energy bands at the interface of the source and in channel regions, which reduces the width of the tunnelling barrier. The presence of these discontinuities further lowers the energy band-gap of Mg_2Si. Thus, incorporation of low bandgap material in source region leads heterojunction to enhance the tunnelling of charge carriers thus improving its ON-state current.

Kumar and Raman[9] proposed Si-based GAA vertical nanowire TFET by charge plasma method.

The proposed architecture uses the charge plasma approach to create P^+-doped and N^+-doped regions in a semiconductor device. This approach is based on two key requirements:[10]

(i) The thickness of the silicon channel must be smaller than the Debye length (L_D). This requirement ensures that the distribution of the charge carriers within the silicon film is governed by the induced charge carriers, resulting from the differences in work function between the source/drain metal contacts and the intrinsic semiconductor region. The Debye length is a parameter that characterizes the extent of electrostatic screening in plasma. In this case, it determines the range over which the induced charges can affect the distribution of charge carriers.

(ii) The work function of the drain (source) metal electrode must be less (more) than that of the intrinsic silicon, resulting in the formation of N^+-doped (P^+-doped) regions. By appropriately selecting the work function of the metal contacts, the charge plasma approach can induce an excess of either holes or electrons in the semiconductor, resulting in the desired P^+ doping or N^+ doping. Hence, to improve the ON-state current of TFETs and electrical parameters, the two above-mentioned methods were employed in the proposed device to enhance the device characteristics.

In this study, to address the issue of low-ON state current, we employ a gate-all-around (GAA) structure to provide better electrostatic control over the channel, and use a novel low bandgap material, magnesium silicide (Mg_2Si), as the source material to enhance the tunneling of charge carriers thereby improving the current. Additionally, the requirement for an abrupt junction at the source-channel interface in TFET devices presents a challenge that is addressed by using a doping-less technique. The study compares the electrical, RF, linearity, and distortion parameters of Si-based GAA-TFET and HPD-GAA-TFET.

2. Device dimensions

Figure 1 presents the cross-sectional layout of the device. It is evident from Fig. 1 that the general construction is of GAA type[11] and the reasons for this design along with its merits are discussed at length in this section.

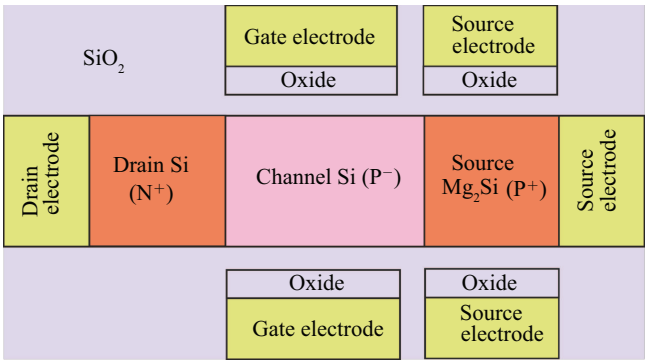


Fig. 1. Schematic diagram of HPD-GAA-TFET.

The stability, power consumption, and I_{ON}/I_{OFF} current of any semiconductor device depend on the measure of gate controllability achievable for them. For TFET constructed using the GAA structure,[12] gate controllability is achieved by choosing a suitably thick diameter preferably lying in a range marked by boundaries beyond which these essential device characteristics tend to degrade. Furthermore, the characteristic length (L_d) depicted by Eq. (1) is miniscule for a typical GAA structure, implying that for the same V_{GS}, higher quantity of inversion layer charge is achievable in the channel region, a factor which gives to the gate, considerable electrostatic control of the channel, leading to a higher electric field in the tunneling region. The end result of this endeavor is an enhanced

drain current.[1] The above deliberations are modelled as follows:

$$L_{\mathrm{d}} = \sqrt{\frac{T_{\mathrm{Si}}^2 \ln(1+2T_{\mathrm{ox}}/T_{\mathrm{Si}})\varepsilon_{\mathrm{Si}}}{4\varepsilon_{\mathrm{Si}}}}, \tag{1}$$

where T_{Si} is the silicon film thickness and T_{ox} is the oxide thickness. We choose a diameter of 5 nm for our model[13] that provides us with the optimum results discussed in the results and analysis section. Further scrutinizing, we observed that the cylindrical construction leads to a greater density of tangential equipotential lines closer to the source.[14] An accumulation such as this leads to stronger band bending, effectively shortening the tunneling path and inevitably leading to the favorable result of increased tunneling current.

A cursory glance at this rather detailed layout of the device gives us the following useful information: the channel extends over a length of 22 nm, with an intrinsic concentration of 10^{15} cm^{-3}. The electrodes at the drain–source periphery have work functions of 3.9 eV and 5.93 eV respectively, which when supplied with a suitable bias (in Table 1) initialize the tunneling process thus providing a steady output current. A closer look reveals this tunneling to take place between 40 nm to 54 nm. Apart from the undoped regions, which is Si, we observed an oxide layer of SiO_2, 1-nm thick at the gate–substrate interspace, acting as an excellent insulator. As electrons accumulate in the drain regions and for maintaining uniform doping levels, complying to our profile of P^+–P^-–N^+, we keep the drain electrode exposed. Furthermore, to reduce the ambipolar current of the device, the drain region is not wrapped.

Table 1. Device parameters.

Parameter	Value
Gate length	22 nm
Drain length	20 nm
Source length	20 nm
Oxide thickness	1 nm
Work-function of gate	4.5 eV
Work-function of source	5.93 eV
Work-function of drain	3.9 eV

These dimensions, as well as each specified region of the device in question, are mapped out on the Silvaco TCAD Atlas software interface with all numerical evaluations pertaining to essentiality required parameters carried out through appropriate models, which are discussed in more detail below.

The non-local BBT model, Shockley–Read–Hall recombination model (for recombination and generation effects), Auger model, CVT model (for Lombardi mobility), bandgap narrowing (BGN), and Fermi–Dirac statistics are used to enhance our outcomes. Along with it, we use the Newton–Richardson method to solve analytical problems. The velocity saturation of high electric field is modeled by the field-dependent mobility (FLDMOB) model and the concentration-dependent low field mobility is handled by CONMOB.[15]

3. Results and analysis

3.1. Charge plasma method

Although the ion implantation method is widely used for doping impurities of desired concentration in a semiconductor wafer, it causes a slew of problems that may be overlooked during the construction of a normal device, but it causes serious problems for a device as specialized as the one discussed here.[16]

Ion implantation primarily depends on the extraction energy that determines the volume of ions to be extracted for implantation. For a device of dimensions such as ours, (having a channel length of 22 nm), low extraction energy is required to deposit a suitably thin layer of dopant. This, however, significantly reduces the number of ions to be extracted, resulting in greater inter-ionic distances. A larger ionic gap leads to greater ion mobility, giving way to high-energy ion collisions, causing interstitial defects on the doped surface. These defects reduce the level of uniform doping originally desired. The problem of ion implantation method for device doping such as the one described here, is one of many problems arising from the variations of extraction energy and ion acceleration, both of which are to control. Hence, we employ plasma doping, a method sufficiently well developed and reliable to achieve the desired concentration of the dopant in the source, channel, and drain region of the device. The magnitudes are discussed further (in Table 2).

For each device variant (Mg_2Si and Si as source), bias electrodes of palladium and hafnium having work functions, 5.93 eV and 3.9 eV respectively are formed at the point where the bias is applied and at the periphery of the plasma–substrate region respectively. When the bias electrode is subjected to an appropriate excitation voltage, Si^+ ions irradiate the substrate with near-perfect uniformity. Compared with the traditional ion-implantation method, the configuration used utilizes low-energy plasma and provides a higher I_{ON} output without adding any physical impurities.

Table 2. Parameters of Mg_2Si.[17]

Parameter	Value
Relative permittivity	20
Electron mobility	370 cm$^2 \cdot$V$^{-1} \cdot$S^{-1}
Hole mobility	70 cm$^2 \cdot$V$^{-1} \cdot$S^{-1}
Energy bandgap	0.77 eV
Electron affinity	3.59 eV
Effective mass of electron	0.22 m_0
Effective mass of hole	0.51 m_0

Here m_0 is the rest mass.

3.2. Source material investigation

Figure 2(a) presents the validation curve of numerical calculation performed by using the TCAD tool. The simulation models are calibrated with the reference data from experimental research that has been published.[18] In order to calibrate the non-local BTBT model, its tunnelling mass is adjusted from their initial value to a regulated value, i.e., me.tunnel = 0.22 m_0 and mh.tunnel = 0.51 m_0, where m_0 is the electron rest mass. A good match between simulation data and experimental data validates the numerical calculation. The merits of using Mg_2Si as a source are discussed in this subsection, starting with the choice to use it over other intermetallic source dopants. The Mg_2Si tends to be interstitial Mg, leading to n-type conductivity (preferred in our case), and it also reduces the problem of lattice mismatching with the silicon substrate, an issue that would be caused if any other material were to be used. Furthermore, its display of a rather low electron affinity (3.59 eV) is complemented by an even lower energy band gap of 0.77 eV. These factors are reasons that lead to the increase of band discontinuities of silicon, and are suitable for increasing the ON current through a significant factor.[7,19] This significance is comparable to that in the case where only silicon is used as a source. It has been investigated that Mg_2Si can be doped into both p-type and n-type,[20,21] making it an ideal option for Si heterojunction TFETs. Figures 2(b) and 2(c) show variations of energy band for both the proposed device i.e., HPD-GAA-TFET and Si-based GAA-TFET under OFF state and ON state. The above statements are understood and proven visually by Figs. 2(b) and 2(c), which show a clearer picture of the band discontinuities and energy gap levels sported by Mg_2Si. This is due to the formation of a staggered type-II heterojunction at the source-channel junction, which creates a narrow energy barrier.[22] Here, it is easy to glean those larger discontinuities between conduction and valence bands that result in abrupt band bending at the Mg_2Si and Si junction which leads to the lowering of tunneling barrier width for HPD-GAA-TFET. This improves the probability of inter-band tunneling of electrons and hence increasing the ON state current of the HPD-GAA-TFET.

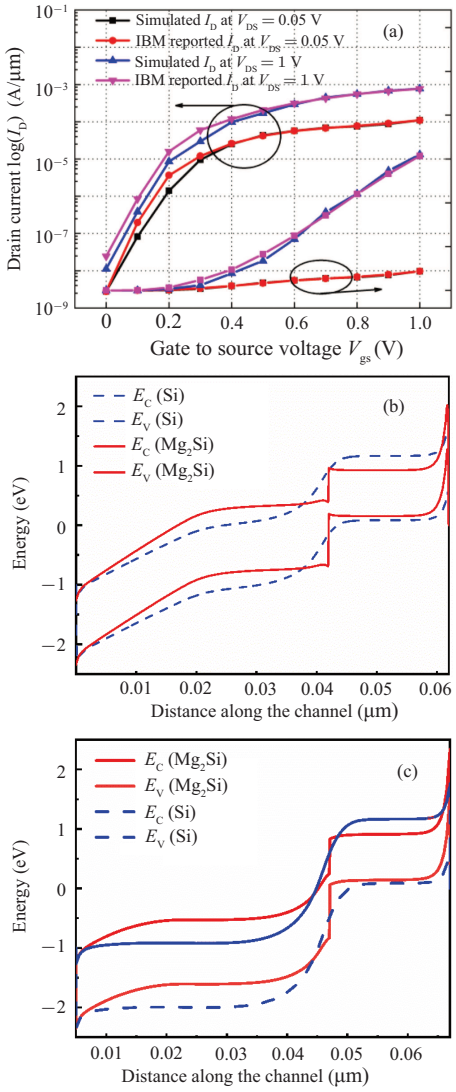


Fig. 2. (a) Comparison between simulated and experimental data. (b) Energy band diagram of HPD-GAA-TFET and Si-based GAA-TFET in OFF state (V_{GS} = 0 V and V_{DS} = 1 V), (c) the ON state (V_{GS} = 1 V and V_{DS} = 1 V).

3.3. Electrical performance

We begin by scrutinizing Figs. 2(b) and 2(c) in which are plotted the curves of band energy *versus* distance along the channel in OFF state and ON state. Figures 3(a) and 3(b) exhibit electron and hole concentrations due to plasma doping across the HPD-GAA-TFET device clearly indicating the doping concentration of 10^{20} cm^{-3} in source region and of 10^{18} cm^{-3} in channel region in the ON state. The diagrams essentially clearly display the band bending between source and channel. It is worthwhile to take a pause and acknowledge the non-local BBT model via which an accurate prediction of tunneling rate is made possible, especially in the case of discontinuous band energy level as we see further in the following Fig. 4.

Figure 4 reflects the contour of nonlocal BTBT rate of electrons for HPD-GAA-TFET. It is observable that the band bending for the case of Mg_2Si used as a source is much steeper than that in Si, which supplies easier tunneling from source to channel in the case of the former. Another observation note is the downward bending of bands on the application of positive V_{GS}. Another striking contrast between the two materials is the abrupt discontinuity in band energy in the case of Mg_2Si against the relative smoothness of Si. This reflects in the charge distribution, which in turn determines the electric field contributions for both materials. The continuity of energy bands in Si-based GAA-TFET results in a continuous distribution of charge from the conduction band of the source

to the conduction band of the channel. This leads to a more pronounced distribution of electric field at the interface in Si-based GAA-TFET than that in HPD-GAA-TFET, as indicated evidently from Fig. 5(a). We observed two peaks at the junctions between the drain-channel region and the source-channel region, owing to charge accumulation at those points. This observation simply verifies the band gap variation for the two materials discussed above.

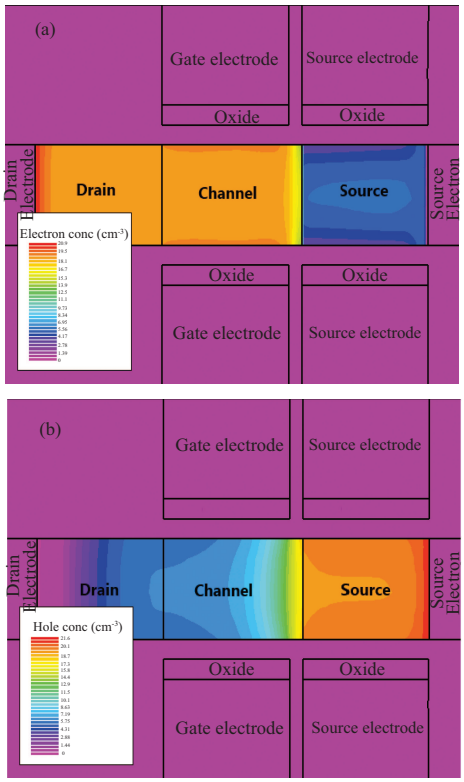


Fig. 3. Charge carrier concentration in HPD-GAA-TFET in terms of (a) electron concentration and (b) hole concentration.

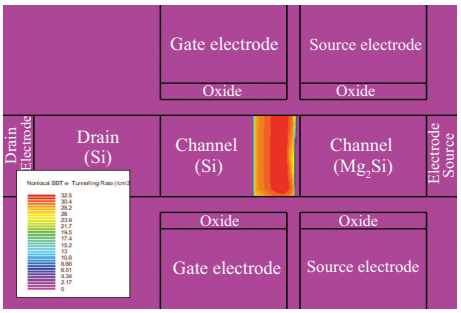


Fig. 4. Non-Local BTBT electron tunneling rate along channel.

The reliability of TFET devices, particularly in short-channel configurations, is of concern owing to the presence of a high electrostatic field at the tunneling junction. This high field leads to the generation of defects at the interface between the semiconductor and oxide material. The peak of vertical electrostatic field at tunnelling junction helps valence electrons to elastically tunnel from source P+ side to conduction band of channel and then these electrons are heated by high vertical electrostatic field to generate interface traps, which further shifts the threshold voltage and degrades drive current.[23] Higher vertical electrostatic field is mainly due to trivalent doping in source region. Thus, interface traps are generated and need to be examined while analyzing the reliability of tunnel FETs.

Therefore, in order to analyze the reliability of both the proposed devices, ITC density is considered at silicon–oxide interface. Figure 5(b) shows the maximum values of lateral and vertical electrostatic-field components for Si-based GAA-TFET and HPD-GAA-TFET. The electron band-to-band tunneling (BTBT) rate is influenced by the lateral electric fields, one of which is perpendicular to the channel plane and the other is along the channel direction. This results in a change in the tunneling current. On the contrary, the vertical electric fields perpendicular to the channel plane and perpendicular to the channel direction, will affect the device reliability, including increased gate leakage current and generation of interface traps. Therefore, a lower vertical electric field and higher lateral electric field are desirable for improving device reliability. It is evident from Fig. 5(b) that vertical electric field component of HPD-GAA-TFET is lesser than that of Si-based GAA-TFET which reflects better reliability.

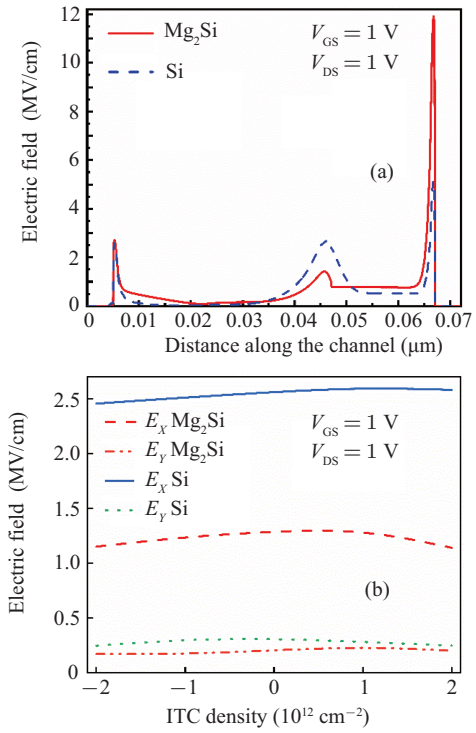


Fig. 5. (a) Electric field varying with distance from channel, (b) lateral and vertical components *versus* ITC density.

According to the above analysis we turn to the next stage, that is, a detailed study of device transfer characteristics at two different values of V_{DS}, namely 0.1 V and 1 V. It is evident from Fig. 6(a) that on application of 1-V drain to source bias, the HPD-GAA TFET gives a higher ON current with Mg_2Si as a source material. The result with Si on the other hand lags

by a significant factor. This clear difference in performance is caused by the lower energy bandgap observed for Mg_2Si and other factors such as minimizing tunneling resistance and lower effective mass which in turn leads to the increase in tunnel mobility.[24] It is also apparent from Fig. 6(a) that increasing V_{GS} leads the ON current to increase greatly. This occurs owing to further shortening of the tunnel path which shows an exponential dependence on V_{GS}. In addition, when the drain source bias is 0.1 V in Fig. 6(b), the performance of Mg_2Si is once again better than that of Si with SS of 12.6 mV/dec, I_{ON} of 0.033 mA and switching ratio of 2.280×10^{12}; the latter displays an SS of 18.7 mV/dec, an I_{ON} of 0.038 μA, and a switching ratio of 1.7×10^{10}. The subthreshold swing is calculated from

$$\mathrm{SS} = \frac{\partial V_{GS}}{\partial \log_{10} I_D}. \tag{2}$$

Finally, the V_{th} value with the application of 1-V V_{DS} is 0.214 V for Mg_2Si and 0.3 V for Si. We see that HPD-GAA-TFET (Mg_2Si) performs better by a significant margin. The ambipolar behavior at negative V_{GS} is suppressed to a greater extent which can be observed in Fig. 7(a). This ambipolar current is well below the ITRS (International Technology Roadmap for Semiconductors) limit of 10 pA/μm.

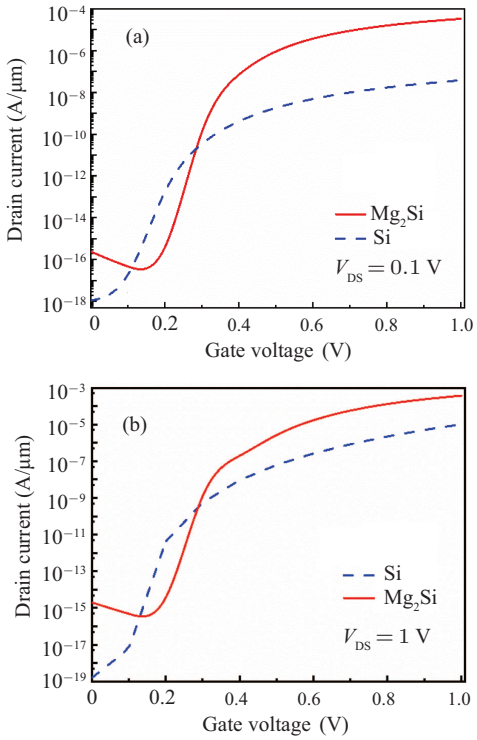


Fig. 6. The I_d–V_{GS} curve of HPD-GAA-TFET and Si-based GAA-TFET for $V_{DS} = 0.1$ V (a) and 1 V (b).

In the context of deep submicron MOS devices, the phenomenon of quantum confinement arises from increased doping levels and reduced gate oxide thickness. This leads to a modification in the potential well formed in channel in the inversion process. As a result of this confinement, the maximum density of carriers is displaced from the interface, and the gate capacitance is significantly changed. These quantum effects play a crucial role in determining the overall device characteristics. The Hansch model[15] accurately describes quantum mechanical confinement in MOS devices, particularly near the gate oxide interface. The HANSCHQM parameter must be specified in the MODELS statement to incorporate the correction into a simulation model. The Hansch correction model is an adaptation of the density of states that accounts for the influence of quantum confinement on the distribution of states as a function of depth from the Si/SiO_2 interface, and is expressed as

$$N_C^* = N_C \left\{ 1 - \exp\left[-\left(\frac{z}{\lambda} \right)^2 \right] \right\}, \tag{3}$$

where N_C is the standard density of states, z is the height below interface, and λ is the user-defined parameter.

Figure 7(b) shows the transfer characteristics of Si-based GAA-TFET with and without quantum confinement model at $V_{DS} = 0.7$ V. However, it can be observed from the figure that quantum confinement model is not dominant in I_D–V_{GS} curve.

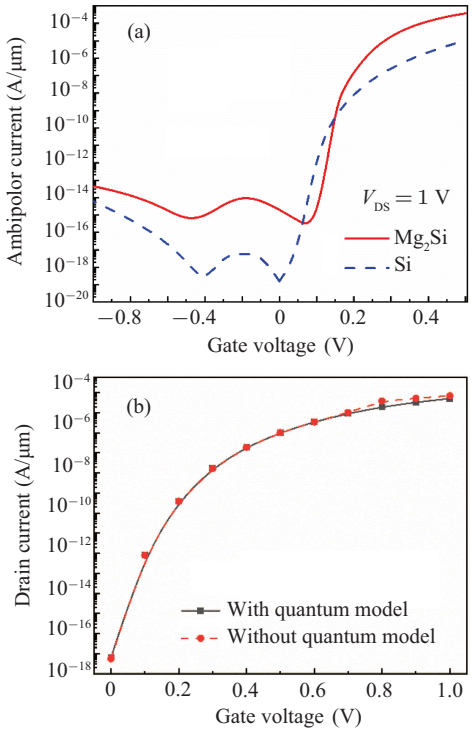


Fig. 7. (a) Ambipolar current *versus* gate voltage of HPD-GAA-TFET and Si-based GAA-TFET, (b) I_D–V_{GS} curve of Si-based GAA-TFET with and without quantum model at $V_{DS} = 0.7$ V.

3.4. Radio frequency, linearity, and distortion analysis

The primary reason for performing linearity analysis on a device is to validate its performance in radio frequency integrated iircuits (RFICs). Intermodulation distortions within the device are the primary cause of its deviation from stable linear performance, and the text that follows here will investigate

the key factors that dictate them. We begin with studying the transconductance ($g_{\rm m}$) defined as follows:

$$g_{\rm m} = \frac{\partial I_{\rm D}}{\partial V_{GS}}. \tag{4}$$

A parameter whose importance lies in the fact that it determines the current conversion rate of a device as an amplifier. Figure 8 shows that $g_{\rm m}$ of HPD-GAA-TFET is greater than Si-based GAA-TFET for linear application of $V_{\rm GS}$. From this graph, we also notice that $g_{\rm m}$ increases very slowly for both Si-based and Mg_2Si-based device after a certain $V_{\rm GS}$. This is favourable for maintaining linearity with reasonable stability in a range of input voltage values.

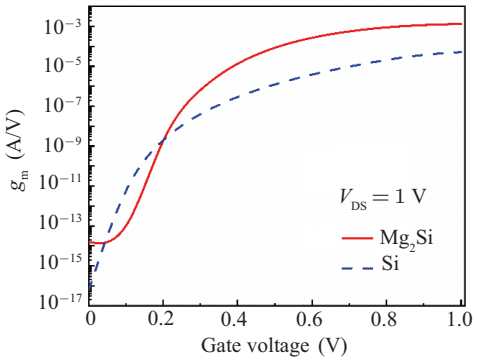


Fig. 8. Transconductance *versus* gate voltage of HPD-GAA-TFET and Si-based GAA-TFET at $V_{\rm DS} = 1$ V.

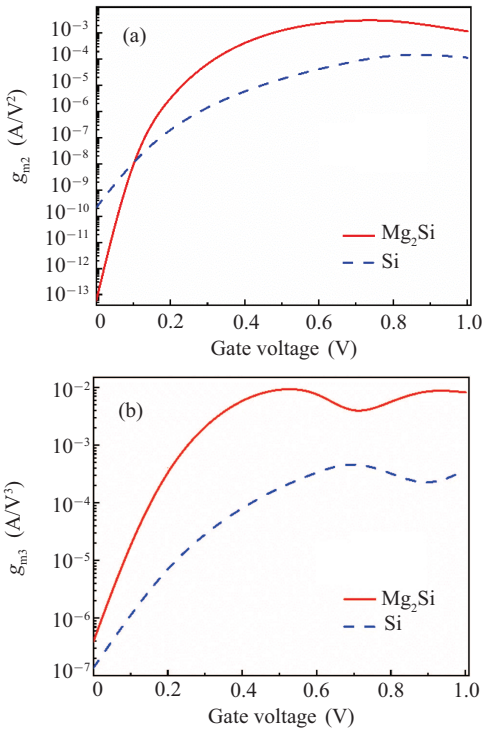


Fig. 9. A comparison between HPD-GAA-TFET and Si-based GAA-TFET in terms of (a) $g_{\rm m2}$ and (b) $g_{\rm m3}$.

However, the higher order of $g_{\rm m}$ that governs the non-linear behavior of the device, initially arising from '$g_{\rm m}$' itself varying in accordance with the input signal to the TFET, needs to be as small as possible to maintain the above discussed.

$$g_{\rm m2} = \frac{\partial^2 I_{\rm D}}{\partial^2 V_{\rm GS}}, \tag{5}$$

$$g_{\rm m3} = \frac{\partial^3 I_{\rm D}}{\partial^3 V_{\rm GS}}. \tag{6}$$

In the context of our device although $g_{\rm m2}$ and $g_{\rm m3}$, which are expressed as Eqs. (5) and (6) respectively, are somewhat significant, their effects on major RF characteristics are mitigated by the dominance of $g_{\rm m}$, which in our case is very large. The value of $g_{\rm m3}$, which controls the lower limit of distortion[25,26] and plays an important role in determining the nonlinearity, is kept at the lowest value in Figs. 9(a) and 9(b).

Now, we come to analyze the remaining factors which will complete our analysis of device linearity, and provide a useful insight into its RF characteristics. Figure 10(a) shows the relation between total gate capacitance $C_{\rm gg}$ and the applied $V_{\rm GS}$. It can be seen that beyond the point of 0.4 V of $V_{\rm GS}$, $C_{\rm gg}$ for HPD-GAA-TFET shows a steep increase compared with the scenario in the Si-based device, which does not show much of an increase at all. $C_{\rm gg}$ is the sum of $C_{\rm gs}$ and $C_{\rm gd}$, however, in contrast to the traditional MOS, where both are significant, $C_{\rm gd}$ dominates over $C_{\rm gs}$ in case of HPD-GAA-TFET. With reference to Fig. 10(b), for our device (and for TFETs in general), we see that the drain is connected to the inversion layer, unlike MOSFETs, where both drain and source are equally connected to the inversion layer.[19] This naturally leads to a larger contribution of $C_{\rm gd}$ in $C_{\rm gg}$. A higher $C_{\rm gg}$ leads to better and larger switching ratio, which in our case is large.

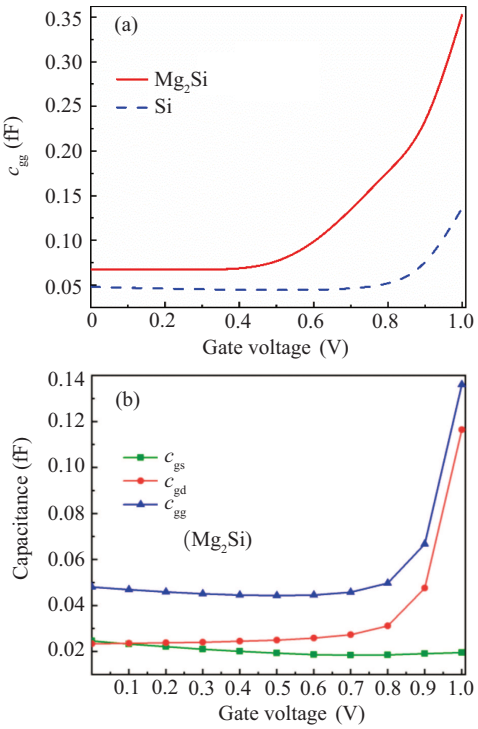


Fig. 10. (a) The $C_{\rm gg}$ of HPD-GAA-TFET and Si-based GAA-TFET, and (b) $C_{\rm gg}$, $C_{\rm gd}$, and $C_{\rm gs}$ of HPD-GAA-TFET.

Another important factor is f_T (unity gain frequency) which is defined as the frequency at which the short circuit gain of the device falls to unity and shown below:

$$f_T = \frac{g_m}{2\pi \times C_{gg}}. \tag{7}$$

Figure 11 shows the variation of cut-off frequency with respect to V_{GS} for HPD-GAA-TFET and Si-based GAA-TFET. The dominance of g_m over C_{gg} reflects high cut-off frequency. The trend is explained by the fact that increasing V_{GS} increases the carriers injected from source to drain via band-to-band tunnelling, effectively increasing f_T. The crossover at 0.2 V in cut-off frequency is due to the dependence of frequency on g_m which changes abruptly at a gate voltage of 0.2 V. Although cut-off frequency also depends on C_{gg} but its effect is nominal.

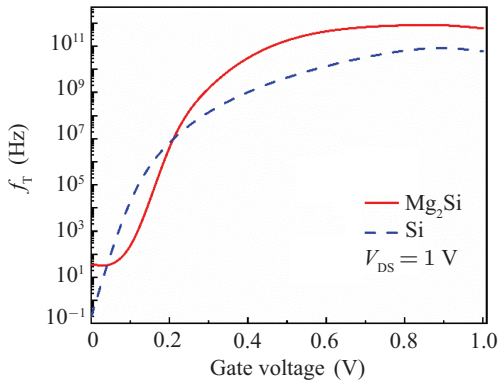


Fig. 11. A comparison of f_T *versus* gate voltage between HPD-GAA-TFET and Si-based GAA-TFET.

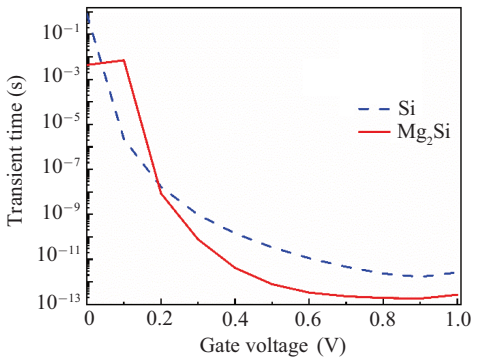


Fig. 12. A comparison of transit time *versus* gate voltage between HPD-GAA-TFET and Si-based GAA-TFET.

Figure 12 shows the gate–voltage-dependent transit time (τ) given by Eq. (8) which is the time taken by the charge carriers to move out of the channel region. For our device, particularly for the HPD-GAA-TFET, it is quite short, ranging from 10^{-11} s to 10^{-15} s, for a V_{GS} range from 0.4 V to 1 V. Lower transit time reflects the speed of device; therefore, it can be said from Fig. 12 that HPD-GAA-TFET is faster than Si-based GAA-TFET.

$$\tau = \frac{1}{2\pi \times f_T}. \tag{8}$$

Transconductance generation factor (TGF) represents the efficiency of the device converting drain current (DC parameter) into transconductance (AC parameter) formulated as Eq. (9).

Figure 13 shows the TGF variation with V_{GS} for both the proposed devices

$$\mathrm{TGF} = \frac{g_m}{I_D}. \tag{9}$$

From Fig. 13 we can conclude that at V_{GS} equaling 0.2 V the TGF for Mg_2Si is remarkably higher, which gives us an idea that how efficiently the current is used to achieve a certain value of transconductance. It also helps us in realizing the circuit operating at low supply voltage.

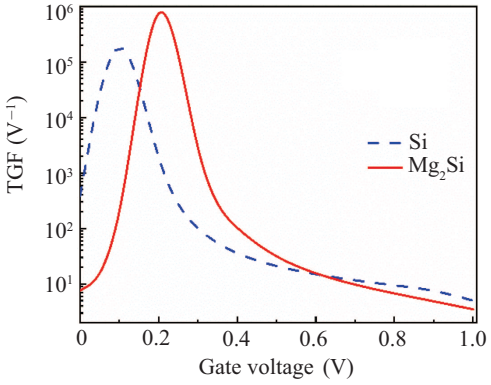


Fig. 13. A comparison of TGF *versus* gate voltage between Mg_2Si and Si.

Moreover, the relationship between the gain obtained by our device and the bandwidth it operates is analyzed, with gain bandwidth product given by

$$\mathrm{GBP} = \frac{g_m}{20\pi \times C_{gd}}. \tag{10}$$

Figure 14 shows the variation of DBT with V_{GS} for both the proposed devices and clearly indicates that Mg_2Si-based device performs better than Si-based over an applied V_{GS} range of (0.2 V–1 V).

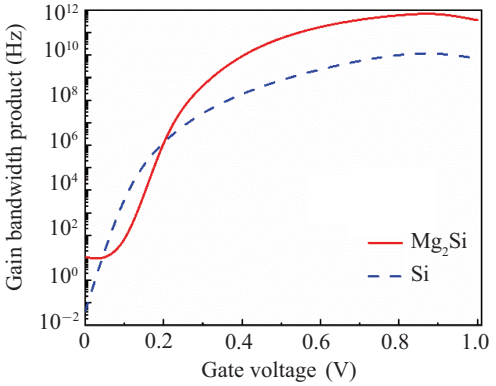


Fig. 14. A comparison of GBP *versus* gate voltage between Mg_2Si and Si.

Progressing towards the non-linear behavior of our device we delve into the second-order voltage intercept point 2 (VIP2) and the third-order voltage intercept point 3 (VIP3), which are caused by the second-order and the third-order non-linearities. VIP2 is the input voltage at which the first-order

harmonic voltage is equal to the second-order harmonic one, and given by

$$\mathrm{VIP2} = 4 \times \frac{g_{\mathrm{m}}}{g_{\mathrm{m2}}}. \tag{11}$$

Figure 15 shows VIP2 and VIP3 for HPD-GAA-TFET and Si-based GAA-TFET. We can see from Fig. 15(a) that for a higher value of input signal, we achieve a higher value of VIP2 by a significant margin, and the higher the value of VIP2, the lesser the distortion and better the linearity is. When further looking at Fig. 15(b) we observed that the amplitude of VIP3 is also greater in the case of Mg_2Si-based device. The VIP3 basically gives the value of input voltage at which the first harmonic voltage is equal to the third-order harmonic voltage given below:

$$\mathrm{VIP3} = \sqrt{24 \times \frac{g_{\mathrm{m}}}{g_{\mathrm{m3}}}}. \tag{12}$$

As can be observed from the mathematical expression of VIP2 and VIP3 although we have a larger value of g_{m2} and g_{m3} (a dominant source of non-linearity) the results of VIP2 and VIP3 are better for Mg_2Si-based device as the dominating factor remains g_{m}, which provides better ability to drive drain current. The higher VIP3 implies that there is a moderate inversion characteristic.[25] At higher gate bias there is an early departure of non-linearity in VIP3 owing to the early zero crossover of g_{m3} in Mg_2Si.

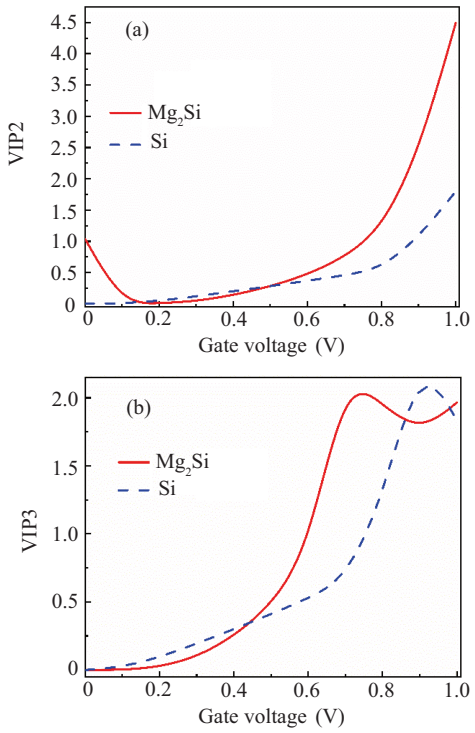


Fig. 15. A comparison of (a) VIP2 and (b) VIP3 *versus* gate voltage between HPD-GAA-TFET and Si-based GAA-TFET.

Further, we calculated the third-order input intercept point (IIP3). It shows the input power for which the first-order harmonic and the third-order harmonic are equal. The IIP3 can be formulated below:

$$\mathrm{IIP3} = \frac{2}{3} \times \frac{g_{\mathrm{m}}}{g_{\mathrm{m3}} \times R_{\mathrm{s}}},$$
$$\mathrm{dBm(IIP3)} = 10\log_{10}(\mathrm{IIP3}) + 30, \tag{13}$$

where $R_{\mathrm{s}} = 50\ \Omega$.

It can be observed from the Fig. 16 that the amplitude of IIP3 is somewhat good for Mg_2Si-based device, which is what is desired for better linearity in RFICs. A higher value of IIP3 also provides an enhanced control and a higher carrier transport rate over the channel.

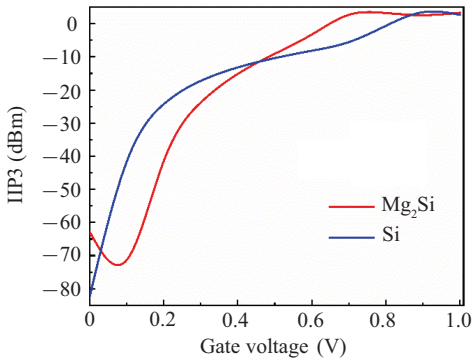


Fig. 16. A comparison of IIP3 *versus* gate voltage between HPD-GAA-TFET and Si-based GAA-TFET.

A harmonic is a signal whose frequency is an integral multiple of the frequency of the same reference signal. And these harmonics cause unwanted distortions which degrade the transfer characteristics of each device. So, to have better linearity and higher gain we need to suppress them as much as possible. The second-order harmonic distortion (HD2) can be expressed as

$$\mathrm{HD2} = \frac{1}{2} \times V_{\mathrm{i}} \times \frac{g_{\mathrm{m2}}}{2g_{\mathrm{m}}}\ \mathrm{dBm}, \tag{14}$$

where $V_{\mathrm{i}} = 50$ V.

Figure 17 shows a comparison of HD2 *versus* gate voltage between Mg_2Si-based and Si-based devices; it is clearly indicated that for the higher value of input signal, we have lesser harmonic distortion.

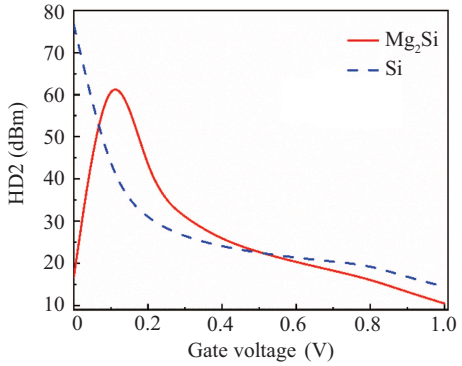


Fig. 17. A comparison of HD2 *versus* gate voltage between HPD-GAA-TFET and Si-based GAA-TFET.

4. Conclusions

In this work, the charge plasma method has been employed to induce uniform doping in an intrinsic Si-wafer. Suitable electrodes are chosen to induce p-type and n-type dopings in the source and drain regions, respectively. Magnesium silicide, a low band gap material is used as a source material to enhance the tunnelling rate of electrons thereby driving the current. A comparison is carried out between Mg_2Si and Si-based doping-less device in terms of electrical, RF, linearity, and distortion performance parameters. It is observed that the Mg_2Si-based device outperforms the Si-based device. High values of VIP2 and VIP3 for HPD-GAA-TFET present high linearity. Moreover, HPD-GAA-TFET operates at faster rate than Si-based device. The electrical performance parameters of HPD-GAA-TFET I_{ON}, SS, V_{th}, and I_{ON}/I_{OFF} are 0.377 mA, 12.660 mV/dec, 0.214 V, and 2.985×10^{12}, respectively. The subthreshold swing and V_t for Mg_2Si-based device decrease by 33% and 43%, respectively with respect to those of Si-based device, while the I_{ON}/I_{OFF} and I_{ON} significantly improve 134 times and 29 times, respectively. Therefore, the overall analysis shows that HPD-GAA-TFET is a suitable contender for low power applications.

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