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Charge trapping effect at the interface of ferroelectric/interlayer in the ferroelectric field effect transistor gate stack

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We study the charge trapping phenomenon that restricts the endurance of n-type ferroelectric field-effect transistors (FeFETs) with metal/ferroelectric/interlayer/Si (MFIS) gate stack structure. In order to explore the physical mechanism of the endurance failure caused by the charge trapping effect, we first establish a model to simulate the electron trapping behavior in n-type Si FeFET. The model is based on the quantum mechanical electron tunneling theory. And then, we use the pulsed I_d–V_g method to measure the threshold voltage shift between the rising edges and falling edges of the FeFET. Our model fits the experimental data well. By fitting the model with the experimental data, we get the following conclusions. (i) During the positive operation pulse, electrons in the Si substrate are mainly trapped at the interface between the ferroelectric (FE) layer and interlayer (IL) of the FeFET gate stack by inelastic trap-assisted tunneling. (ii) Based on our model, we can get the number of electrons trapped into the gate stack during the positive operation pulse. (iii) The model can be used to evaluate trap parameters, which will help us to further understand the fatigue mechanism of FeFET.

Keywords: ferroelectric, interface, ferroelectric field-effect transistors (FeFETs), charge trapping

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1. Introduction

Hafnium-based ferroelectric (FE) materials have attracted extensive attention since their discovery.[1–6] Compared with the traditional perovskite FE materials, hafnium-based FE materials have excellent compatibility with the existing complementary metal–oxide–semiconductor field-effect transistor (CMOSFET) fabrication process.[7,8] In addition, the hafnium-based FE material can remain the ferroelectricity at a relatively thin film,[9–11] which is conducive to making devices further scale down. Therefore, the discovery of hafnium-based FE materials makes ferroelectric field effect transistors (FeFETs) become one of the emerging memory technology with great potential.[12–14] At present, the main gate structure used in FeFET is a metal/ferroelectric/interlayer/Si (MFIS) structure. The bottleneck of FeFET with MFIS structure is poor endurance.[15] The factors which limit the endurance of a FeFET are concluded to be the charge trapping phenomenon caused by the spontaneous polarization.[16–19] To improve the endurance of the FeFET, it is important to understand the mechanism of charge trapping. However, the current method of characterizing the phenomenon of charge trapping through experimental measurement still cannot clarify the driving force.[17–20] At present, some studies have modeled the electrical characteristics of the FeFET, hoping to find the factors that affect the charge trapping by fitting them with the experimental data. However, most of these models use compact-model, and these models mainly use empirical formulas.[21–23] Therefore, the physical origin of charge trapping has not been fully understood yet.

This work establishes a model to simulate the charge trapping process when applying an operating gate voltage pulse. Our model is based on the electron tunneling theory, which considers that the electrons in the Si substrate of the FeFET are trapped at the FE/IL interface through the interlayer (IL) barrier by different tunneling mechanisms. The number of electrons trapped at the FE/IL interface (ΔQ_t) can be obtained by integrating the total tunneling current (J_{total}). And then threshold voltage shift between the rising and falling edges (ΔV_{th}) can be obtained by using the background capacitance of the FE layer (C_{FE}), which is measured in the experiment.

In order to reveal the driving force behind the charge trapping phenomenon, we use the pulsed I_d–V_g method to measure ΔV_{th}. By fitting the simulated ΔV_{th} with the experimentally measured ΔV_{th}, we find that the main tunneling mechanism that causes the charge trapping phenomenon is the trap-assisted tunneling (TAT) mechanism. Therefore, the purpose of improving the fatigue characteristics of FeFET can be achieved by replacing the IL material or improving the fabricating process of the IL to create the IL with fewer traps to suppress charge trapping.

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2. Model of electron trapping

We study the n-type FeFET with an MFIS structure which is widely used. The device structure used in our experiment and simulation is shown in Fig. 1(a), and the IL is SiO_2. It has been reported that hole-trapping is less significant in n-type FeFETs.[20] Therefore, our model only considers electron trapping. The energy band diagram is shown in Fig. 1(b). When a positive voltage is applied to the device, a large number of electrons in the inversion layer of the Si substrate will be trapped in the gate stacks of the FeFET. Due to the high electric field across IL, the electron trapping/de-trapping behavior mainly occurs at the FE/IL interface in a FeFET.[17,18,20] In our model, the electron trapping effect is considered as the electron transfer between the Si substrate and FE/IL interface based on the tunneling process. The barrier that the substrate electrons need to tunnel through is determined by the voltage across the IL. Therefore, the number of trapped electrons equals the integral of the tunneling current over time. This work establishes a tunneling current model based on the tunneling mechanism instead of the traditional semi-empirical leakage model. The model uses three basic tunneling mechanisms: direct tunneling (DT), Fowler–Nordheim tunneling (FNT), and trap-assisted tunneling (TAT) to simulate the behavior of electron trapping into the gate stacks. The tunneling current mechanism and the variation of the IL barrier caused by the trapped electrons are shown in Figs. 1(c) and 1(d).

2.1. DT and FNT

The essential difference between the DT and FNT is that the barrier shape of the electron face is different, so they can use a unified expression. We use the Landauer model to calculate the tunneling current caused by the DT and FNT mechanisms.[24,25] The expression is

$$J_{\mathrm{DF}} = \frac{q m_0 k_{\mathrm{B}} T}{2\pi^2 \hbar^3} \int_{E_{\mathrm{T(FE/IL)}}}^{\infty} f(E)\, T(E)\, \mathrm{d}E, \tag{1}$$

where q, m_0, k_{B}, T, $\hbar$, E, and $E_{\mathrm{T(FE/IL)}}$ are the electron charge, the rest mass of a free electron, the Boltzmann constant, the temperature, the reduced Plank constant, the electron's energy, and the trap energy level position at the FE/IL interface relative to the FE conduction band, respectively.

The supply function $f(E)$ in Eq. (1) is expressed by the Fermi–Dirac distribution function on both sides of the barrier

$$f(E) = \frac{1 + \mathrm{e}^{\left(E - E_{\mathrm{F(Si)}}\right)/k_{\mathrm{B}}T}}{1 + \mathrm{e}^{\left(E - E_{\mathrm{F(FE/IL)}}\right)/k_{\mathrm{B}}T}}, \tag{2}$$

where $E_{\mathrm{F(Si)}}$ is the Fermi energy level of the Si substrate and $E_{\mathrm{F(FE/IL)}}$ is the Fermi level at the FE/IL interface.

The tunneling probability $T(E)$ in Eq. (1) of electrons is obtained by the Wentzel–Kramers–Brillouin (WKB) approximation[26]

$$T(E) = \exp\left[-\frac{2}{\hbar}\left|\int_0^{t_{\mathrm{IL}}} \sqrt{2m^*_{\mathrm{IL}}\left(E - U(x)\right)}\,\mathrm{d}x\right|\right], \tag{3}$$

where t_{IL} is the thickness of the IL, m^*_{IL} is the effective mass of electrons in the IL, and $U(x)$ is the potential barrier function of the IL.

2.2. TAT

In this work, we consider the inelastic TAT. That is, the TAT current is generated by multi-phonon assistance.[27,28] The expression of the TAT current is

$$J_{\mathrm{TAT}} = q \int_0^{t_{\mathrm{IL}}} \frac{N_{\mathrm{t}}}{\tau_{\mathrm{e}}(x) + \tau_{\mathrm{c}}(x)}\,\mathrm{d}x, \tag{4}$$

where N_{t} is the trap concentration of the IL. $\tau_{\mathrm{e}}(x)$ and $\tau_{\mathrm{c}}(x)$ are the emission time constants and the capture time constants of electrons, respectively, and they are calculated by the following expressions:

$$\tau_{\mathrm{e}}^{-1}(x) = \int_{\Phi_{\mathrm{t(IL)}}(x)}^{\infty} N_{\mathrm{l}}(E)\left[1 - f_{\mathrm{l}}(E)\right] T_{\mathrm{l}}(E,x) e_{\mathrm{n}}(E,x)\,\mathrm{d}E, \tag{5a}$$

$$\tau_{\mathrm{c}}^{-1}(x) = \int_{\Phi_{\mathrm{t(IL)}}(x)}^{\infty} N_{\mathrm{r}}(E) f_{\mathrm{r}}(E) T_{\mathrm{r}}(E,x) c_{\mathrm{n}}(E,x)\,\mathrm{d}E, \tag{5b}$$

where $\Phi_{\mathrm{t(IL)}}(x)$ is the position of the trap energy level in IL relative to the IL conduction band. The $f_{\mathrm{l}}(E)$ and $f_{\mathrm{r}}(E)$ are the Fermi–Dirac distribution function on the left and right sides of the IL barrier. $T_{\mathrm{l}}(E,x)$ is the electron tunneling probability from the left side of IL into traps in the IL, and $T_{\mathrm{r}}(E,x)$ is the electrons tunneling probability from traps in the IL to the FE/IL interface. Here we also use the WKB approximate to calculate the tunneling probability. The $e_{\mathrm{n}}(E,x)$ and $c_{\mathrm{n}}(E,x)$ are the emission rate and capture rate, which can be obtained in detail from Ref. [28].

At present, in most of the existing literature, both elastic and inelastic TAT models only consider a single energy level for the TAT mechanism.[28–35] Multiple energy levels are mathematically equivalent to a single energy position for the electrical measurement and simulation results. For a single energy level condition, it can be considered that the density of states of this level in the IL of the actual device is larger, and most of the electrons trapped at this level contribute most of the TAT current. Due to the lower density of states of other trap levels, the number of trapped electrons is relatively small. Therefore, our model also considers the trap energy level of IL as a single energy level. It is represented by a red dashed line in Fig. 1(c).

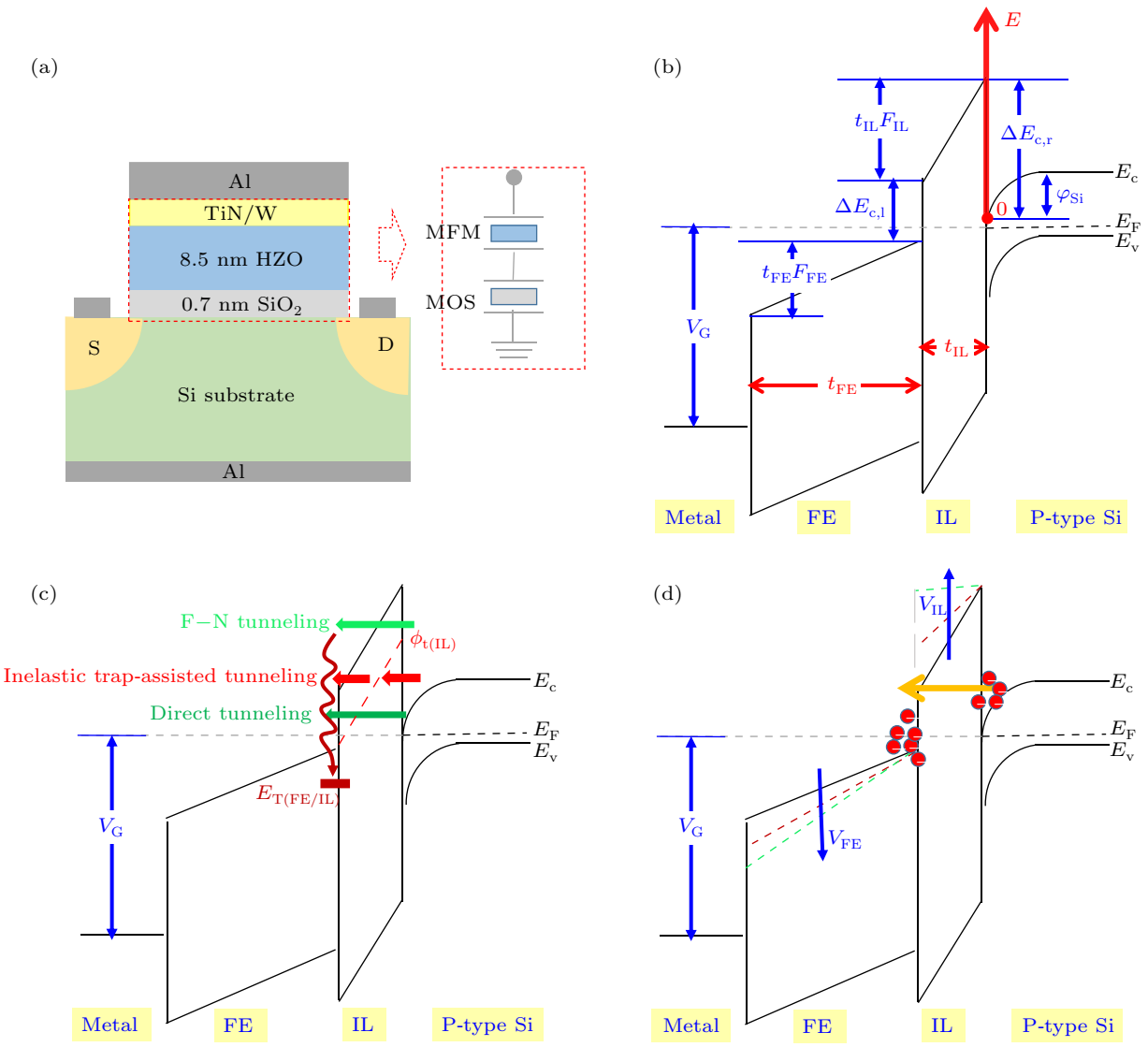


Fig. 1. (a) The structure of n-FeFET in our experiment. (b) The energy band diagram corresponding to the device structure in (a) under positive voltage and the definition of parameters. (c) Schematic diagram of three tunneling current mechanisms in the device and the definition of parameters. (d) The variation of IL barrier is caused by the trapped electrons at the FE/IL interface under positive voltage.

2.3. Relationship between charge and voltage distribution in the gate stack

According to Fig. 1(a), we can see that the gate of the Fe-FET with MFIS structure is equivalent to the series connection of a FE capacitor and a MOS capacitor. Thus, the voltage distribution relationship of the gate stack at a given gate voltage is

$$V_{\mathrm{FE}}(Q_{\mathrm{m}}) = V_{\mathrm{G}} - V_{\mathrm{IL}}(Q_{\mathrm{m}}) - \varphi_{\mathrm{s}}(Q_{\mathrm{m}}) - \varphi_{\mathrm{ms}}, \tag{6}$$

where V_{FE}, Q_{m}, V_{G}, V_{IL}, φ_{s}, and φ_{ms} are the voltage on the FE layer, the number of charges on the metal, the applied voltage on the gate, the voltage across the IL, the surface potential of the Si substrate and the work function difference between the metal gate and the Si substrate, respectively. Equation (6) is also called the loadline of FeFET.[36]

The charges in the gate obey the continuity of electrostatic displacement

$$Q_{\mathrm{m}} = \varepsilon_{\mathrm{FE}}\varepsilon_0 V_{\mathrm{FE}}/t_{\mathrm{FE}} + P = \varepsilon_{\mathrm{IL}}\varepsilon_0 V_{\mathrm{IL}}/t_{\mathrm{IL}} = -(Q_{\mathrm{Si}} + Q_{\mathrm{t}}), \tag{7}$$

where $\varepsilon_{\mathrm{FE}}$, ε_0, t_{FE}, P, $\varepsilon_{\mathrm{IL}}$, Q_{Si}, and Q_{t} are the dielectric constant of the FE layer, the vacuum dielectric constant, the thickness of the FE layer, the charges contributed by spontaneous polarization (P_{s}), the dielectric constant of the SiO_2 layer, the number of electrons on the Si substrate, and the number of electrons trapped at the FE/IL interface, respectively.

For the FE layer, we use the Miller model[37] to calculate P. Miller gives the expression of P as follows:

$$\frac{\partial P}{\partial E_{\mathrm{FE}}} = \left[1 - \tanh\left[\left(\frac{P - P_{\mathrm{sat}}}{\xi P_{\mathrm{s}} - P}\right)^{1/2}\right]\right] \times \frac{P_{\mathrm{s}}}{2\delta}\left[1 - \tanh^2\left(\frac{E_{\mathrm{FE}} - E_{\mathrm{c}}}{2\delta}\right)\right], \tag{8}$$

where E_{FE} is the electric field of the FE layer; P_{s} is the spontaneous polarization of the FE layer; E_{c} is the coercive electric

field of the FE layer; ξ represents the scanning direction of the electric field, when $\xi = +1$ indicates an increase in an electric field, and when $\xi = -1$ indicates a decrease in an electric field. $P_{\rm sat}$ is the saturated polarization of the FE layer, its expression is

$$P^{+}_{\rm sat}(E_{\rm FE}) = P_{\rm s}\tanh\left(\frac{E_{\rm FE}-E_{\rm c}}{2\delta}\right), \tag{9a}$$

$$P^{-}_{\rm sat}(E_{\rm FE}) = -P^{+}_{\rm sat}(-E_{\rm FE}), \tag{9b}$$

where $P^{+}_{\rm sat}$ represents the $P_{\rm sat}$ of positive polarization, and $P^{-}_{\rm sat}$ represents the $P_{\rm sat}$ of negative polarization.

The expression of δ in Eq. (8) is

$$\delta = E_{\rm c}\left[\ln\frac{1+P_{\rm r}/P_{\rm s}}{1-P_{\rm r}/P_{\rm s}}\right]^{-1}, \tag{10}$$

where $P_{\rm r}$ is the remanent polarization of the FE layer.

Considering the quantum mechanical confinement effect of Si substrate, the relationship between $Q_{\rm Si}$ and $\varphi_{\rm s}$ can be obtained by a self-consistent solution of Schrodinger and Poisson equations.[38]

2.4. Calculation of the amount of trapped charge

If the rising edge of the operation voltage is fast enough, it is considered that there is no additional electron injection. At the beginning of the operation pulse, we use the number of trapped charges ($Q_{\rm t0}$) at the FE/IL interface as $0.8P_{\rm s}$ which was reported in previous experimental results.[20] Then during the process of applying a positive voltage, the $Q_{\rm t}$ at the FE/IL interface is

$$Q_{\rm t} = Q_{\rm t0} + \Delta Q_{\rm t}, \tag{11}$$

$$Q_{\rm t0} = 0.8P_{\rm s}, \tag{12}$$

$$\Delta Q_{\rm t}(t) = \int_{0}^{t_{\rm pw}} J_{\rm total}(t)\,{\rm d}t, \tag{13}$$

$$J_{\rm total}(t) = J_{\rm DT}(t) + J_{\rm FN}(t) + J_{\rm TAT}(t). \tag{14}$$

2.5. Model assumptions

To simplify the problem and intuitively study the electron trapping behavior in FeFET, due to the negligible tunneling current from the FE/IL interface to the metal gate with the thick FE layer (8.5 nm) and lower FE electric field ($<$ 5.5 MV/cm) compared with thin IL thickness (0.7 nm) and high electric field ($>$ 10 MV/cm) on IL.

3. Simulation process

The detailed simulation flow is given in Fig. 2. We divide the pulse width ($t_{\rm pw}$) into several time intervals, and the trapped electrons calculated by tunneling current in each time interval ($\Delta Q_{\rm t}(i)$) simultaneously change the voltage division of the gate layers. By combining Eqs. (1)–(14) with the Miller model of the FE layer and the MOS loadline of the device, the voltage of each gate layer, $\Delta Q_{\rm t}(i)$, and the variation of polarization ($\Delta P(i)$) can be calculated for each time interval. The total number of electrons trapped during the $t_{\rm pw}$ is obtained and denoted as $\Delta Q_{\rm t}$, and the total variation of polarization is denoted as ΔP. The threshold voltage shift ($\Delta V_{\rm th}$) during the $t_{\rm pw}$ can be obtained by the background capacitance of FE ($C_{\rm FE}$)

$$\Delta V_{\rm th} = \left(\Delta Q_{\rm t} + \Delta P\right)/C_{\rm FE}, \tag{15}$$

where $C_{\rm FE}$ was obtained by experimentally measuring $\varepsilon_{\rm FE}$ of the FE layer.

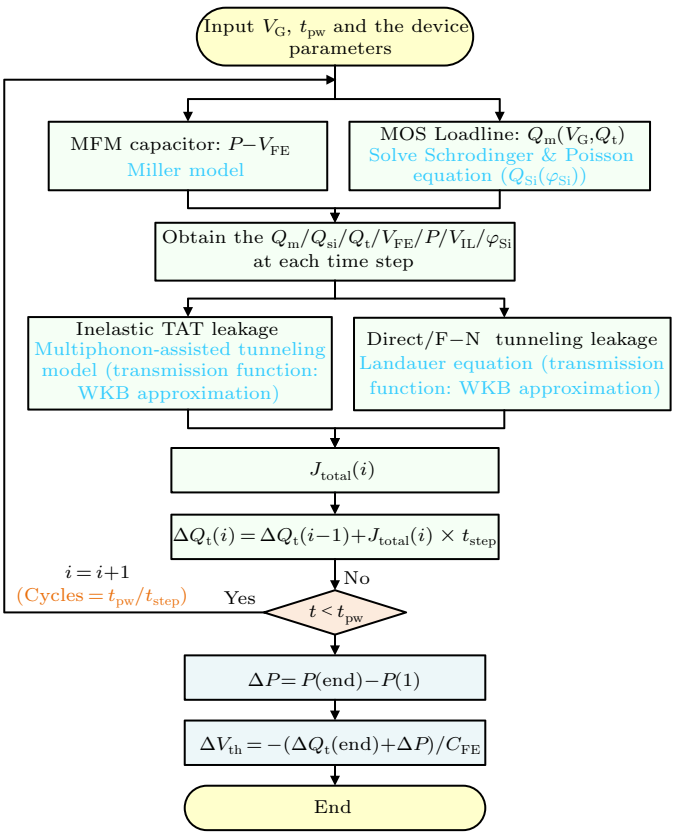


Fig. 2. The simulation flow in this work.

4. FeFET fabrication and trapped electrons measurements

The devices used for measurement were prepared by the gate-last process.[39] The ratio of gate length to gate width (L/W) of our devices was 5 μm/150 μm. The process flow could be divided into 5 parts based on lithography: source and drain injection, channel area opening, gate etching, source and drain opening, and metal etching. Firstly, the substrate silicon wafer was cleaned with diluted hydrofluoric acid (HF) to remove natural oxides, and then PE-oxides with 300 nm were deposited. As ions with energy of 40 keV and a dose of 4×10^{15} cm^{-2} were implanted into Si substrate to form

source and drain regions and then annealed at 1050 °C in N_2 atmosphere for 5 s. Secondly, the gate area was defined by photolithography, and after being cleaned by diluted HF, a 0.7 nm SiO_2 interlayer was grown by wet ozone oxidation. Next, about 8.5 nm $Hf_{0.5}Zr_{0.5}O_2$ was grown by atomic layer deposition (ALD) at 300 °C. The $Hf_{0.5}Zr_{0.5}O_2$ was annealed at 550 °C in N_2 for 60 s to form the ferroelectric orthorhombic phase. After the formation of the gate, the source/drain contact locations were determined by photolithography, the source and drain regions were exposed, and 10 nm TiN and 75 nm W were deposited by physical vapor deposition (PVD). Finally, the top and bottom Al electrodes were deposited. The structure of the FeFET devices prepared by the above process flow is shown in Fig. 1(a).

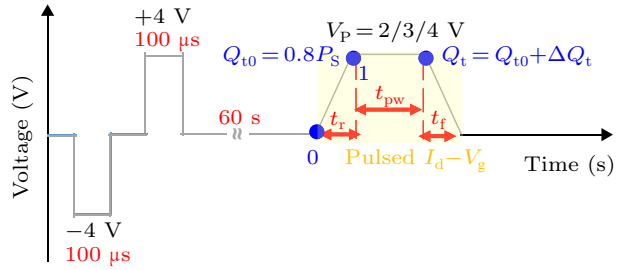


Fig. 3. The test waveform used in our experiment.

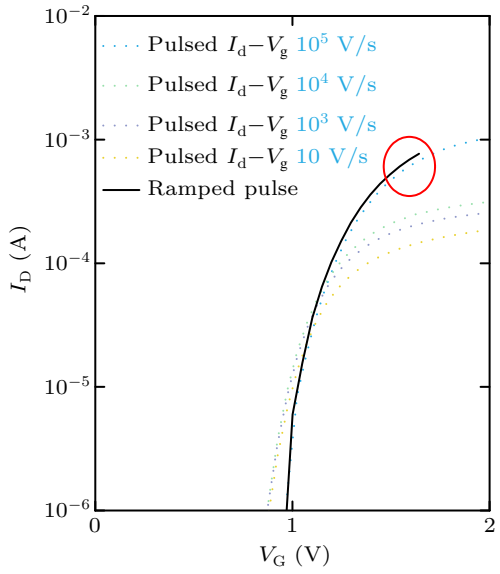


Fig. 4. Comparison of I_D–V_G curves measured by pulsed I_d–V_g and ramped pulse method.

In order to measure the trapped electrons of FeFET under the operating voltage, we refer to the pulsed I_d–V_g test method used in high-k devices.[40] The test waveform used in our experiment is shown in Fig. 3. For the device in Fig. 1(a), we first apply a pair of gate voltage pulses with an amplitude of ±4 V and a pulse width of 100 μs to pre-polarize the device, and then wait for 60 s before applying the second trapezoidal wave. According to the pulsed I_d–V_g test method, when the rising edge time t_r is short enough, ΔQ_t at the rising edge can be ignored. That is, Q_t at point 0 in Fig. 3 is equal to the Q_t at point 1. In Ref. [40], whether there are electrons trapped within t_r can be verified by ramped pulse measurement method. Figure 4 shows the comparison between pulsed I_d–V_g and ramped pulse method with different rising rates when $V_G = 2$ V. It can be seen that there are nearly no electrons trapped when the rising rate is 10^5 V/s, so the rising edge rate used in our experiment is 10^5 V/s. In the experiment, we use different t_{pw} and pulse amplitude (V_p) to measure the threshold voltage at the rising and falling edge, and their difference is denoted as ΔV_{th}.

In this way, we can connect the parameter ΔV_{th} which can be directly measured in the experiment, with the parameter ΔQ_t which cannot be measured directly. The ΔQ_t obtained by simulation can use Eq. (15) converted into ΔV_{th}. Next, we will fit the simulated ΔV_{th} with the experimentally measured ΔV_{th} to reveal the driving force behind the charge trapping phenomenon.

5. Application of our model in published data

In order to verify that our model is accurate and available, we first use the model to simulate the experimental data in Ref. [41]. The simulation results are shown in Fig. 5. We can see that our model fits with the experimental data well in Ref. [41]. The simulation parameters are shown in Table 1. The $E_{T(FE/IL)}$, $\Phi_{t(IL)}$, and N_t determined by our model are consistent with the Ref. [41]. This proves that our model can also evaluate the trap parameters in the FeFET according to the measurement results of ΔV_{th}.

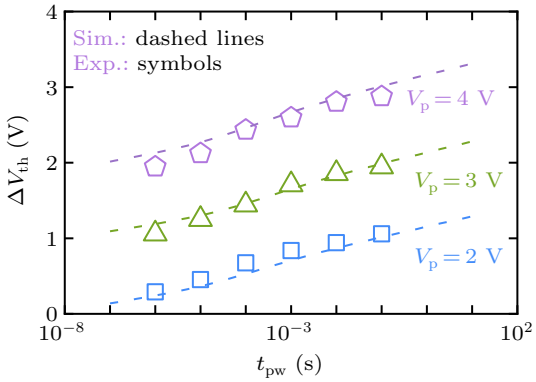


Fig. 5. Our simulation model fits the experimental data in Ref. [41].

6. Application of our model in our experimental data

Figure 6(a) shows the experimental data measured by the pulsed I_d–V_g method and the results of fitting the experimental data. We can see that our model fits well with our experimental data. The simulation parameters used in the simulation are shown in Table 1. It should be noted that although the devices fabricated in our work has a similar structure to the devices prepared in Ref. [41] because the fabrication process of the

SiO_2 layer and the temperature conditions for its growth have a significant impact on the quality of the SiO_2 layer, the traps in the SiO_2 layer may be different.

Table 1. Fitting parameters used in our simulation.

	Unit	Experiment from Ref. [41]	Our experiment
MFIS stack		TiN/9 nm HZO/ 1.2 nm SiO_2	TiN/8.5 nm HZO/ 0.7 nm SiO_2
ε_{FE}		30	30
ε_{IL}		3.9	3.9
P_s	μC/cm^2	20	20
P_r	μC/cm^2	18	18
E_c	MV/cm	1.1	1.1
Φ_{ms}	V	−0.2	−0.2
$E_{T(FE/IL)}$	eV	2.3	2.5
$\Phi_{t(IL)}$	eV	2.65	1.8
N_t	cm^{-3}	10^{19}	10^{19}
Q_{t0}	μC/cm^2	16	16
$\Delta E_{c,r}$	eV	3.1	3.1

Figure 6(b) shows the composition of the tunneling current obtained by the simulation program when $V_G = 4$ V, the line in light brown represents J_{DT}, the line in light blue represents J_{TAT}, and the bold line in light green represents J_{total}.

It can be seen that the electrons trapped at the FE/IL interface are mainly caused by the TAT mechanism. Therefore, the most effective way to suppress the electron trapping effect of FeFET is to suppress the TAT current. The TAT current is mainly related to the trap density and trap energy level position in the IL, so we can achieve this purpose by changing the fabrication process condition of the IL or changing the material of the IL.

Figure 6(c) shows the variation of the voltage of each layer within the pulse width when $V_G = 4$ V. It can be seen that during the operating pulse, the V_{IL} decreases rapidly until unchanged, while V_{FE} increases, which is consistent with the analysis of the energy band diagram in Fig. 1(d).

Figure 6(d) shows the variation of trapped charges within pulse width and the variation of polarization within pulse width when $V_G = 4$ V. It can be seen that within the pulse width range of our experimental (10^{-7} s–1 s), P of the FE layer is almost unchanged, meaning that P of the FE layer has completely switched, while the number of electrons trapped in the gate slowly increases. It can be seen that a large number of electrons have been trapped in the FeFET gate before 10^{-7} s, and the V_{th} has completed a significant drift (about 3 V) before 10^{-7} s. That is to say, the time of the electrons to begin trapped is less than the order of μs.

This is also the reason why Fig. 6(b) does not include J_{FN} because the conduction band offset between SiO_2 and Si is very large (about 3.1 eV), so only a few electrons will tunnel through the triangular barrier, i.e., the F–N tunneling mechanism. Besides, under the pulse width of 10^{-7} s, a large number of charges have been trapped at the FE/IL interface already, so the voltage on the IL is very small. Therefore the tunneling current caused by the F–N mechanism has decayed to be smaller within the measurement range.

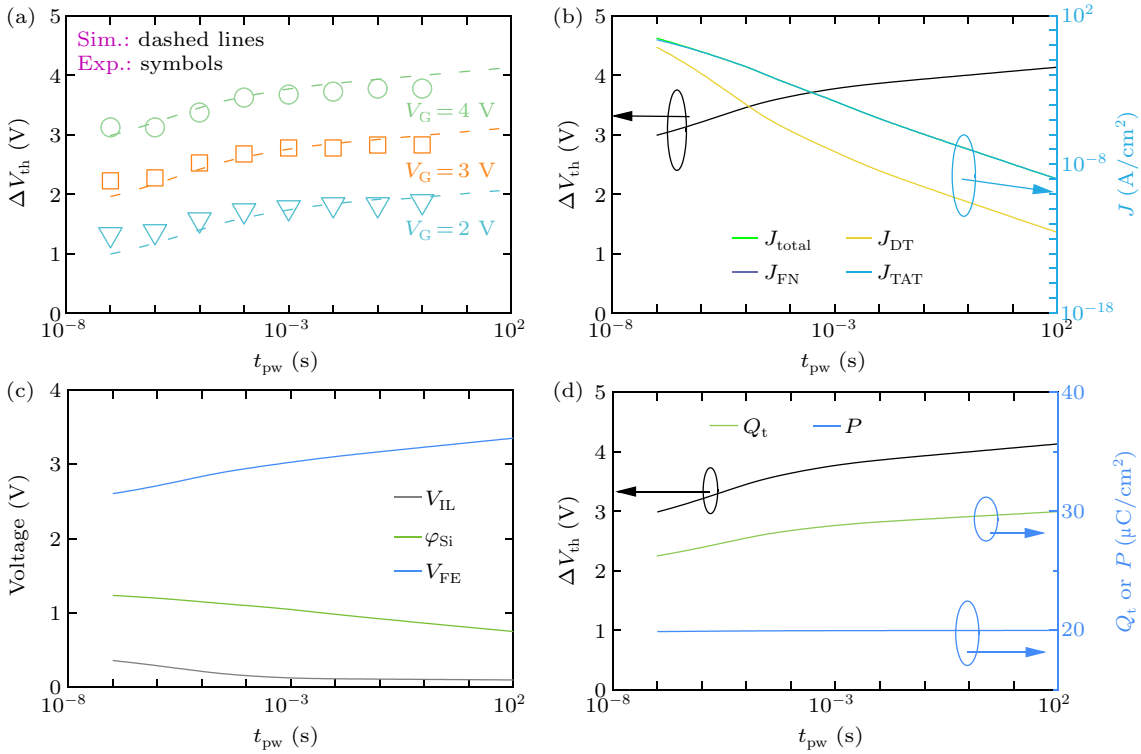


Fig. 6. (a) The fitting results of our model and experimental measurement data. (b) The component of tunneling current during platform wave time when $V_G = 4$ V. (c) The variation of the voltage of each layer within the pulsewidth when $V_G = 4$ V. (d) The variation of trapped charges within pulsewidth and the variation of polarization within pulsewidth when $V_G = 4$ V.

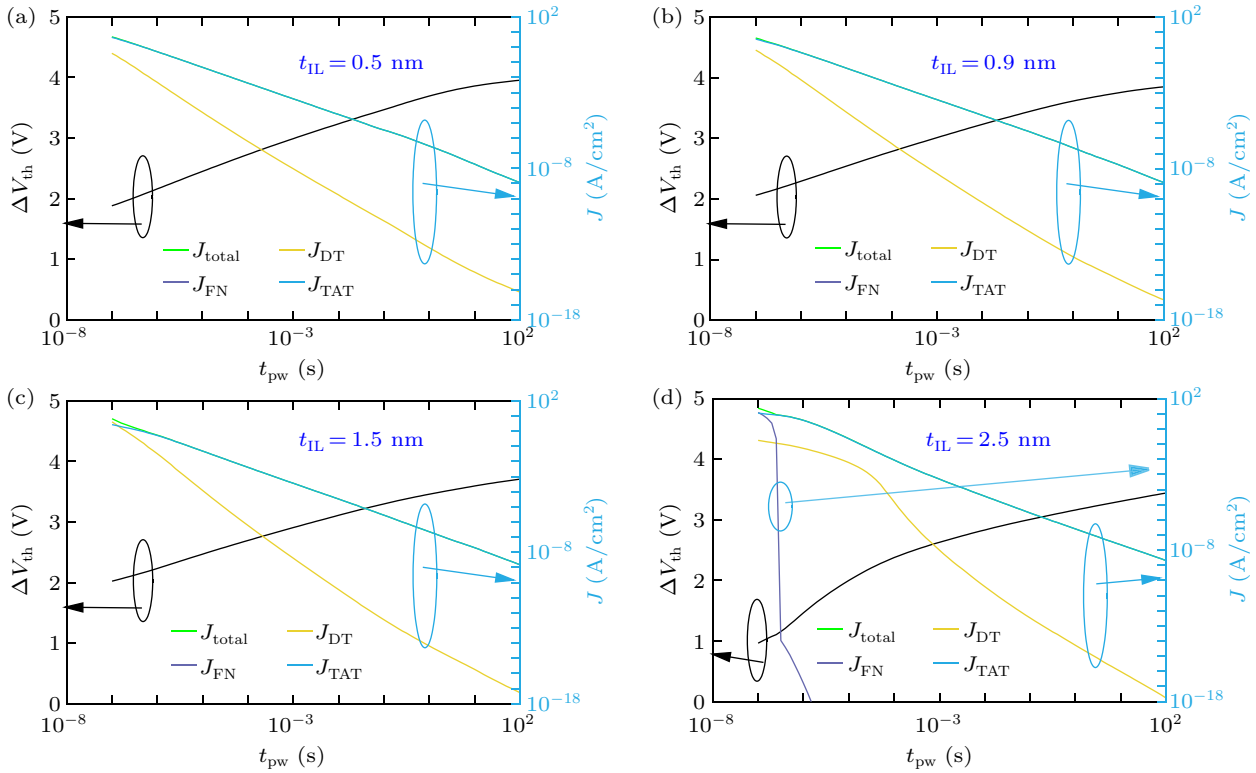


Fig. 7. The leakage mechanism variation of (a) $t_{IL} = 0.5$ nm, (b) $t_{IL} = 0.9$ nm, (c) $t_{IL} = 1.5$ nm, (d) $t_{IL} = 2.5$ nm when $V_G = 4$ V.

Figure 7 shows as the t_{IL} increases, the mechanism of tunneling current changes. When the $t_{IL} = 2.5$ nm, the electric field on the IL is lower than that of the thinner t_{IL}, so the speed of electrons trapped at the FE/IL interface is slower. Because the electric field on IL slowly decreases, the J_{FN} does not disappear instantly but lasts for a short time contributing to the J_{total}, while the J_{FN} decays quickly. From this perspective, the TAT tunneling mechanism remains the main driving force behind the charge trapping phenomenon.

7. Conclusion and perspectives

We have studied the phenomenon that electrons in the silicon substrate are trapped at the FE/IL interface in the FeFET gate stack. We propose a gate charge trapping model of the FeFET with the MFIS gate structure. Our model considers the trapped electrons at the FE/IL interface as the quantum mechanical tunneling through the IL barrier, and the number of trapped electrons is obtained by calculating the tunneling current. The results of the model simulation are matching with the threshold voltage shift measured in the experiment. Based on our model, we find that electrons tunnel through the interlayer by the TAT mechanism. This work gives a solution to improve the endurance of FeFET from another perspective.

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References

[1] Li Y, Liu X P, Sun T Y, Zhang F B, Fu T, Wang-yang P H, Li H O and Chen Y H 2022 *Chin. Phys. B* **31** 097307
[2] Li Y L, Zhu H, Li R, Liu J, Xiang J J, Xie N, Huang Z, Fang Z X, Liu X and Zhou L X 2022 *Chin. Phys. B* **31** 088502
[3] Böscke T S, Müller J, Bräuhaus D, Schröder U and Böttger U 2011 *Appl. Phys. Lett.* **99** 102903
[4] Müller J, Böscke T S, Bräuhaus D, Schröder U, Böttger U, Sundqvist J, Kücher P, Mikolajick T and Frey L 2011 *Appl. Phys. Lett.* **99** 112901
[5] Li T, Ye M, Sun Z, Zhang N, Zhang W, Inguva S, Xie C, Chen L, Wang Y, Ke S and Huang H 2019 *ACS Appl. Mater. Interfaces* **11** 4139
[6] Liu J, Liu S, Liu L H, Hanrahan B and Pantelides S T 2019 *Phys. Rev. Appl.* **12** 034032
[7] Hu A B and Xia Q X 2010 *Chin. Phys. B* **19** 057302
[8] Trentzsch M, Flachowsky S, Richter R, Paul J, Reimer B, Utess D, Jansen S, Mulaosmanovic H, Müller S, Slesazeck S, Ocker J, Noack M, Müller J, Polakowski P, Schreiter J, Beyer S, Mikolajick T and Rice B 2016 *Proceedings of the 62th IEEE International Electron Devices Meeting (IEDM)*, December 3–7, 2016, San Francisco, America, pp. 11.5.1
[9] Yurchuk E, Müller J, Knebel S, Sundqvist J, Graham A P, Melde T, Schröder U and Mikolajick T 2013 *Thin Solid Films* **533** 88
[10] Polakowski P and Muller J 2015 *Appl. Phys. Lett.* **106** 232905
[11] Dünkel S, Trentzsch M, Richter R, Moll P, Fuchs C, Gehring O, Majer M, Wittek S, Müller B, Melde T, Mulaosmanovic H, Slesazeck S, Müller S, Ocker J, Noack M, Löhr D A, Polakowski P, Müller J, Mikolajick T, Höntschel J, Rice B, Pellerin J and Beyer S 2017 *Proceedings of the 63th IEEE International Electron Devices Meeting (IEDM)*, December 2–6, 2017, San Francisco, America, pp. 19.7.1
[12] Li X Q, George S, Liang Y H, Ma K S, Ni K, Aziz A, Gupta S K, Sampson J, Chang M F, Liu Y P, Yang H Z, Datta S and Narayanan V 2018 *IEEE Trans. Electron Devices* **65** 2670
[13] Ni K, Yin X Z, Laguna A F, Joshi S, Dunkel S, Trentzsch M, Mueller J, Beyer S, Niemier M, Hu X S and Datta S 2019 *Nat. Electron.* **2** 521
[14] Mulaosmanovic H, Mikolajick T and Slesazeck S 2018 *IEEE Electron Device Lett.* **39** 135
[15] Mulaosmanovic H, Breyer E T, Dunkel S, Beyer S, Mikolajick T and Slesazeck S 2021 *Nanotechnology* **32** 502002

[16] Yurchuk E, Muller J, Muller S, Paul J, Pesic M, van Bentum R, Schroeder U and Mikolajick T 2016 *IEEE Trans. Electron Devices* **63** 3501

[17] Gong N and Ma T P 2018 *IEEE Electron Device Lett.* **39** 15

[18] Ichihara R, Suzuki K, Kusai H, Ariyoshi K, Akari K, Takano K, Kamiya K M Y, Takahashi K, Miyagawa H, Kamimuta Y, Sakuma K and Saitoh M 2020 *Proceedings of the 39th IEEE Symposium on VLSI Technology*, June 16–19, 2020, Honolulu, America, p. 1

[19] Saitoh M, Ichihara R, Yamaguchi M, Suzuki K, Takano K, Akari K, Takahashi K, Kamiya Y, Matsuo K, Kamimuta Y, Sakuma K, Ota K and Fujii S 2020 *Proceedings of the 66th IEEE International Electron Devices Meeting (IEDM)*, December 12–18, 2020, San Francisco, America, pp. 18.1.1

[20] Toprasertpong K, Lin Z Y, Lee T E, Takenaka M and Takagi S 2020 *Proceedings of the 39th IEEE Symposium on VLSI Technology*, June 16–19, 2020, Honolulu, America, p. 1

[21] Wang Z, Tasneem N, Islam M M, Chen H, Hur J, Chern W, Yu S M and Khan A 2022 *IEEE Trans. Electron Devices* **69** 1519

[22] Xiang Y, Bardon M G, Kaczer B, Alam M N K, Ragnarsson L A, Kaczmarek K, Parvais B, Groeseneken G and Van Houdt J 2021 *IEEE Trans. Electron Devices* **68** 2107

[23] Deng S, Jiang Z H, Dutta S, Ye H C, Chakraborty W, Kurinec S, Datta S and Ni K 2020 *Proceedings of the 66th IEEE International Electron Devices Meeting (IEDM)*, December 12–18, 2020, San Francisco, America, pp. 4.4.1

[24] Ryndyk D A 2018 *Theory of Quantum Transport at Nanoscale (introduction and contents)* (Berlin: Springer)

[25] Liu L, Liu C, Jiang L, Li J, Ding Y, Wang S, Jiang Y G, Sun Y B, Wang J, Chen S, Zhang D W and Zhou P 2021 *Nat. Nanotechnol.* **16** 874

[26] Merzbacher E 1998 *Quantum Mechanics* (Hoboken: John Wiley & Sons)

[27] Lun Z Y, Li Y, Zhao K, Du G, Liu X Y and Wang Y 2016 *Chin. Phys. B* **25** 088502

[28] Herrmann M and Schenk A 1995 *J. Appl. Phys.* **77** 4522

[29] Suzuki E, Schroder D K and Hayashi Y 1986 *J. Appl. Phys.* **60** 3616

[30] Svensson C and Lundstrom I 1973 *J. Appl. Phys.* **44** 4657

[31] Fleischer S, Lai P T and Cheng Y C 1992 *J. Appl. Phys.* **72** 5711

[32] Houng M P, Wang Y H and Chang W J 1999 *J. Appl. Phys.* **86** 1488

[33] Cheng X R, Cheng Y C and Liu B Y 1988 *J. Appl. Phys.* **63** 797

[34] Gehring A, Jimenez-Molinos F, Kosina H, Palma A, Gamiz F and Selberherr S 2003 *Microelectron. Reliab.* **43** 1495

[35] Jiménez-Molinos F, Palma A, Gámiz F, Banqueri J and López-Villanueva J A 2001 *J. Appl. Phys.* **90** 3396

[36] Ni K, Sharma P, Zhang J C, Jerry M, Smith J A, Tapily K, Clark R, Mahapatra S and Datta S 2018 *IEEE Trans. Electron Devices* **65** 2461

[37] Miller S L, Schwank J R, Nasby R D and Rodgers M S 1991 *J. Appl. Phys.* **70** 2849

[38] Moglestue C 1986 *J. Appl. Phys.* **59** 3175

[39] Tian F, Zhao S, Xu H, Xiang J, Li T, Xiong W, Duan J, Chai J, Han K, Wang X, Wang W and Ye T 2021 *IEEE Trans. Electron Devices* **68** 5872

[40] Young C D, Zhao Y, Heh D, Choi R, Lee B H and Bersuker G 2009 *IEEE Trans. Electron Devices* **56** 1322

[41] Zhou H, Ocker J, Padovani A, Pesic M, Trentzsch M, Dunkel S, Mulaosmanovic H, Slesazeck S, Larcher L, Beyer S, Muller S and Mikolajick T 2020 *Proceedings of the 66th IEEE International Electron Devices Meeting (IEDM)*, December 12–18, 2020, San Francisco, America, pp. 18.6.1