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TOPICAL REVIEW — Valleytronics

Perspectives of spin-valley locking devices

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Valleytronics is an emerging field of research which utilizes the valley degree of freedom to encode information. However, it is technically nontrivial to produce a stable valley polarization and to achieve efficient control and manipulation of valleys. Spin–valley locking refers to the coupling between spin and valley degrees of freedom in the materials with large spin–orbit coupling (SOC) and enables the manipulation of valleys indirectly through controlling spins. Here, we review the recent advances in spin–valley locking physics and outline possible device implications. In particular, we focus on the spin–valley locking induced by SOC and external electric field in certain two-dimensional materials with inversion symmetry and demonstrate the intriguing switchable valley–spin polarization, which can be utilized to design the promising electronic devices, namely, valley-spin valves and logic gates.

Keywords: spin–valley locking, spintronics, valleytronics, spin–orbit coupling

PACS: 73.90.+f, 85.75.–d, 71.70.Ej, 73.63.–b **DOI:** 10.1088/1674-1056/acc809

1. Introduction

Energy extrema of band dispersion in momentum space can be exploited as a new degree of freedom, known as valleys.[1,2] The exploitation and manipulation of valleys have led to the field of valleytronics, which has aroused considerable interest recently due to fundamental interest and potential device applications.[1–3] In analogy to the spin polarization in spintronics,[4] valley polarization is characterized by electron preferentially occupying a single valley. Producing a stable valley polarization is essential for valleytronic applications. Monolayer transition metal dichalcogenides (TMDCs) MX_2 (M = Mo, W; X = S, Se, Te)[5–7] provide a promising platform to explore the rich valley physics, such as the valley selective circular dichroism,[8,9] the valley Hall effect,[10] the valley Seebeck effect,[11] valley excitons,[12] etc. For example, a large valley polarization of $\sim 30\%$ was observed in the pristine monolayer MoS_2 through optical pumping technique.[9] However, the lifetime of valley polarization induced by circularly polarized photons is very short due to the fast recombination of electron–hole pair. In addition, the valley-polarized current was proposed and demonstrated in graphene nanoribbons and monolayer MoS_2 via optical or parametric pumping technique[13–17] or by scattering at nonmagnetic disorders.[18] Another efficient way to achieve valley polarization is to lift the valley degeneracy thereby resulting in the valley splitting. Spin–valley locking[19–21] induced by large spin–orbit coupling (SOC) allows control of the valley polarization by lifting the valley degeneracy. Since the two degenerate valleys have opposite spins protected by time-reversal symmetry T, the valley degeneracy can be lifted by broking the T symmetry to induce spin splitting, which can be realized by using magnetic means such as external magnetic field[22,23] or intrinsic magnetic order.[24–28]

On the electronic device application side, in analogy to spin-valve effect,[4,29,30] valley-valve effect is the change of electrical resistance between two values modulated by valley-dependent electron transport. Since the intervalley transport requires the flipping of valley index, the current flowing is expected to be largely suppressed, which yields the high resistance state. In contrast, intravalley transport typically gives rise to relatively low electrical resistance. The valley-valve effect has been predicted for a graphene nanoribbon[31] via local application of a pair of electrostatic potentials as well as WS_2/MoS_2 van der Waals heterostructures.[32] In addition, valley-based logic gates have been proposed in a quasi-two-dimensional (2D) system with merging Dirac cones, which reveal all-electric controlled valley-filter and valley-valve effects.[33] Recently, Tao *et al.*[34] proposed valley–spin valves (VSVs) and logic gates based on the strong spin–valley locking effect in certain 2D materials. Using quantum-transport calculations on practical 2D materials-based electronic devices, a giant VSV effect of nearly 100% was predicted for both germanene- and stanene-based VSVs.[34] Further, they proposed the design of valley–spin logic gates by utilizing the predicted giant VSV effect and demonstrated the realization of seven complete logic gates, namely, NOT, XNOR, XOR, AND, NAND, OR, and NOR.[35] More importantly, the proposed valley–spin logic gates satisfy the concatenation requirement, where the output voltage of the logic gate can be used as the logic input for the successive gate.[36]

In this review article, we overview the emerging field of research devoted to spin–valley locking electronic devices.

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Starting from the basic concepts of valleytronics such as valley polarization and spin–valley locking, we introduce the switchable valley–spin polarization crucial for the design of novel electronic devices. We further discuss the specific materials exhibiting electrically switchable valley–spin polarization. Then we move to the design of valley–spin valves and logic gates. Finally, we outline the perspective of this field of research.

2. Valley–spin valves

2.1. Switchable valley–spin polarization

As previously mentioned, in analogy to spin polarization shown in Fig. 1(a), valley polarization characterizes the imbalanced electron or hole occupation numbers between degenerate valleys K and K' shown in Fig. 1(b). In the presence of SOC, bands around valleys K and K' reveal Zeeman-type spin splitting, which in turn results in spin–valley locking as shown in Fig. 1(c) and observed in TMDCs monolayer.[5] In the case of spin–valley locking, although the net spin polarization and net valley polarization are both zero, the electrons are fully spin-polarized around a given valley K or K'. Thus, one can define the valley-dependent spin polarization or valley–spin polarization as $\mathrm{VSP}_{K/K'} = (N^{\uparrow}_{K/K'} - N^{\downarrow}_{K/K'})/(N^{\uparrow}_{K/K'} + N^{\downarrow}_{K/K'})$, where N denotes the electron or hole occupation number. From Fig. 1(c), one can see that the electrons are fully spin-polarized around K or K' valley and the polarity of valley–spin polarization is positive (negative) at the K (K') valley.

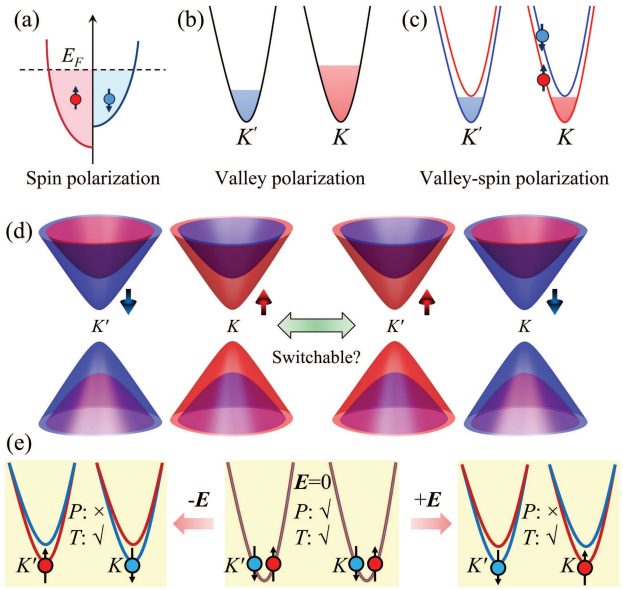


Fig. 1. Sketches of (a) spin polarization, (b) valley polarization, (c) spin–valley locking and valley–spin polarization, and (d) switchable valley–spin polarization.[35] Arrows denote the spin directions while K and K' denote two valleys, which are related by time-reversal symmetry. (e) Mechanism of switchable valley–spin polarization by electric field $\boldsymbol{E}$ in certain 2D materials with inversion (P) and time-reversal (T) symmetries.[34]

In analogy to switchable magnetization in ferromagnets or switchable polarization in ferroelectrics crucial to the design of non-volatile electronic devices, a natural question to ask is: is it possible to switch the polarity of valley–spin polarization using external means as schematically shown in Fig. 1(d)? It is found that the valley–spin polarization for the 2D materials with inversion symmetry and large SOC is indeed switchable by external electric field.[37] As shown in Fig. 1(e), we consider the 2D system with inversion (P) and time-reversal (T) symmetries and the band dispersion reveals two well-separated valleys K and K' related by T symmetry, where K or K' is a non-time-reversal-invariant momentum. In the absence of external electric field $\boldsymbol{E}$, the band structure is both spin degenerate and valley degenerate (central panel of Fig. 1(e)) due to the combination of P and T symmetries. Application of $\boldsymbol{E}$ breaks the P symmetry and the bands are spin splitting around valleys K and K' by SOC, which results in the spin–valley locking (right panel of Fig. 1(e)) and the valley–spin polarizations are opposite between the two valleys as enforced by T symmetry. Changing the sign of $\boldsymbol{E}$ is equivalent to the P symmetry operation, under which the valley K transforms to K' ($-K$) while the spin remains invariant. Thus, the polarity of valley–spin polarization is fully reversed (left panel of Fig. 1(e)). Such conclusion is based on the general symmetry analysis and is thus generally applicable.

2.2. 2D materials with switchable valley–spin polarization

Having demonstrated the switchable valley–spin polarization based on the general symmetry analysis, we next exemplify this phenomenon in the specific 2D materials based on a tight-binding model or density functional theory (DFT) calculations. As previously demonstrated,[34] the switchable valley–spin polarization by electric field can be realized in a large number of 2D materials such as silicene,[38,39] germanene,[40] stanene,[41,42] 1T′-MX_2 monolayer,[43] and 2H-MX_2 bilayer (M = Mo, W; X = S, Se, Te).[44] Those 2D materials have inversion symmetry and have been successfully synthesized. Figures 2(a)–2(c) show the calculated band structure for the stanene tunable by electric field E_z. For $E_z = 0$ (Fig. 2(a)), a band gap of 0.2 eV is opened at the K and K' valleys by SOC, and the bands are spin and valley degenerate due to the combination of P and T symmetries. For finite E_z (Figs. 2(b) and 2(c)), the band structure is spin splitting and fully spin polarized around the K and K' valleys. Comparing Fig. 2(b) with Fig. 2(c) reveals that changing the sign of E_z interchanges the roles of spin up and down electrons, which in turn switches the valley–spin polarization. Figures 2(d)–2(f) show the DFT calculated electronic structure of 1T′-MoS_2 monolayer around the K and K' valleys. Similar to the stanene, in the absence of E_z, the band structure exhibits two spin-degenerate valleys (Fig. 2(d)). Application of E_z splits the bands into two spin subbands with opposite spin polarizations at the two valleys K and K' (Fig. 2(e)). Importantly, the po-

larity of the valley–spin polarization is reversed by changing the direction of E_z (Fig. 2(f)). A similar behavior is also observed for the 2H-MoS_2 bilayer, as seen from Figs. 2(g)–2(i). The spin degeneracy of the two-valley band structure is lifted by E_z with spin polarization being opposite at the two valleys and being reversed with the reversal of E_z. It is seen that the numerical calculations are consistent with above general symmetry analysis. In the above band structure calculations for the stanene and the following quantum transport calculations for the stanene-based electronic devices, the low-energy tight-binding Hamiltonian is given by[45–47]

$$H = -t\sum_{\langle i,j\rangle\alpha} c^{\dagger}_{i\alpha}c_{j\alpha} + \mathrm{i}\frac{\lambda_{\mathrm{SO}}}{3\sqrt{3}}\sum_{\langle\langle i,j\rangle\rangle\alpha,\beta} \nu_{ij}c^{\dagger}_{i\alpha}\sigma_z^{\alpha\beta}c_{j\beta} + \mathrm{i}\lambda_{\mathrm{R1}}\sum_{\langle i,j\rangle\alpha,\beta} c^{\dagger}_{i\alpha}\left(\boldsymbol{\sigma}\times\hat{d}_{ij}\right)^{z}c_{j\beta} \quad (1)$$

$$-\mathrm{i}\frac{2\lambda_{\mathrm{R2}}}{3}\sum_{\langle\langle i,j\rangle\rangle\alpha,\beta}\xi_i c^{\dagger}_{i\alpha}\left(\boldsymbol{\sigma}\times\hat{d}_{ij}\right)^{z}c_{j\beta} + lE_z\sum_{i\alpha}\xi_i c^{\dagger}_{i\alpha}c_{i\alpha}, \quad (2)$$

where the first term is the nearest-neighbor hopping, $c^{\dagger}_{i\alpha}$ ($c_{j\alpha}$) is an electron creation (annihilation) operator at the site i (j) with spin $\alpha =\uparrow, \downarrow$, t is the hopping parameter and $\langle i,j\rangle$ denotes the sum over the nearest-neighbor sites. The second term represents the intrinsic SOC with strength λ_{SO}, $\langle\langle i,j\rangle\rangle$ denotes the sum over the next-nearest-neighbor sites, σ_z is the z-component of the Pauli matrix, and $\nu_{ij} = +1$ (-1) selects anticlockwise (clockwise) hopping with respect to the z axis. The third term represents the Rashba SOC induced by an external electric field, and the fourth term is the intrinsic Rashba SOC. Our previous work[34] demonstrates that λ_{R1} is significantly smaller than λ_{SO}, and the intrinsic Rashba SOC (λ_{R2}) has a negligible effect. Both Rashba terms are therefore ignored. The last term arises from the applied electric field E_z, $\xi_i = +1$ (-1) distinguishes site $i = A$ (B), and $2l$ is the A–B sublattice buckling height. According to Eq. (1), when $\lambda_{\mathrm{R1}} = \lambda_{\mathrm{R2}} = 0$, $[\sigma_z, H] = 0$, and the spin component σ_z is a good quantum number. The following tight-binding parameters $t = 1.3$ eV, $\lambda_{\mathrm{SO}} = 0.1$ eV, and $l = 0.4$ Å are used for the stanene.

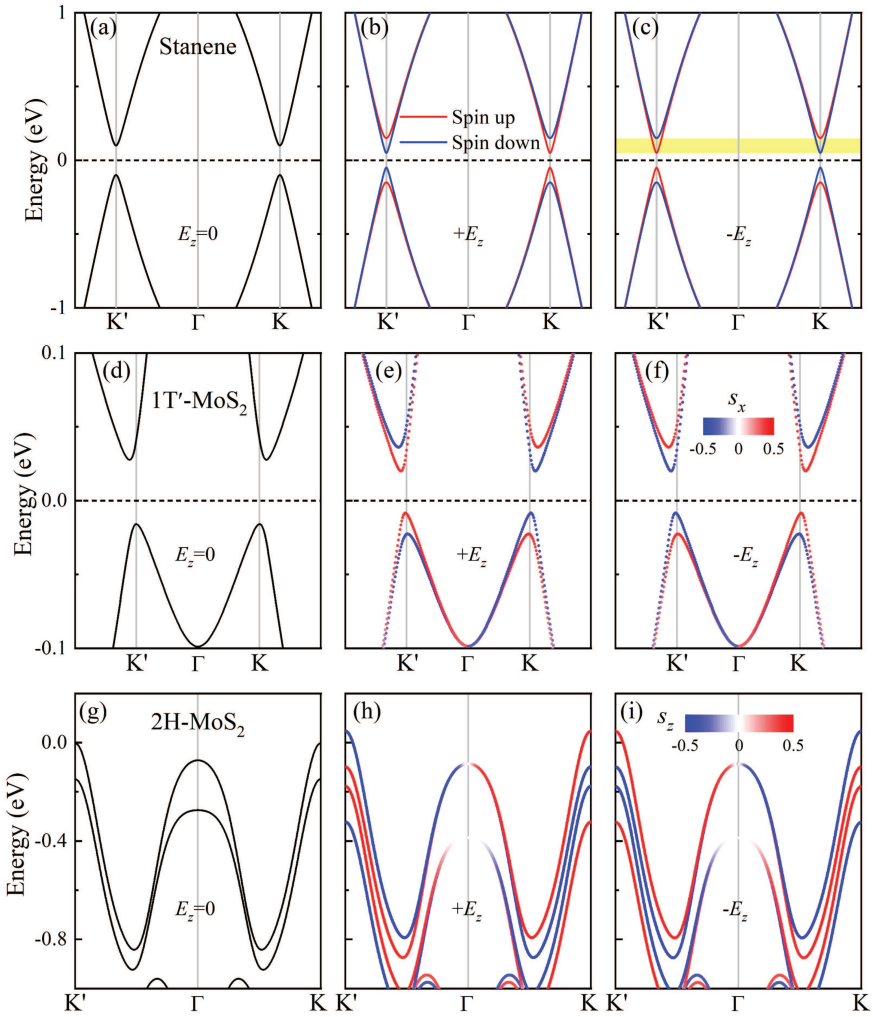


Fig. 2. Calculated E_z tunable band structure for (a)–(c) stanene, (d)–(f) 1T′-MoS_2 monolayer, and (g)–(i) 2H-MoS_2 bilayer.[34] In (c), yellow region denotes the energy window to achieve a giant VSV effect. In the calculations, the magnitude of E_z is 1.25 V/nm for stanene, 5 V/nm for 1T′-MoS_2, and 1 V/nm for 2H-MoS_2. The color quantifies the expectation value of s_x in (e), (f) and s_z in (h), (i).

2.3. Valley–spin valve effect

The switchable valley–spin polarization can be exploited to design the novel electronic device, this is, valley–spin valve (VSV). Figure 3(a) shows the two-terminal device model for the VSV, where the two regions designated as 1 and 2 serve as a valley–spin polarizer and a valley–spin analyzer, respectively. The working principle for the VSV can be understood from the schematic band alignments shown in Fig. 3(b). To be specific, the incoming electrons are neither spin polarized nor valley polarized. In region 1, the application of electric field $\boldsymbol{E}$ breaks the inversion symmetry and results in spin–valley locking so that electrons are spin-up polarized in valley K and spin-down polarized in valley K'. In region 2, the valley–spin analyzer selects electrons according to their valley–spin polarization, which can be controlled by the sign of E. If the field in region 2 is parallel to that in region 1, the valley–spin polarization of the analyzer is the same as that of the polarizer, and both spin-up and spin-down electrons can be efficiently transmitted through the intravalley transport. This configuration is expected to have low resistance (ON state). On the contrary, if the applied field in region 2 is antiparallel to that in region 1, the valley–spin polarization of the analyzer is opposite to that of the polarizer, and either spin electrons encounter a potential barrier for the intravalley transport. Thus, this configuration is expected to produce much higher resistance of the device (OFF state). Such resistance difference between ON and OFF states is dubbed as the VSV effect.

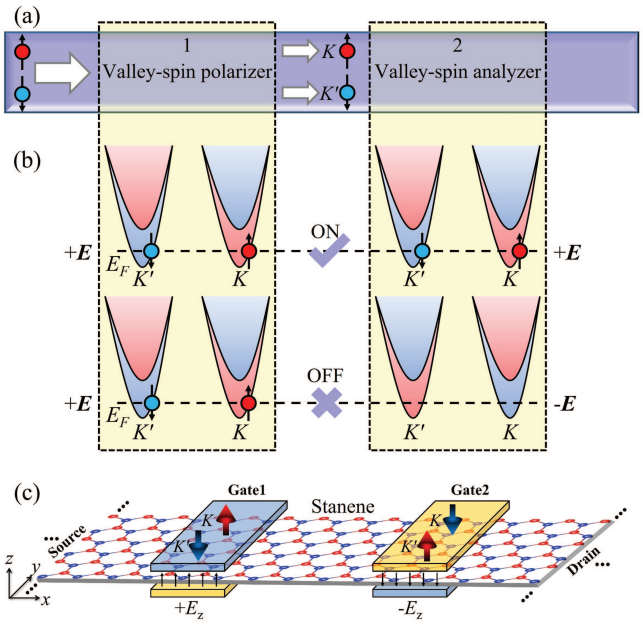


Fig. 3. (a) Schematic two-terminal device model for the valley–spin valve.[34] Regions 1 (spin–valley polarizer) and 2 (spin–valley analyzer) are applied with external electric field $\boldsymbol{E}$. (b) Band alignments between regions 1 and 2.[34] The dashed line indicates the Fermi energy E_F. Electrons (filled circles) can either be transmitted (ON state) or blocked (OFF state) depending on the relative orientation of $\boldsymbol{E}$ in regions 1 and 2. (c) Sketches of a stanene-based valley–spin valve device.[34] The two gates of width d_1 are separated by distance d_2. E_z (black solid arrows) is the electric field generated by the gate voltage. The red and blue arrows denote spin orientations in the K and K' valleys for each gated region.

The feasibility of VSV effect was demonstrated in the stanene-based devices, as shown in Fig. 3(c) with double gates placed within the central region. The device state is defined as "parallel" ("anti-parallel") when the electric fields E_z are parallel (antiparallel) between gates 1 and 2. VSV conductance ratio η characterizing the VSV effect is defined as $\eta = (G_P - G_{AP})/(G_P + G_{AP})$, with G_P (G_{AP}) being the total conductance for the device in the parallel (antiparallel) state. Conductance G at energy E is calculated by using the Landauer–Büttiker formula[48] as $G(E) = \left(e^2/h\right)\sum_{\sigma,k_y} T_\sigma(E,k_y)$, where e is the electron charge, h is the Planck's constant, T_σ is the transmission for spin σ. k_y is the transverse Bloch wave vector, which is conserved in the transport process.

Figure 4(a) shows the calculated conductance versus the Fermi energy E_F for parallel (G_P) and antiparallel (G_{AP}) states and the resulting VSV conductance ratio η. It is seen that when E_F is close to the conduction band minimum E_c, G_P is about four orders of magnitude larger than G_{AP} and η is nearly 100% within the energy window (yellow colored region and Fig. 2(c)), indicating a giant VSV effect. Figure 4(b) shows G_P, G_{AP} and η as a function of E_z for $E_F = 0.01$ eV. As can be seen, the difference between G_P and G_{AP} increases significantly with increasing E_z and decreases slightly at larger E_z. As a consequence, η increases significantly and saturates at about 100% after certain E_z. It is seen that the giant VSV effect can be achieved in the VSV device constructed by certain 2D materials with electrically switchable valley–spin polarization. More importantly, the giant VSV effect is robust against the disorder due to the well-separated K and K' valleys. Figure 4(c) shows the averaged conductance and the VSV ratio as a function of disorder strength W. We assume an Anderson-type disorder in the central region, which is modeled by adding a random on-site potential uniformly distributed in the range from $-W/2$ to $W/2$. It is seen that, under weak disorder ($W < 10$ meV), the averaged conductance and the VSV ratio η are nearly independent of W. When 10 meV$< W <$ 100 meV, $\langle G_{AP}\rangle$ increases monotonically with increasing W due to valley-mix scattering, while $\langle G_P\rangle$ is almost unchanged. When $W > 100$ meV, η decreases monotonically with W. The shaded area represents the realistic strength of disorder, which produces the sheet resistance of stanene comparable to experimentally measured value.[49] Thus, VSV is largely robust against the disorder scattering. Figure 4(d) schematically shows the electron scattering processes in the AP (OFF) state. We can see that the intravalley scattering is forbidden due to the opposite spin polarizations while the intravalley scattering is allowed contributing to the G_{AP}. However, the two K and K' valleys are well separated by a wavevector comparable to the size of the Brillouin zone. Thus, intervalley scattering is equivalent to a large momentum transfer, which requires a very strong random potential. Thus, the well-separated K and K' valleys are responsible for the robustness of VSV effect against the disorder.

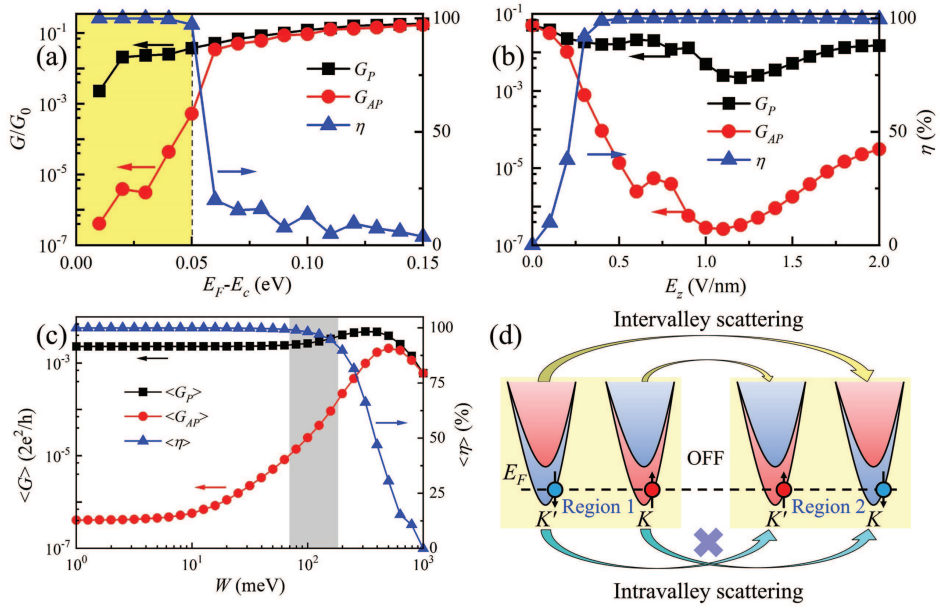


Fig. 4. Calculated conductance (G_P and G_{AP}) in units of $G_0 = 2e^2/h$ (left axis) and VSV conductance ratio η (right axis) as a function of (a) the Fermi energy E_F and (b) electric field E_z assuming $d_1 = 100a$ and $d_2 = 20a$.[34] The yellow region in (a) denotes the energy window for achieving a giant VSV effect. (c) Calculated averaged conductance $\langle G_P \rangle$ and $\langle G_{AP} \rangle$ (left axis) and the VSV ratio η (right axis) for stanene as a function of disorder strength W.[34] The shaded region indicates a range of experimentally measured sheet resistances. (d) Schematic intervalley and intravalley scatterings in the AP state (OFF state).

3. Valley–spin logic gates

One can further design the logic gates based on the VSV device. Figure 5(a) schematically shows a prototype four-terminal building block for the design of XNOR and XOR gates. The source and drain are connected by a 2D channel, whose transport properties are controlled by gates A and B. The logic inputs are encoded by the polarity of gate voltage and positive (negative) voltage corresponds to logic input 1 (0). According to the VSV effect, the device conductance is high (ON state) or low (OFF state) depending on the relative voltage polarities between gates A and B, as schematically shown in Fig. 5(b). Figures 5(c) and 5(d) show the designs of XNOR and XOR gates, respectively. A and B serve as logic inputs while the logic output is encoded by the polarity of the output voltage. From Fig. 5(c), when the logic inputs $A = B = 1$ or 0, the top circuit is in ON state while the bottom circuit is in OFF state, and the output voltage is +VDD, corresponding to logic 1. When the logic inputs $A \neq B$ ($A = 1$, $B = 0$ or $A = 0$, $B = 1$), the top circuit is in OFF state while the bottom circuit is in ON state, and the output voltage is −VDD, corresponding to logic 0. According to the truth table of XNOR gate, the XNOR logic operation is realized. The working principle for XOR gate can be understood in the same way. It is noteworthy that the NOT gate can be realized from the XNOR gate by setting A to 0 or from the XOR gate by setting A to 1.

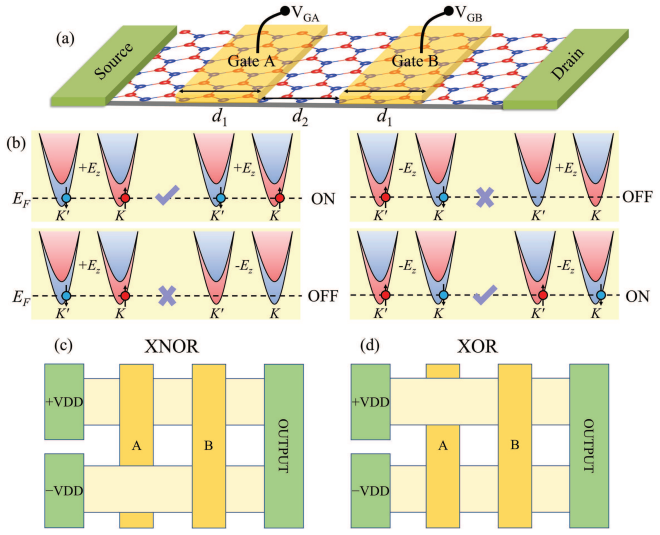


Fig. 5. (a) Schematic of the four-terminal device model with two gates A and B.[35] The source and drain are directly connected to the 2D channel. (b) Band alignments at the gate regions for different gate polarities determined by the electric field E_z.[35] Electrons (filled circles) can be transmitted (ON state) or blocked (OFF state) depending on the polarity of E_z in the gated regions. Schematics of (c) XNOR and (d) XOR gates.[35] The light-yellow regions represent 2D channels. Gates A and B act as two logic inputs. Gate A serves as a top gate or back gate, providing an invert of A input in the latter case. VDD is the supply voltage, providing +VDD (−VDD) voltage in the upper (lower) circuit.

The design of other logic gates, namely, OR, NOR, AND, and NAND gates, requires a five-terminal building block shown in Fig. 6(a), where three gates A, B, and C are involved. Depending on the relative input polarities of the gates, the device can either be in high conductance state (ON state) or in low conductance state (OFF state), as shown in Fig. 6(b). Figure 7 shows the designs of OR, NOR, AND, and NAND gates. The working principle for OR gate (Fig. 7(a)) can be understood as follows: Control gate CTRL is set to −VDD, and when $A = B = 0$ (−VDD), the two upper devices are in OFF state while the lower one is in ON state. Hence, the output voltage is going to be close to −VDD corresponding to logic

state 0. In other cases, the lower device is in OFF state while one of the two upper devices is in ON state. Hence, the output voltage is going to be close to +VDD corresponding to logic state 1. According to the truth table of OR gate, the OR logic operation is realized. The working principles for the other three gates can be understood in the same way.

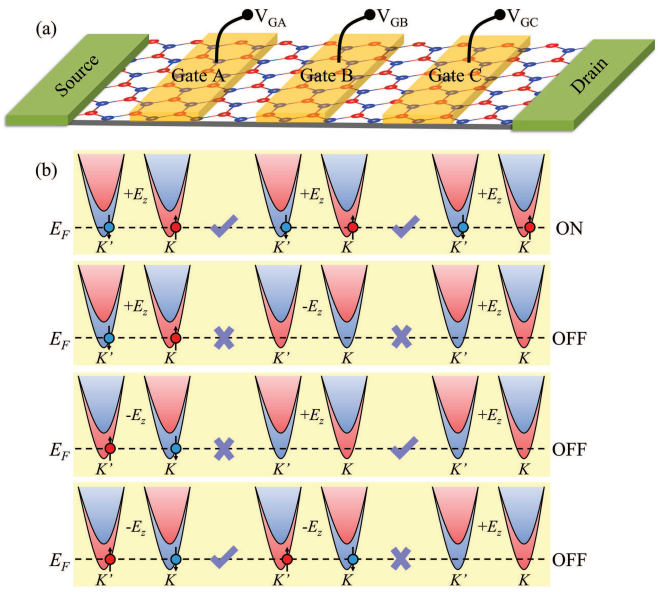


Fig. 6. (a) Schematic of the five-terminal device model with three gates A, B, and C.[35] (b) Band alignments at the gate regions for different gate polarities determined by the electric field E_z.[35] Dashed lines denote the Fermi energy E_F. Electrons (filled circles) can be transmitted (ON state) or blocked (OFF state) depending on polarity of E_z in the gated regions.

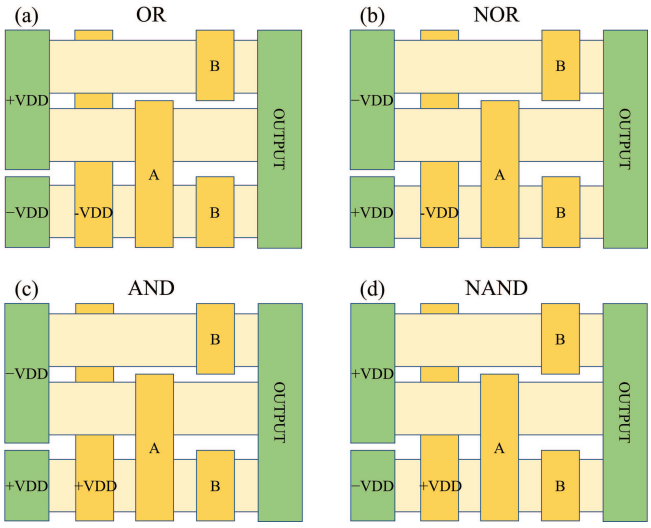


Fig. 7. Schematics of (a) OR, (b) NOR, (c) AND, and (d) NAND gates.[35] VDD is the supply voltage.

To summarize, based on the VSV device and giant VSV effect, one can design the seven complete logic gates, namely, NOT, XNOR, XOR, AND, NAND, OR, and NOR. More importantly, the proposed valley–spin logic gates satisfy the concatenation requirement, where the output voltage of the logic gate can be used as the logic input for the successive gate.

4. Summary and outlook

In summary, we have reviewed the recent advances in spin–valley locking physics and device applications, including the valley–spin valves and logic gates. One can define the valley–spin polarization based on spin–valley locking, and more interestingly, certain 2D materials with inversion symmetry and large SOC reveal electrically switchable valley–spin polarization. Such an intriguing property enables valley manipulation by all electrical means and provides an efficient way to control the valley degree of freedom. Switchable valley–spin polarization can be used to design the promising electronic devices such as valley–spin valves and logic gates. For the former, giant VSV effect is demonstrated based on quantum transport calculations on practical 2D materials-based devices and is robust against the disorder scattering. For the latter, seven complete logic gates, namely, NOT, XNOR, XOR, AND, NAND, OR, and NOR, can be realized. More importantly, the concatenation requirement crucial for programmable logic devices is satisfied. Since the operations of the proposed spin–valley locking devices are based on all-electric means, the fast-switching speed and low-power consumption are expected.[36]

Overall, spin–valley locking is a thriving field of research with extraordinary prospects both for the fundamental physics and for practical applications. Looking forwards, the research of spin–valley locking can be extended into some burgeoning materials such as oxides,[37] van der Waals,[50] moiré heterostructures,[51–53] topological quantum materials,[54,55] etc. In particular, in ferroelectric materials with large SOC,[37,56–58] the extrema (valleys) of band dispersions such as the conduction band minimum or the valence band maximum are spin polarized. As a result, the spin, valley and ferroelectric polarization are intrinsically coupled, which opens up new avenues of research. In bilayer TMDCs, one could explore the gate-controlled spin–valley–layer locking.[59] In certain 2D ferromagnetic materials, the magnetization and valley are intrinsically locked, which enables the switchable valley–spin polarization by magnetization and results in anomalous valley Hall effect.[60] Moreover, the coupling of the valley and antiferromagnetic order in certain 2D antiferromagnetic materials enables the optical polarization in the spin–valley space,[61] magnetoelectric coupling[62] and the design of novel spin filed effect transistors.[63] Regarding the experimental realization of the proposed spin–valley locking devices, the 2D materials such as germanene and stanene have been successfully synthesized and the double-gate technique has been widely employed in 2D electronic devices.[64,65] To protect the spin coherence against the relaxation crucial for the experimental verification, it is crucial to achieve high-quality materials with minimizing interfacial strains and low defects. In future, one could also explore

the spin–valley locking in topological quantum materials[54,55] and design novel electronic devices[66] based on topological protection.

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