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Modulated optical and ferroelectric properties in a lateral structured ferroelectric/semiconductor van der Waals heterojunction

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Modulation between optical and ferroelectric properties was realized in a lateral structured ferroelectric $CuInP_2S_6$ (CIPS)/semiconductor MoS_2 van der Waals heterojunction. The ferroelectric hysteresis loop area was modulated by the optical field. Two types of photodetection properties can be realized in a device by changing the ON and OFF states of the ferroelectric layer. The device was used as a photodetector in the OFF state but not in the ON state. The higher tunnelling electroresistance ($\sim 1.4 \times 10^4$) in a lateral structured ferroelectric tunnelling junction was crucial, and it was analyzed and modulated by the barrier height and width of the ferroelectric CIPS/semiconductor MoS_2 Schottky junction. The new parameter of the ferroelectric hysteresis loop area as a function of light intensity was introduced to analyze the relationship between the ferroelectric and photodetection properties. The proposed device has potential application as an optoelectronic sensory cell in the biological nervous system or as a new type of photodetector.

Keywords: ferroelectric tunnelling junction, metal/ferroelectric/semiconductor, tunnelling electroresistance, optoelectronic properties

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1. Introduction

Memristors are ideal building blocks for brain-like neuromorphic devices.[1–6] A two-terminal structured ferroelectric tunnelling junction (FTJ) has transmission properties similar to the biological synapse; its top and bottom electrodes are commonly used to mimic the presynaptic and postsynaptic membranes in biological synapses.[7] Traditional memristors that achieve basic synaptic functions by applying voltage alone are purely electronic synapses; however, they lack the function of mimicking sensory cells in a biological nervous system.

Some researchers have introduced light stimulation to mimic functions in sensory cells.[7–10] Shen *et al.* reported TiN_xO_{2-x}/MoS_2/indium tin oxide (ITO) devices that showed basic analog resistive switching behavior and various basic synaptic functions such as short-term plasticity and long-term plasticity, and finally constructed a 4×4 photoelectric synapse array that was used to simulate human visual perception and visual memory functions.[7] To achieve light stimulation, most artificial optoelectronic synapses are typically designed as vertical structures with transparent ITO as the top electrode. However, it is challenging to fabricate thin ITO films; the transmittance of ITO is generally $< 90\%$ and it decreases with increase in film thickness.[8] Lateral structured devices fabricated using a thin two-dimensional (2D) material can be used to realize the role of light-stimulated synapses.

Two-dimensional (2D) ferroelectric $CuInP_2S_6$ (CIPS) has shown excellent ferroelectric properties;[11–13] it can be used to switch polarization in flakes down to several layers at room temperature,[11] and it can be easily integrated onto flat substrates to form FTJ devices due to their strong intralayer coupling and weak interlayer interactions.[13] Recently, Sun and colleagues showed that a tunnelling electroresistance (TER) of over 10^7 could be obtained by using a thin $CuInP_2S_6$/graphene junction.[12] Further research could help realize sensory devices using CIPS as a ferroelectric material.

As a 2D semiconductor material, MoS_2 has a strong and fast photoresponse[14,15] that benefits the integration of field-effect transistors into other new sensing devices. Furthermore, van der Waals (vdW) heterojunctions based on MoS_2 and other materials, including MoS_2/Si,[16] MoS_2/WSe_2[17] and MoS_2/h-BN/graphene,[18] are widely used in optoelectronic applications. Based on the advantages of MoS_2, combining it with CIPS to construct a lateral structured Au/CIPS/MoS_2/Au vdW heterojunction could possibly realize sensory devices with 2D vdW junctions.

Semiconductors are also crucial for forming a Schottky barrier to obtain a higher TER, which is essential for the FTJ.[19–24] For vertical structured FTJ devices, an enhanced TER ($\sim 10^3$–10^4) can be obtained using the ferroelectric/semiconductor heterojunction.[22–24] To the best of our knowledge, no lateral structured ferroelectric/semiconductor

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FTJ with a higher TER ($> 10^4$) has been reported.

2. Results and discussion

We demonstrated that lateral structured Au/CIPS/MoS_2/Au vdW heterojunctions could be used in planar FTJ devices, combining excellent TER and optical properties. Figure 1(a) shows a schematic diagram of a lateral structured device. Ferroelectric CIPS flakes were used as the ferroelectric material to realize polarized ON and OFF states. Semiconductor MoS_2 flakes were used to modulate the barrier height and width of the memristors and as the optoelectronic material of the photodetector. Both CIPS and MoS_2 flakes were transferred onto a patterned high-work-function Au electrode; details are presented in the supporting information section 'Device fabrication'. Devices with different ferroelectric mechanisms and *I*–*V* characteristics are shown in Fig. 1.

The formation mechanisms of the ON and OFF states of the proposed CIPS/MoS_2 heterojunction were analyzed and are shown in Fig. 1(b). The work function of Au is 5.1 eV,[25] the electron affinity of CIPS is 3.7 eV and the indirect band gap of MoS_2 is 1.365 eV.[12,26] When different voltages were applied to the device, the polarization directions of CIPS were different, resulting in two different resistance states. The polarization direction of CIPS pointed to MoS_2 when a positive polarization voltage was applied, which generated pairs of bound polarized charges in the dielectric CIPS flakes (left of Fig. 1(b)). The positive bound polarized charges attracted electrons in MoS_2, causing the accumulation of electrons at the MoS_2 surface of the CIPS–MoS_2 interface. Thus, the depletion region of MoS_2 was annihilated. The conductivity of MoS_2 also improved when electrons gathered at the MoS_2 surface to fill the conduction band of MoS_2. In this case, MoS_2 flakes were the n^+-type semiconductor that formed the metal/ferroelectric/semiconductor-type FTJ.[24,27,28] A depolarization field, opposite to the polarization direction, was easily formed in the CIPS ferroelectric barrier and benefited from the incomplete screening of the MoS_2 films. Such a depolarization field lowers the Schottky barrier height (SBH) and generates a higher tunnelling transmittance, inducing a larger tunnelling current.[29] Therefore, the decreased barrier height at the CIPS–MoS_2 interface resulted in a low resistance (ON state).

In contrast, the CIPS polarization direction deviated from the MoS_2 flakes when a negative polarization voltage was applied (right side of Fig. 1(b)). Negative bound polarized charges caused the depletion of electrons at the MoS_2 side of the CIPS–MoS_2 interface. The width of the depletion region (i.e., the effective barrier width) increased due to electron depletion at the interface,[20] and the accumulation of holes at the CIPS–MoS_2 interface decreased the conductivity of MoS_2. The immobile ionized donors at the MoS_2 surface screened the negative bound polarized charges at the CIPS surface. Such screening is usually insufficient[24,27,28] to produce a depolarization field and increases the SBH at the CIPS–MoS_2 interface. The increased barrier width and height provide greater resistance to stop the tunnelling current through the heterojunction, resulting in a device with high resistance (OFF state). The realization of ON and OFF states can be mainly attributed to the modulation of the SBH and width by the CIPS polarization reversal and the screening of the MoS_2 flakes.

Semiconductor MoS_2 is crucial for modulating the barrier width and height to improve TER. To analyze the effect of the semiconductor MoS_2, an Au/CIPS/Au FTJ without MoS_2 flakes was also fabricated (Fig. 1(d)). The formation mechanisms of the ON and OFF states are analyzed in Fig. 1(e). The top Au electrode (work function = 5.24 eV)[30] was prepared using the transfer method (details in the supporting information section 'Au electrode fabrication, release, transferring and lamination process'), and the bottom Au electrode (work function = 5.1 eV)[25] was customized using photolithography to realize the asymmetry of the electrodes. At different voltages, the electric field-induced CIPS polarization changed the band alignment of CIPS at the Au–CIPS interface, resulting in two resistance states (ON and OFF states). When the polarization direction of CIPS is upward, negatively polarized charges are generated at the bottom of the CIPS and positively polarized charges accumulate on the top of the CIPS. The ferroelectric polarized charges cannot be fully compensated by the electrode charges due to interfacial effects.[31] The built-in internal field is directed from the positive to the negative polarized charges, causing the SBH to be reduced.[29,31] The device is in a low-resistance state (ON state). When the polarization direction of CIPS is downward, the CIPS generates the opposite polarized charges and the polarization reversal of CIPS alters the built-in internal field, which increases the SBH.[29,31] The device is in a high-resistance state (OFF state). Such vertical structured Au/CIPS/Au only modulated the barrier height to improve TER.

TER is considerably influenced by the width and height of the potential barrier;[29] the equation for TER is given by[32]

$$\mathrm{TER} = \frac{J_{\mathrm{ON\ state}} - J_{\mathrm{OFF\ state}}}{J_{\mathrm{OFF\ state}}}. \tag{1}$$

Under the Wentzel–Kramers–Brillouin (WKB) approximation, the current density is given by[33]

$$J \cong C\frac{\exp\left\{\alpha(V)\left[\left(\varphi_2 - \frac{eV}{2}\right)^{\frac{3}{2}}\right] - \left(\varphi_1 + \frac{eV}{2}\right)^{\frac{3}{2}}\right\}}{\alpha^2(V)\left[\left(\varphi_2 - \frac{eV}{2}\right)^{\frac{1}{2}} - \left(\varphi_1 + \frac{eV}{2}\right)^{\frac{1}{2}}\right]^2} \times \sinh\left\{\frac{3}{2}\alpha(V)\left[\left(\varphi_2 - \frac{eV}{2}\right)^{\frac{1}{2}} - \left(\varphi_1 + \frac{eV}{2}\right)^{\frac{1}{2}}\right]\frac{eV}{2}\right\}, \tag{2}$$

where C and $\alpha(V)$ are expressed as $C=-(4em)/(9\pi^2\hbar^3)$ and $\alpha(V)=[4d(2m)^{1/2}]/[3\hbar(\varphi_1+eV-\varphi_2)]$. If the difference between potential steps $\Delta\varphi\equiv\varphi_2-\varphi_1$ is too small compared with the average potential barrier, $\bar{\varphi}\equiv(\varphi_2+\varphi_1)/2$, then $\Delta\varphi/2<\bar{\varphi}$. In the case of a small bias voltage, Eq. (2) can be approximated as[32]

$$J\approx\frac{e^2}{h}\frac{1}{2\pi d}\frac{\sqrt{2m\bar{\varphi}}}{\hbar}\exp\left[-2\frac{\sqrt{2m\bar{\varphi}}}{\hbar}d\right]V, \tag{3}$$

where d is the barrier width, m is the effective mass of electrons in the potential barrier, h is Planck's constant, $\hbar$ is the reduced Planck's constant, e is the electron charge, V is the bias voltage and $\varphi_1(\varphi_2)$ is the barrier height at the Au/CIPS (CIPS/MoS_2) interface. From Eq. (3), TER depends on the average barrier height $\bar{\varphi}$ and the barrier width d when the polarization of the CIPS flakes is reversed. Let us assume that $\delta\varphi$ is the change in the barrier height from $\bar{\varphi}-\Delta\varphi/2$ (ON state, current density $J_{\text{ON state}}$) to $\bar{\varphi}+\Delta\varphi/2$ (OFF state, current density $J_{\text{OFF state}}$), then TER is expressed as[32]

$$\text{TER}\approx\exp\left[\frac{\sqrt{2m}}{\hbar}\frac{\delta\varphi}{\sqrt{\bar{\varphi}}}d\right]. \tag{4}$$

Therefore, TER increases with the barrier height $\delta\varphi$, as expressed in Eq. (4). The change in the barrier height of the CIPS–MoS_2 interface is much larger than that of the CIPS–Au interface when the barrier height of the CIPS–MoS_2 interface is modulated, which increases TER.

Obviously, TER increases with an increase in the barrier width of the depletion region d, as calculated using Eq. (4). The barrier width of the depletion region is related to the effective free carrier concentration of the semiconductor. The relationship between the width of the depletion region and the effective free carrier concentration is shown below:[34]

$$d=\sqrt{\frac{2\varepsilon_s V_{\text{bi}}}{eN_{\text{eff}}}}, \tag{5}$$

where ε_s is the dielectric constant of semiconductors, V_{bi} is the built-in potential and N_{eff} is the effective free carrier concentration.

For the case of n^+-type MoS_2, the effective free carrier concentration decreases at high resistance (OFF state), which can be attributed to the depletion of electrons at the MoS_2 surface, increasing the width of the depletion region.

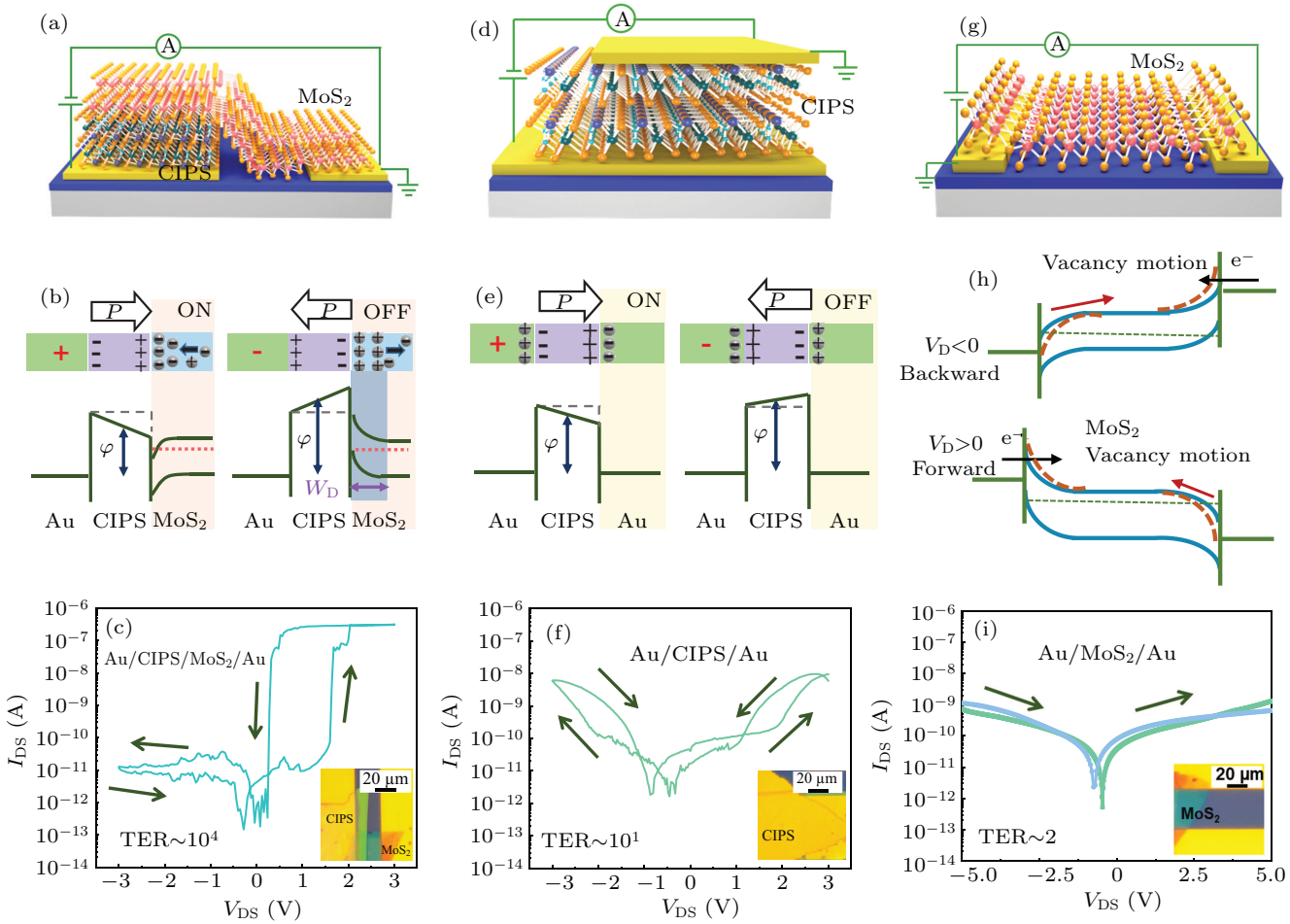


Fig. 1. (a) Schematic diagram of a lateral structured Au/CIPS/MoS_2/Au vdW FTJ. (b) Band diagrams for the ON and OFF states of the Au/CIPS/MoS_2/Au vdW FTJ. (c) *I*–*V* curve of the Au/CIPS/MoS_2/Au vdW FTJ with clear switching behavior and low operation voltage. (d) Schematic diagram of a vertical structured Au/CIPS/Au FTJ. (e) Band diagrams for the ON and OFF states of the Au/CIPS/Au FTJ. (f) *I*–*V* curve of the Au/CIPS/Au vdW FTJ with switching behavior. (g) Schematic diagram of a lateral structured Au/MoS_2/Au. (h) Band diagrams at different bias voltages of the lateral structured Au/MoS_2/Au. The green curve above represents the conduction band before the voltage sweep and the red dotted line represents the change in the Schottky barrier height. (i) *I*–*V* characteristics of the Au/MoS_2/Au junction in both forward and backward states; the inset is an optical image of the device.

However, for the Au/CIPS/Au device, it is difficult to change the barrier width at the CIPS–Au interface. Therefore, the change in the barrier width shows that the TER of the Au/CIPS/MoS_2/Au vdW FTJ is higher than that of the Au/CIPS/Au FTJ. Thus, the analysis of the effects of barrier height and width on the improvement of TER suggested that an Au/CIPS/MoS_2/Au vdW FTJ can significantly improve TER.

Experimental *I*–*V* hysteresis loops of Au/CIPS/MoS_2/Au and Au/CIPS/Au junctions are shown in Figs. 1(c) and 1(f). The asymmetric hysteresis of the Au/CIPS/MoS_2/Au FTJ may be attributed to the asymmetric contact.[35] *I*–*V* characteristics of the devices in the voltage range from 3 to −3 V are shown in Fig. S2. In the OFF state, the tunnelling current of the proposed Au/CIPS/MoS_2/Au FTJ is one order of magnitude smaller than that of the Au/CIPS/Au FTJ. In the ON state, the tunnelling current of the proposed Au/CIPS/MoS_2/Au FTJ is two orders of magnitude larger than that of the Au/CIPS/Au FTJ. Thus, introducing MoS_2 to the construction of lateral structured Au/CIPS/MoS_2/Au vdW FTJ devices significantly improves the TER (by three orders of magnitude). A TER of $\sim 1.4 \times 10^4$ was obtained for the proposed lateral structured Au/CIPS/MoS_2/Au vdW FTJ devices.

The ferroelectric properties of CIPS are crucial. The Au/MoS_2/Au junction without the CIPS flakes [Fig. 1(g)] resembles only a Schottky diode.[36] The inhibitory behavior of the MoS_2–Au potential barrier for improving TER is almost negligible. The modulation of the MoS_2/Au SBH can be qualitatively described by the band diagrams shown in Fig. 1(h). According to Li *et al.*, the switching behavior of resistance states is mainly attributed to the redistribution of sulfur (S) vacancies under the electric field.[37] The influence of impurity movement on the interface between MoS_2 and the substrate, and the adsorption of charged impurities by MoS_2 in the environment, are ignored. Under negative bias (backward), S vacancies drift from the left to the right electrode.[37] This decreases and increases the density of S vacancies at the left and right electrodes, respectively. As a result, the SBH on the left and right sides decreases and increases, respectively. Conversely, under positive bias (forward), S vacancies drift from the right to the left electrode. Their *I*–*V* characteristics are shown in Fig. 1(i). The $I_{\text{forward}}/I_{\text{backward}}$ ratio is extremely small under both positive and negative biases. The defects of S vacancies drift under voltage bias, and any further influence of barrier height and width in the Au/CIPS/MoS_2/Au devices is almost negligible. Thus, data retention can be attributed to the polarization-induced ON–OFF states.

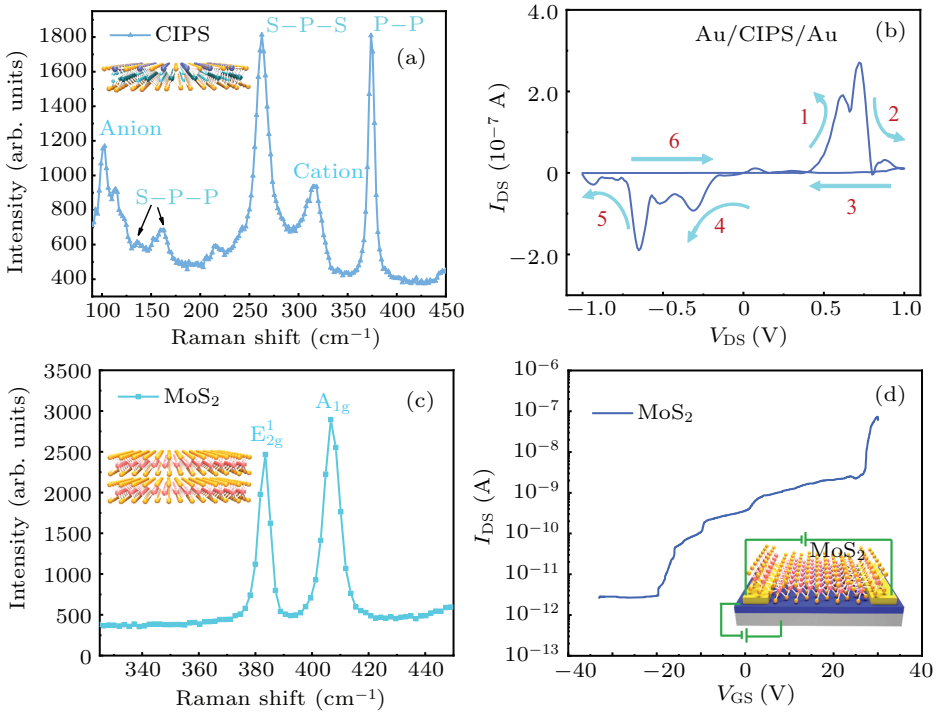


Fig. 2. (a) Raman spectra of CIPS flakes measured at room temperature. (b) *I*–*V* characteristics of CIPS flakes. (c) Raman spectra of MoS_2 flakes measured at room temperature. (d) I_{DS}–V_G characteristics of the MoS_2 transistors.

The CIPS and MoS_2 materials were characterized using Raman and *I*–*V* characteristic curve tests. Figure 2(a) shows the Raman spectra of the CIPS flakes at room temperature. Because of the anion ($P_2S_6^{4-}$) liberation, a peak at 102 cm^{-1} is easily observed. The presence of δ (S–P–P) and δ (S–P–S) modes leads to multiple Raman peaks of 140–290 cm^{-1}. The presence of the cations (Cu^{I}, In^{III}) leads to the appearance of a Raman peak at 316.5 cm^{-1}. The ν (P–P) mode results in a peak at 373.7 cm^{-1}.[38] Figure 2(b) shows the *I*–*V* characteristics of the CIPS flakes. The *I*–*V* curves were di-

vided into six parts at 0 V → 1 V → 0 V and 0 V → −1 V → 0 V, with multiple peaks appearing in the sweep voltage. The two-step 90° switch polarization reversal was responsible for these peaks, demonstrating the ferroelectric nature of CIPS flakes.[39] Figure 2(c) shows the Raman spectra of the MoS_2 flakes. The out-of-plane (E^1_{2g}) and in-plane resonance peaks (A_{1g}) of MoS_2 can be observed at 383.5 cm^{-1} and 406.6 cm^{-1}, respectively.[40] The distance between the two characteristic peaks is approximately 23.1 cm^{-1}. Referring to the previous data, this difference of approximately 23.1 cm^{-1} represents four layers of MoS_2 flakes.[41,42] Figure 2(d) tests the I_{DS}–V_G characteristics of the MoS_2 transistors. The transmission characteristics show typical n-type semiconductor characteristics under a sweep gate voltage from −33 V to 33 V.[43,44]

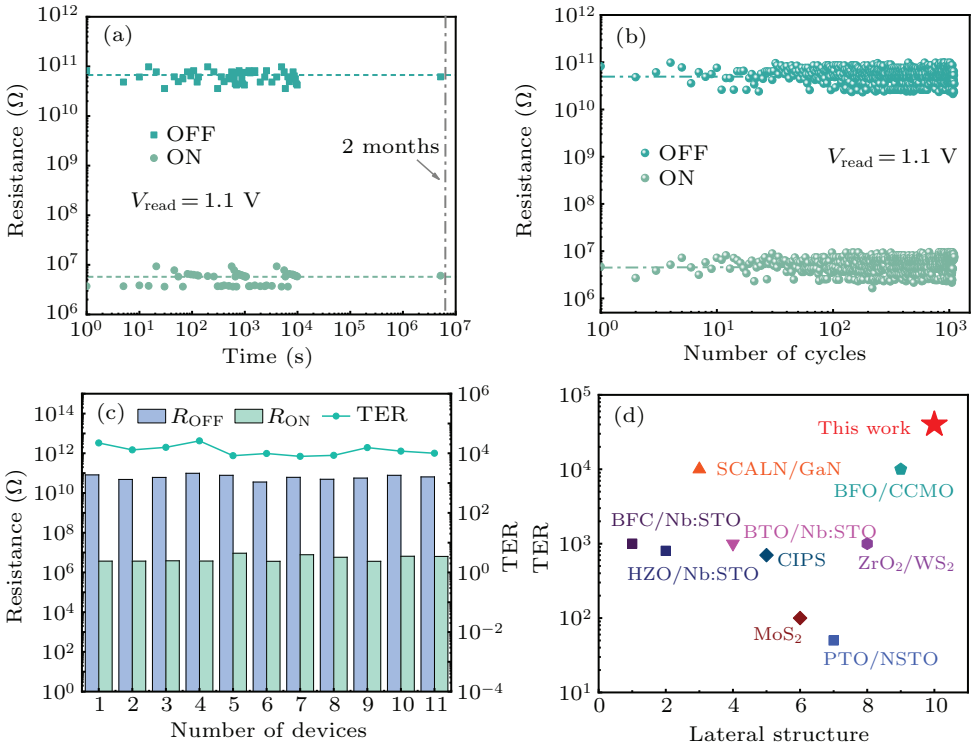


Fig. 3. (a) Data retention characteristics of the device in the ON and OFF states. (b) Endurance characteristics of the device. Experimental measurements were obtained for 1000 switching cycles. (c) Resistances (ON and OFF states) of the 11 different FTJ devices and the corresponding TERs. (d) TERs of the reported lateral structured devices.

Our proposed Au/CIPS/MoS_2/Au vdW FTJs with 11 nm CIPS and 2 nm MoS_2 (figure S3 shows material thickness) exhibited good reliability, such as long data retention, excellent endurance performance and uniformity. The electrical characteristics and properties were tested and analyzed and are shown in Fig. 3. Figure 3(a) shows the data retention properties at room temperature. The TER was stable at 1.4×10^4 after more than 2 months, which showed that the proposed device has a robust performance.[12,45] Figure 3(b) shows the endurance test of the FTJ over 1000 cycles. After 1000 cycles, the TER remained above 1.4×10^4, indicating good endurance of the device. Several devices were prepared and tested for different values of resistance and TER in the ON and OFF states, as shown in Fig. 3(c). The device exhibited good uniformity. The TER of the proposed vdW FTJ compared with that of the other lateral structured devices[46–54] is shown in Fig. 3(d). Our proposed vdW FTJ showed the highest TER for the lateral structured devices. The Au/CIPS/MoS_2/Au vdW FTJ demonstrated non-volatile switching and non-destructive readout reliability and is thus considered an ideal candidate for high-TER memory.[55]

The direct tunneling and Fowler–Nordheim tunnelling (FNT) mechanisms are the main transport mechanisms in our proposed Au/CIPS/MoS_2/Au vdW FTJ. There are three main possible transport mechanisms: direct tunnelling, FNT and thermionic emission.[56] The physical phenomenon of FNT is the same as that of direct tunnelling; however, at different voltage states, FNT tunnelling occurs at higher voltages.[24] To prove that the tunnelling mechanism of carriers is also independent of thermal emission, the I–V characteristics of the proposed Au/CIPS/MoS_2/Au vdW FTJ at different temperatures and the corresponding TER were obtained and are shown in Fig. S4. The current exhibited a weak change in the temperature range 250–340 K for the ON and OFF states, and the TER remained almost the same. According to the current density formula for the thermionic emission[57,58]

$$J_{\text{Schottky}} = A^* T^2 \exp\left[-\frac{q}{k_B T}\left(\varphi_B - \sqrt{\frac{qE}{4\pi\varepsilon_0\varepsilon_{\text{ifl}}}}\right)\right], \quad (6)$$

the thermal activation process of the thermionic emission mechanism led to strong temperature dependence ($J \propto T$). The

unchanged TER shows that the transport mechanism is independent of the thermionic emission. The *I*–*V* characteristic curve of the device under different voltages was fitted as shown in Fig. S5. It is known that if $\ln(I/V^2) \propto 1/V$ is satisfied FNT prevails,[59] and if $\ln(I/V^2) \propto \ln(1/V)$ is satisfied direct tunnelling plays a leading role. Both FNT and direct tunnelling can be observed in the fitting results.[60] By fitting the experimental data, it can be found that the primary tunnelling mechanism is direct tunneling under low voltage. As the voltage increases, FNT becomes dominant.

The proposed Au/CIPS/MoS_2/Au vdW FTJ also exhibited excellent photoresponsive properties, benefiting from the light absorption properties of the MoS_2 semiconductor. The Au/CIPS/MoS_2/Au vdW FTJ had a rather low current when the polarization direction of CIPS was downward (OFF state) (Fig. 1(c)). A low dark current has been found to be critical for high-performance photodetectors. To elaborate the performance mechanism when the device was laser-illuminated (449 nm laser), the energy band arrangements of the CIPS/MoS_2 heterojunction under different polarization states are shown in Fig. 4(a); the inset of Fig. 4(a) shows a schematic diagram of the device. The photogenerated electrons and holes are easily separated and collected to form photocurrents. When the polarization direction of CIPS is upward (ON state), the bending of the MoS_2 energy band at the interface changes from bottom to top. Due to the positive polarized charges accumulating at the interface, free electrons are attracted and free holes are repelled opposite to the current direction. The dark current is also larger, because of which the change in the photocurrent is insignificant in the ON state. When the polarization direction of CIPS is downward (OFF state), the energy band remains upward. Free electrons are repelled, and free holes are attracted due to the negatively polarized charges accumulating at the interface, the same as the current direction. At this time, the dark current is small, and the photocurrent easily increases under illumination. Therefore, the photocurrent can be mainly attributed to the contribution of photogenerated electrons under positive bias and the dark current is smaller, which improves the photoresponse behavior.

Figure 4(b) shows the hysteresis loops (V_{DS} was between −4 V and 4 V) of the generated photocurrents with different polarization states under 449 nm laser irradiation. Figure 4(c) shows the dependence of photocurrent as a function of light intensity (V_{DS} = 1.3 V). In the ON state, the magnitude of the current is almost constant. However, the photocurrent of this device in the OFF state strongly depends on the light intensity and increases with increase in light intensity. In the OFF state, the current of the device increases from 4×10^{-12} A to 1.2×10^{-10} A when light intensity increases from 0 to 0.57 mW·cm^{-2}; the value of I_{light}/I_{dark} is 30. A better linear relationship is obtained, demonstrating that the device has excellent photoresponsive performance in the OFF state.

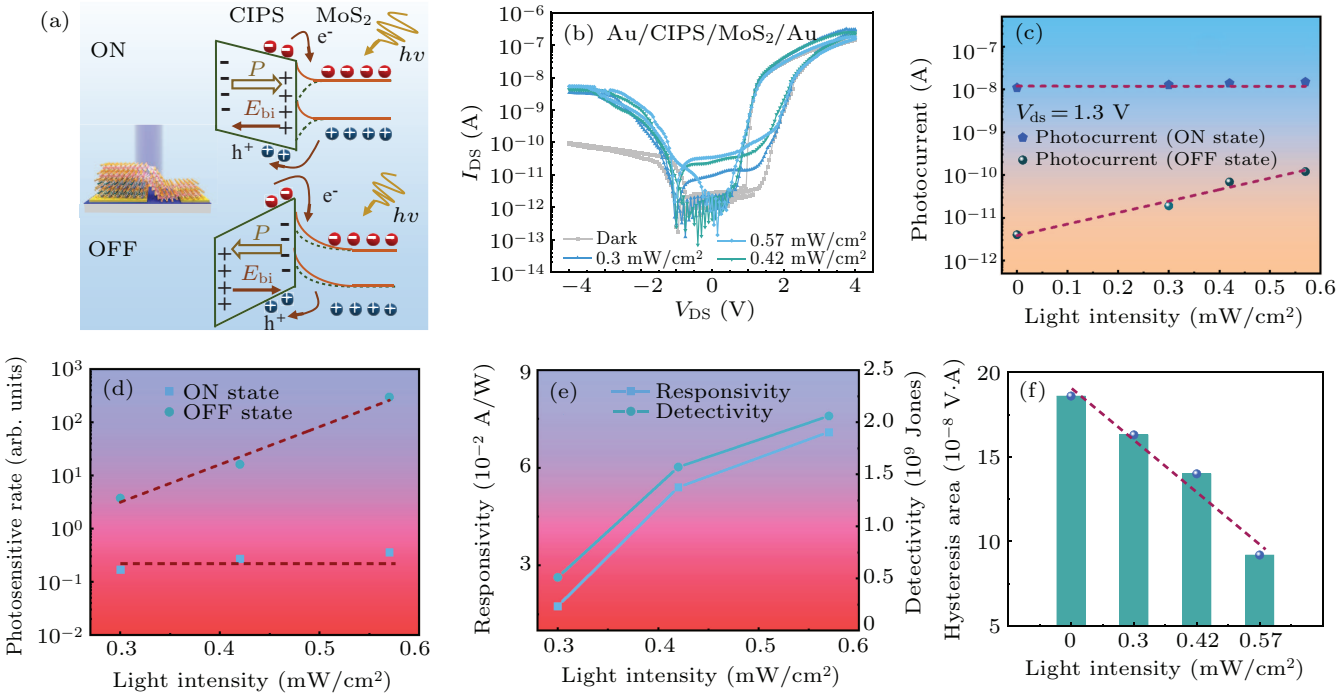


Fig. 4. (a) Band diagrams of the photodetector in the ON and OFF states; at V_{DS} = 1.3 V, the green dotted line is the energy band without light and the 0 V bias voltage, and the solid orange line is the energy band at 1.3 V bias voltage with a 449 nm laser. (b) Hysteresis loops under different light intensities for a 449 nm laser. (c) Photocurrent as a function of light intensity in the ON and OFF states. (d) Photosensitive rate as a function of the light intensity of the device in the ON and OFF states. (e) Responsivity and detectivity of the proposed Au/CIPS/MoS_2/Au vdW FTJ photodetector as a function of light intensity in the OFF state. (f) Hysteresis loop area as a function of light intensity.

The difference in the dark currents in the ON and OFF states is the main reason for the difference in the photoresponsive performance in the ON and OFF states. The dark current in the ON state is much higher than that in the OFF state. Light stimulation onto the device in the ON state cannot easily increase the current, because the dark current in the ON state is already very high. Light stimulation onto the device in the OFF state easily increases the current, benefiting from the very slow dark current in the OFF state. A new parameter of the photosensitive rate ($R_{\rm p}$) as a function of the light intensity is proposed here to analyze the effects of the ON and OFF states; the relationship is defined using

$$R_{\rm p} = \frac{I_{\rm light} - I_{\rm dark}}{I_{\rm dark}}, \tag{7}$$

where $I_{\rm light}$ is the light current and $I_{\rm dark}$ is the dark current. As shown in Fig. 4(d), the photosensitive rate in the OFF state to the light stimulation is much greater than that in the ON state.

Photoresponsivity (R_λ) and detectivity (D^*), which are important parameters for evaluating the ability to convert light signals into electrical signals,[61] were analyzed in the OFF state and are shown in Fig. 4(e). R_λ and D^* can be calculated as defined in Ref. [62]

$$R_\lambda = \frac{I_{\rm p}}{P} = \frac{I_{\rm light} - I_{\rm dark}}{P}, \tag{8}$$

$$D^* = \frac{R\sqrt{A}}{\sqrt{2eI_{\rm dark}}}, \tag{9}$$

where P is the light power, A is the photosensitive area and e is the electron charge. Values of $R_\lambda = 7.1 \times 10^{-2}$ A·W^{-1} and $D^* = 2.06 \times 10^9$ Jones were obtained in the OFF state. Our experiment shows excellent detector sensitivity in the OFF state.

Light stimulation can be used to modulate the ferroelectric properties, and the ferroelectric properties can yield a new type of photodetector with the new parameters. The new parameter of the hysteresis loop area as a function of light intensity was analyzed to obtain the relationship between the ferroelectric and photodetection properties, as shown in Fig. 4(f). The linear relationship provides a new characteristic for analyzing the photodetector.

The modulated relationship between ferroelectric TER and photosensitive rate $R_{\rm p}$ can be summarized by

$$\mathrm{TER}_{\rm dark} > \mathrm{TER}_{\rm light} \quad \text{and} \quad R_{\rm p,OFF} > R_{\rm p,ON}, \tag{10}$$

where the ferroelectric TER parameters under dark and light modulation are defined as

$$\mathrm{TER}_{\rm dark} = \frac{I_{\rm ON,dark}}{I_{\rm OFF,dark}}, \tag{11}$$

$$\mathrm{TER}_{\rm dark} = \frac{I_{\rm ON,light}}{I_{\rm OFF,light}}. \tag{12}$$

The photosensitive rates ($R_{\rm p}$) in the different ferroelectric ON and OFF states are defined as

$$R_{\rm p,OFF} = \frac{I_{\rm OFF,light} - I_{\rm OFF,dark}}{I_{\rm OFF,dark}}, \tag{13}$$

$$R_{\rm p,ON} = \frac{I_{\rm ON,light} - I_{\rm ON,dark}}{I_{\rm ON,dark}}. \tag{14}$$

It should be mentioned that a larger $\mathrm{TER}_{\rm dark}$ is the key point for obtaining two types of photodetection properties in a device. For our proposed ferroelectric CIPS/semiconductor MoS_2-based heterojunction, if $\mathrm{TER}_{\rm dark}$ is already large enough ($\sim 10^4$), the dark current in the ON state ($\sim 10^{-8}$ A) is already comparable to or of the same order as the current of the MoS_2 junction under light irradiation and the photoresponsive performance in the ON state is weak.

Schematic diagrams of the ferroelectric TER parameter in the ferroelectric/semiconductor heterojunction and the photoelectric $I_{\rm light/dark}$ parameter in the semiconductor junction are shown in Fig. 5. When the $\mathrm{TER}_{\rm ON/OFF}$ is the same order as $I_{\rm light/dark}$, the photoresponsive performance in the ON state is negligible. Two types of photodetection properties in one device can be obtained.

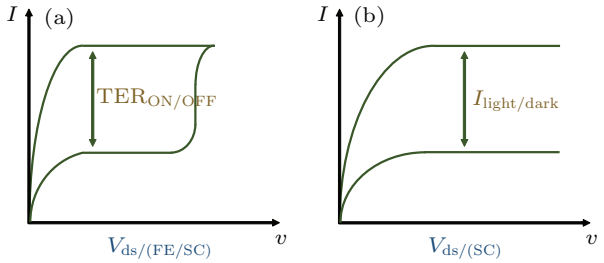


Fig. 5. Schematic diagrams of the ferroelectric TER and the photoelectric $I_{\rm light/dark}$ parameter in the ferroelectric/semiconductor heterojunction and semiconductor junction.

3. Conclusion

A combination of higher TER and excellent optoelectronic properties can be obtained by using a lateral structured Au/CIPS/MoS_2/Au vdW FTJ. CIPS polarization directions are easily modulated by an applied voltage to form the ON and OFF states. The barrier width and height at the CIPS–MoS_2 interface were modulated to improve the TER. The ferroelectric and photodetection properties modulated each other. The results show that the devices composed of 2D ferroelectric materials and 2D semiconductors exhibit excellent nonvolatile and photoresponsive performance, providing an excellent method for developing high-TER memristors or preparing new photodetectors.

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