

A non-quasi-static model for nanowire gate-all-around tunneling field-effect transistors

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A non-quasi-static model for nanowire gate-all-around tunneling field-effect transistors

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Nanowires with gate-all-around (GAA) structures are widely considered as the most promising candidate for 3-nm technology with the best ability of suppressing the short channel effects, and tunneling field effect transistors (TFETs) based on GAA structures also present improved performance. In this paper, a non-quasi-static (NQS) device model is developed for nanowire GAA TFETs. The model can predict the transient current and capacitance varying with operation frequency, which is beyond the ability of the quasi-static (QS) model published before. Excellent agreements between the model results and numerical simulations are obtained. Moreover, the NQS model is derived from the published QS model including the current–voltage (I–V) and capacitance–voltage (C–V) characteristics. Therefore, the NQS model is compatible with the QS model for giving comprehensive understanding of GAA TFETs and would be helpful for further study of TFET circuits based on nanowire GAA structure.

Keywords: tunneling field effect transistor, relaxation time approximation, non-quasi-static, non-quasi-static

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1. Introduction

Based on the mechanism of the band-to-band tunneling (BTBT), the tunneling field effect transistors (TFETs) can break the sub-threshold swing (SS) of 60 mV/dec which is the limitation for metal-oxide-semiconductor field-effect transistors (MOSFETs). Therefore the TFETs allow further scaling of supply voltage and are more suitable for low power applications.[1–4]

However, like MOSFETs, the TFETs also suffer from some detrimental non-ideal effects, such as the short channel effects (SCEs) and drain-induced barrier lowering (DIBLs).[5,6] To suppress these effects and boost the device performance, many innovation works have been carried out and turned out that the nanowire structure with the gate all around the channel body shows the highest gate control efficacy and strongest immunity to SCEs and DIBLs.[7] Therefore, the nanowire GAA TFETs have the better SS characteristics and on-state current compared with other devices.[6] At present, the GAA structure is widely considered as the most promising candidate for 3 nm technology and numerous experimental and theoretical works are carried out for nanowire GAA devices.[8]

Besides the device fabrication and simulation studies, a friendly predictive model applied in simulation program with integrated circuit emphasis (SPICE) is extremely significant for practical applications of TFETs. So far, there have been many models published for I–V and C–V performance of GAA TFETs.[9–23] While the models present good agreements of the model results with the numerical data, they are based on the quasi-static (QS) approach. That is to say, it is assumed that the charge redistribution time equals zero, and once the biases are applied, the channel charges achieve equilibrium state. This is obviously not the actual situation. It may be not a big problem to ignore the carrier redistribution time for slow-changing signals. However, for fast-changing signals, especially when the signal changing time is comparable to the carrier redistribution time, this assumption would result in erroneous results, such as over-estimated transient charges and current, unchanged capacitance with signal frequency and even convergent problems, which would be discussed in detail later.

In Ref. [24], small-signal parameters of the GAA TFETs with different gate lengths are extracted from the conventional non-quasi-static (NQS) model for an MOSFET, in which the charge redistribution time is considered. The Y-parameters modeled by circuit simulations are compared with the data from three-dimensional (3D) device simulations, and excellent agreements are obtained. Although this model is significant and may be practically useful for the GAA TFET circuit simulations, it is mainly empirical and the small-signal parameters must be re-extracted once the physical parameters or geometric dimensions of the device are changed. Furthermore, the model only considers the ac small-signal behavior but the

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transient analysis.

From the development of the MOSFET NQS model, an NQS model can be threshold-voltage-based,[25–27] inversion-charge-based,[28–30] or surface-potential-based.[31–33] In the process of model derivation, it is necessary to make a compromise among the model complexity, speed, and accuracy. For example, both the spline collocation method[32] and the channel segmentation[31] are accurate, and they are also significantly more complex. Despite not high accuracy, the popular simplified relaxation time approximation (RTA) method[25,33–37] using a characteristic time to approximately describe the redistribution process of the channel carriers can reduce execution time and improve convergence. Therefore, the RTA method is employed in this study to develop the NQS model for GAA TFETs.

In this paper, we propose a physics-based NQS model for GAA TFETs with the aid of the RTA method. This NQS model is validated with the numerical simulations and good agreements are obtained for both the transient and ac small-signal behavior. Moreover, the NQS model is developed from an SPICE friendly compact model which can be implemented into circuit simulator, and thus the proposed model is compatible with the QS model for giving comprehensive understanding of GAA TFETs.

2. Drawbacks of the QS model

Many QS models have been developed for GAA TFETs, and in our previous work we also proposed a compact model which can predict both the *I*–*V* and *C*–*V* characteristics.[23] Considering that the model is compatible with SPICE platform and can be implemented into circuit simulators, we take this model as an example to present the drawbacks of the QS approach. The studied GAA TFET and the simulation setup are the same as those in Ref. [23]. The Synopsys Sentaurus technology computer aided design (TCAD) tools are used to study the device performance and the dynamic nonlocal BTBT model is adopted for considering the arbitrary tunneling barrier with non-uniform electrical field. Considering the nanowire diameter in our work is 15 nm and relatively larger, the quantum confinement effect is ignored and thus the bulk Kane model is adopted to determine the BTBT probability. The parameters $A = 4 \times 10^{14}$ cm^{-3}·s^{-1} and $B = 1.9 \times 10^{7}$ V·cm^{-1} in Kane's model are used.[38–40] However, it should be noted that the device would transit from a 3D electron system to a one-dimensional electron system with the scaling of the nanowire diameter.[41] In this case, the quantum confinement must be considered[42,43] and the modified Kane model for lower-dimensional systems should be used.[44,45] Other models like the doping-dependent mobility, the high-field saturation effects, and Shockley–Read–Hall (SRH) recombination are also considered.

Figure 1 shows the device structure split as three regions, the source depletion region I, the channel depletion region Ⅱ and the drift-diffusion region Ⅲ. The device parameters and symbols are summarized in Table 1. Figure 2 presents the transient gate charges calculated with the QS model for gate bias varying for different rise time t_r. As indicated by the TCAD results, when the gate bias increases from $V_{GS} = 0.0$ V at $t = 10$ ps to $V_{GS} = 2.0$ V at $t = 10$ ps $+t_r$, the gate charges gradually increase from one equilibrium state to another new equilibrium state. Nevertheless, we should note that, at $t = 10$ ps $+t_r$ when the gate bias reaches 2.0 V and becomes unchanged later, the gate charges are still increasing and do not reach the new equilibrium state. Namely, it still needs some time for the gate charges to re-distribute to reach the new equilibrium state after the gate bias becomes unchanged. However, this re-distribution time is ignored in the QS model, which leads to over-estimated gate charges and early equilibrium state, as shown by the dashed line. This problem becomes more serious for faster signal with smaller $t_r = 2$ ps.

Table 1. Parameters and values used in the model development.

Symbol	Defination	Values	Units
L_g	channel length	5	nm
R_{wire}	nanowire radius	7.5	nm
W_G	gate metal work-function	4.2	eV
L_D	drain region length		
T_{ox}	gate oxide thickness	2	nm
ε_{ox}	gate oxide dielectric constant	22	
ε_{Si}	channel dielectric constant	11.7	
N_S	source doping density	1×10^{20}	cm^{-3}
N_C	channel doping density	1×10^{15}	cm^{-3}
N_D	drain doping density	5×10^{19}	cm^{-3}
E_g	energy band-gap of channel material	1.12	eV
χ	electronic affinity of channel material	4.09	eV
N_C	density of state of the conduction band	3.2×10^{19}	cm^{-3}
N_V	density of state of the valance band	1.8×10^{19}	cm^{-3}

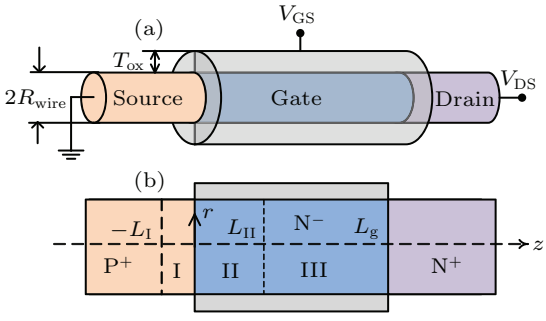


Fig. 1. (a) The 3D structure and (b) the corresponding schematic cross-section view of the nanowire GAA TFETs.

Due to the deviation of gate charges, the transient current is also over-estimated, especially for $t_r = 2$ ps, as presented in Fig. 2(b). As indicated by the TCAD results, the gate current gradually increases during the rise time of gate bias and then gradually decreases to zero after the gate bias becomes unchanged. Owing to the ignored charge re-distribution

time, transient current calculated by the QS model abruptly jumps to zero once the gate bias becomes unchanged. This sharp jump of the current to zero is obviously not physical and would cause convergent problems during the circuit-level simulations.

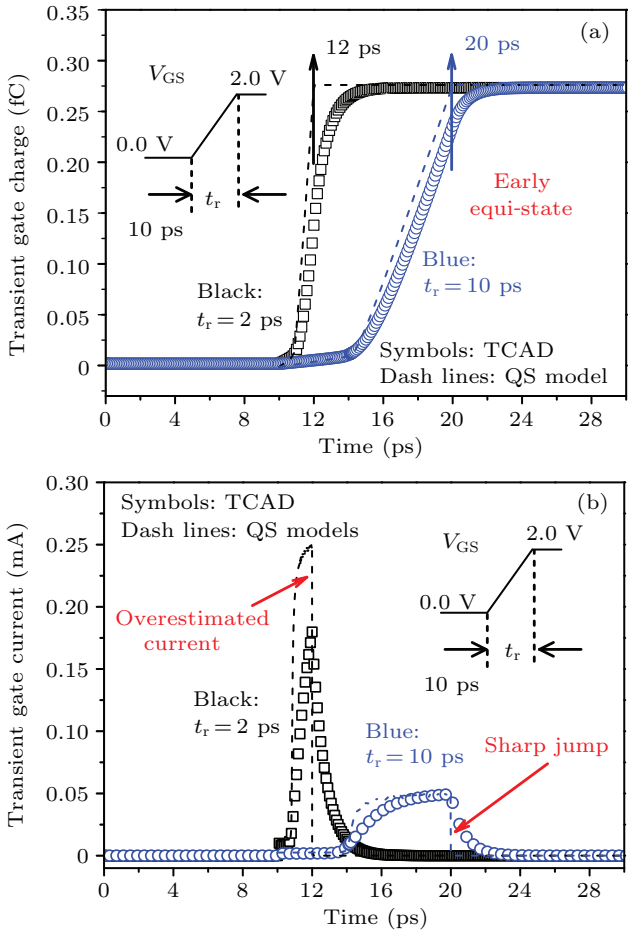


Fig. 2. (a) The transient gate charges and (b) gate current varied with the rise time of the gate bias t_r.

In addition, with increased small signal frequency, the signal cycle becomes shorter and not enough long for the carriers to respond. Therefore, the amount of responding carriers and the capacitance would decrease, which is also beyond the ability of the QS model.[46]

3. The NQS model derivation

3.1. Transient current

These shortcomings of the QS model are primarily owing to the hypothesis that the transient channel charges $Q_{ch}(t)$ always equal the equilibrium channel charges $Q_{cheq}(t)$ at any time, which is not the actual situation as discussed above. It is the assumption that causes the ignoring of the charge re-distribution time. To remedy this problem, we define the charges needed for $Q_{ch}(t)$ to reach $Q_{cheq}(t)$ as $Q_{def}(t)$:

$$Q_{def}(t) = Q_{cheq}(t) - Q_{ch}(t). \tag{1}$$

For constant bias, the device is in the equilibrium state and therefore the $Q_{def}(t)$ equals zero, just like that in the QS model. For varied bias, the $Q_{ch}(t)$ cannot keep up with the $Q_{cheq}(t)$, and the $Q_{def}(t)$ is nonzero. Actually the $Q_{def}(t)$ characterizes the degree of the $Q_{ch}(t)$ deviating from the $Q_{cheq}(t)$. For bias varying slowly, the $Q_{def}(t)$ is small and decays exponentially in the device body. Using the RTA approach, we can obtain the following expression:

$$\frac{dQ_{def}(t)}{dt} \approx -\frac{Q_{def}(t)}{\tau(t)} \tag{2}$$

in which $\tau(t) = RC$ describes how the $Q_{def}(t)$ decays with time in the device. R and C are resistance and capacitance, respectively. Both R and C are dependent on $Q_{ch}(t)$. The $Q_{def}(t)$ is small for bias varying slowly and $Q_{ch}(t)$ is approximately equal to $Q_{cheq}(t)$. Therefore, the C can be approximately considered as the low-frequency capacitance C_{low-f} for simplicity.

As for R, considering that the carrier tunneling from source is too few and can be neglected compared with that from drain, the R can be regarded as mainly distributed on the path through which the carriers transport from the drain into the channel. Thus the R can be expressed as

$$R = R_C + R_D, \tag{3}$$

where the R_C is the diffusion resistance for the region Ⅲ and the R_D is for the region drain. The conduction σ reads

$$\begin{cases} \sigma_{chan}(t) = Q_{cheq}(t)\,\mu_{e,chan}, \\ \sigma_{drain}(t) = Q_{drain}(t)\,\mu_{e,drain}, \end{cases} \tag{4}$$

in which $\mu_{e,chan}$ is the electron mobility in region Ⅲ and $\mu_{e,drain}$ is the electron mobility in drain region. The $Q_{cheq}(t)$ is dependent on the surface potential φ_S and the $Q_{drain}(t)$ is determined by the drain doping density N_D. Thus we can obtain

$$\begin{cases} Q_{cheq}(t) = (V_G - V_{FB} - \varphi_s)\,(2\varepsilon_{ox}/T_{ox,eff}R_{wire}), \\ Q_{drain}(t) = N_D q, \end{cases} \tag{5}$$

where q is the unit charge, V_{FB} is the flat-band voltage, R_{wire} is nanowire radius. $T_{ox,eff}$ is effective oxide thickness, and $T_{ox,eff} = R_{wire}\ln(1 + T_{ox}/R_{wire})$ with T_{ox} being the gate oxide thickness. For a wire with length L and cross-sectional area S, its resistance is $R = L/(\sigma S)$. Thus, from Eqs. (4) and (5) we can obtain the R_C and R_D as follows:

$$\begin{cases} R_C = \frac{L_G - L_{II}}{2\pi R \mu_{e,chan}(V_G - V_{FB} - \varphi_s)(\varepsilon_{ox}/T_{ox})}, \\ R_D = \frac{L_D}{(\pi R_{wire}^2)(N_D q \mu_{e,drain})}, \end{cases} \tag{6}$$

where L_G is the gate length, L_D is the drain length, and L_{II} is the region Ⅱ length. It should be noted that φ_S, L_{II}, V_{FB}, $Q_{cheq}(t)$, and C_{low-f} are all known paramters in the QS model.[23]

With $Q_{ch}(t)$ gradually approaching $Q_{cheq}(t)$, the $Q_{def}(t)$ gradually decays. Thus, the transient charging current $i(t)$ can be expressed as a function of $Q_{ch}(t)$ or $Q_{def}(t)$

$$i(t) = \frac{dQ_{ch}(t)}{dt} = -\frac{dQ_{def}(t)}{dt}. \tag{7}$$

Using Eqs. (2) and (7), we can obtain

$$i(t) = \frac{\mathrm{d}Q_{\mathrm{ch}}(t)}{\mathrm{d}t} \approx \frac{Q_{\mathrm{def}}(t)}{\tau(t)}. \tag{8}$$

Substituting Eq. (1) into Eq. (8) yields

$$\frac{\mathrm{d}Q_{\mathrm{def}}(t)}{\mathrm{d}t} + \frac{Q_{\mathrm{def}}(t)}{\tau(t)} - \frac{\mathrm{d}Q_{\mathrm{cheq}}(t)}{\mathrm{d}t} = 0. \tag{9}$$

The general solution to Eq. (9) can be expressed as

$$\begin{aligned} Q_{\mathrm{def}}(t) &= A\exp\left(-\frac{t}{\tau(t)}\right) + \exp\left(-\frac{t}{\tau(t)}\right) \\ &\times \int_{t_0}^{t} \exp\left(\frac{t}{\tau(t)}\right)\frac{\mathrm{d}Q_{\mathrm{cheq}}(t)}{\mathrm{d}t}\mathrm{d}t, \end{aligned} \tag{10}$$

where t_0 is the starting changing time of the applied bias. Thus $Q_{\mathrm{def}}(t_0) = 0$, with which we can obtain $A = 0$.

$$Q_{\mathrm{def}}(t) = \exp\left(-\frac{t}{\tau(t)}\right)\int_{t_0}^{t} \exp\left(\frac{t}{\tau(t)}\right)\frac{\mathrm{d}Q_{\mathrm{cheq}}(t)}{\mathrm{d}t}\mathrm{d}t. \tag{11}$$

The $Q_{\mathrm{def}}(t)$ can be expressed in the discretization form

$$\begin{cases} Q_{\mathrm{def}}(t) = G(t)\exp\left(-\frac{t}{\tau(t)}\right), \\ G(t) = \sum_{0}^{N-1} \exp\left(\frac{t_n}{\tau(t_n)}\right)\left(Q_{\mathrm{cheq}}(t_{n+1}) - Q_{\mathrm{cheq}}(t_n)\right), \\ t_n = t_0 + n\Delta t, \quad \Delta t = \frac{t-t_0}{N}. \end{cases} \tag{12}$$

The transient charges and current are exhibited in Figs. 3 and 4 for different changing ranges and rise times, respectively. It can be seen that the agreement between the model results and the numerical simulations is greatly improved compared to the QS model. Considering that the current is just the charges flowing per unit time, it is easy to understand that the larger bias changing range and smaller rise time lead to larger transient current in Figs. 3 and 4.

In Eq. (12), $\tau(t)$ and $Q_{\mathrm{cheq}}(t)$ are dependent on the gate bias, which leads to varied $G(t)$ during the bias rising stage. However, once the gate bias reaches constant after $t = 10\ \mathrm{ps} + t_{\mathrm{r}}$, $\tau(t)$, $Q_{\mathrm{cheq}}(t)$ and $G(t)$ also become unchanged. Thus the $Q_{\mathrm{def}}(t)$ and current start to exponentially decrease with constant τ, as shown in Figs. 3(b) and 4(b). This provides us a method to extract the relaxation time from the experimentally measured transient current.

In the equilibrium state, $Q_{\mathrm{ch}}(t) = Q_{\mathrm{cheq}}(t)$ and the NQS model becomes the QS model. The $Q_{\mathrm{ch}}(t)$ determines the channel conduction but would not influence the current which is dominated by the source tunneling process. However, in the non-equilibrium state, $Q_{\mathrm{ch}}(t)$ cannot keep up with $Q_{\mathrm{cheq}}(t)$ and deviates from $Q_{\mathrm{cheq}}(t)$. To gradually recover from $Q_{\mathrm{ch}}(t)$ to $Q_{\mathrm{cheq}}(t)$, the channel charges need to transport into or out the channel by source-side tunneling process and drain-side thermal injection. However, compared with the thermally injected charges from the drain, the source tunneling probability is too small and the tunneling charges are too few. The transient current is almost totally determined by the drain-side thermal injection. That is why the transient current is greater than the on-state tunneling current usually with the magnitude of μA for silicon-based devices.

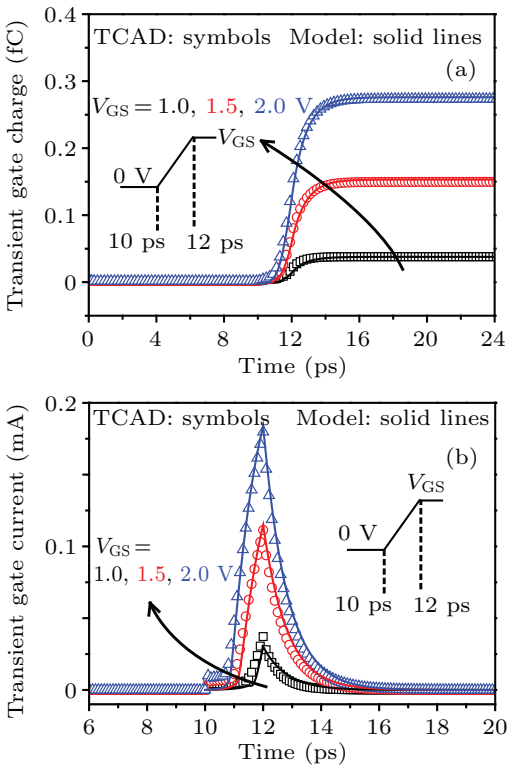


Fig. 3. The transient gate (a) charges and (b) current for changing gate bias from 0.0 V at $t = 10$ ps to V_{GS} at $t = 12$ ps.

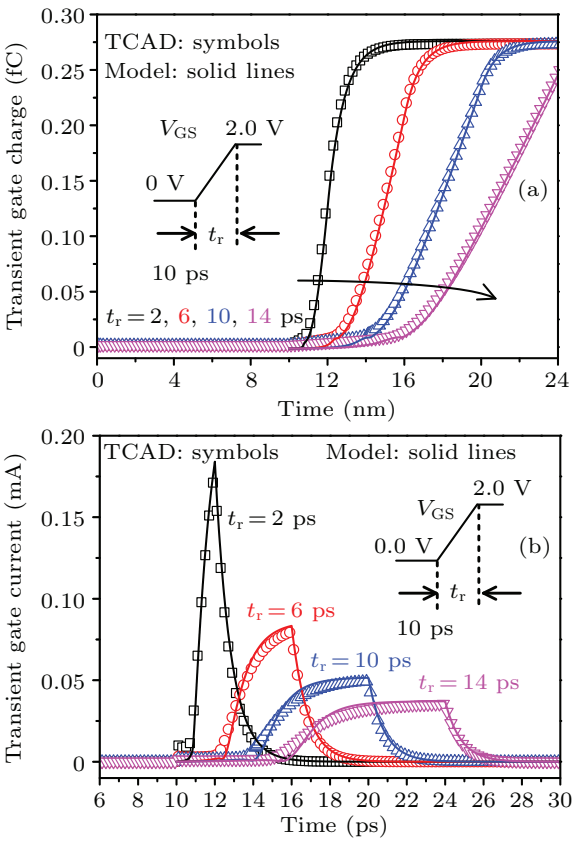


Fig. 4. The transient gate (a) charges and (b) current for changing gate bias from 0.0 V at $t = 10$ ps to 2.0 V with different rise time t_{r}.

3.2. High-frequency capacitance

Using Eqs. (1) and (8), we can reach

$$\frac{\mathrm{d}Q_{\mathrm{ch}}(t)}{\mathrm{d}t} \approx \frac{Q_{\mathrm{cheq}}(t) - Q_{\mathrm{ch}}(t)}{\tau}. \tag{13}$$

The capacitance as a function of signal frequency can be determined with Laplace transformation

$$\begin{cases} Q_{\mathrm{ch}}(\mathrm{j}\omega) = \frac{Q_{\mathrm{cheq}}}{1+\mathrm{j}\omega\tau}, \\ C_{\mathrm{gg}}(\mathrm{j}\omega) = \frac{C_{\mathrm{low-f}}}{1+\mathrm{j}\omega\tau}. \end{cases} \tag{14}$$

The variation of the capacitance at fixed biases is presented in Fig. 5 for different operation frequencies, and obviously good agreement of the model results and numerical data is presented. Considering that the NQS model is developed from the QS model, the accuracy of the NQS model is also dependent on the QS model. The deviation for low frequency smaller than about 10^9 Hz mainly results from the inaccuracy of the QS model. Due to the fact that the QS model error for $V_{\mathrm{GS}} = 2.0$ V is smaller than that for $V_{\mathrm{GS}} = 1.0$ V, the capacitance in Fig. 5 for $V_{\mathrm{GS}} = 2.0$ V fits better with the TCAD result than that for $V_{\mathrm{GS}} = 1.0$ V. Actually both the errors of the RTA method and the QS model determine the accuracy of the NQS model. In comparison, the QS model is more important. In fact, the potential along the source/channel interface is not constant and the source depletion width is actually varied with r. However, this is ignored and the source depletion region is taken as a regular cylinder for simplicity in the QS model, resulting in deviation of the terminal charges and capacitance. Thus a more realistic shape assumption of the source depletion region would be greatly helpful to improve the accuracy of the QS and NQS model.

We can also see from Fig. 5 that the capacitance decreases with operation frequency because the carriers responding are reduced with shorter signal cycle. It is should be noted that the decreasing rate of the capacitance with operation frequency varies with bias. Owing to the larger τ cased by relatively larger $C_{\mathrm{low-f}}$ for $V_{\mathrm{GS}} = 2.0$ V, the capacitance at $V_{\mathrm{GS}} = 2.0$ V reduces faster than that at $V_{\mathrm{GS}} = 1.0$ V

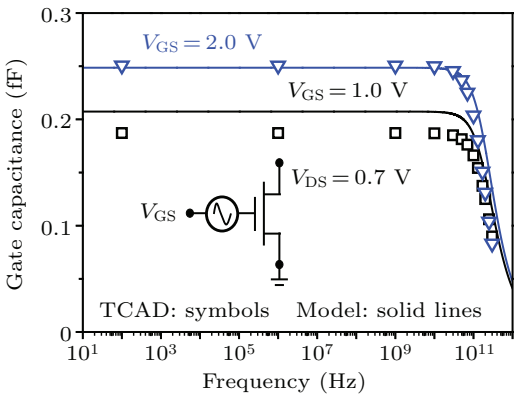


Fig. 5. The gate capacitance versus the operation frequency.

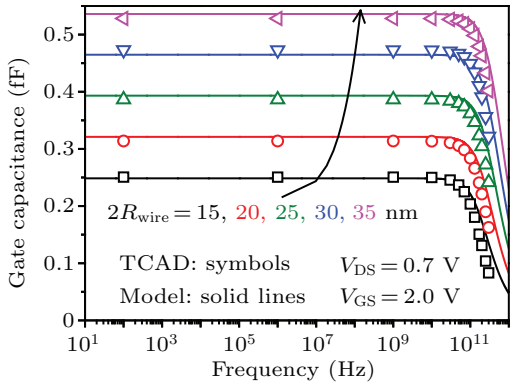


Fig. 6. The gate capacitance versus R_{wire}.

The effects of the nanowire diameter ($2R_{\mathrm{wire}}$) are also studied, as shown in Fig. 6. The larger the diameter is, the more the carriers accumulated in the channel body and responding to the gate bias are, thus the larger the $C_{\mathrm{low-f}}$ is. The larger $C_{\mathrm{low-f}}$ further results in larger τ and faster decreasing rate of the capacitance with operation frequency as shown in Fig. 6. Considering that the scaling of the nanowire diameter can greatly improve the device performance by reducing the defects at the tunneling interface, a very small nanowire diameter is desired[47–49] and the diameter of many reported excellent nanowire GAA TFETs is also below 35 nm.[47–52] Therefore, the proposed NQS model is effective for the desired diameter range and the diameter larger than 35 nm is not preseted in Fig. 6.

Last but not least, many works on the fabrication of nanowire GAA TFETs are reported.[47,53] However, there is no experimental report on the transient current and high-frequency capacitance so far. Therefore, we do not present the comparison with the experimental data. The modeled data shows good agreement with the numerical results, indicating that the NQS model would be helpful for further investigation of the nanowire GAA TFETs.

4. Conclusion

In this paper, an NQS model based on the RTA technique is developed for the first time for nanowire GAA TFETs. The model can predict the transient current and capacitance varying with operation frequency. Good agreements of the model results and numerical data are obtained. Moreover, the NQS model is derived from the previously proposed QS model including I–V and C–V characteristics. Therefore, the NQS model is compatible with the QS model for giving comprehensive understanding of GAA TFETs and would be helpful for further study of TFET circuits based on nanowire GAA structures.

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