A SiC asymmetric cell trench MOSFET with a split gate and integrated p$^+$-poly Si/SiC heterojunction freewheeling diode

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A new SiC asymmetric cell trench metal–oxide–semiconductor field effect transistor (MOSFET) with a split gate (SG) and integrated p$^+$-poly Si/SiC heterojunction freewheeling diode (SGHJD-TMOS) is investigated in this article. The SG structure of the SGHJD-TMOS structure can effectively reduce the gate-drain capacitance and reduce the high gate-oxide electric field. The integrated p$^+$-poly Si/SiC heterojunction freewheeling diode substantially improves body diode characteristics and reduces switching losses without degrading the static characteristics of the device. Numerical analysis results show that, compared with the conventional asymmetric cell trench MOSFET (CA-TMOS), the high-frequency figure of merit (HF-FOM, $R_{on,sp} \times Q_{gd,sp}$) is reduced by 92.5%, and the gate-oxide electric field is reduced by 75%. In addition, the forward conduction voltage drop (V_F) and gate-drain charge (Q_{gd}) are reduced from 2.90 V and 63.5 μC/cm^2 in the CA-TMOS to 1.80 V and 26.1 μC/cm^2 in the SGHJD-TMOS, respectively. Compared with the CA-TMOS, the turn-on loss (E_{on}) and turn-off loss (E_{off}) of the SGHJD-TMOS are reduced by 21.1% and 12.2%, respectively.

Keywords: split gate (SG), heterojunction freewheeling diode (HJD), SiC asymmetric cell trench MOSFET, turn-on loss, turn-off loss

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1. Introduction

Silicon carbide (SiC) power metal–oxide–semiconductor field effect transistor (MOSFET) has the advantages of high breakdown voltage (BV) because of its PN junction, low specific on-resistance ($R_{on,sp}$), large thermal conductivity, fast transformational speed, anti-irradiation, and so on.[1–10] The SiC MOSFET can meet the strict requirements of advanced power electronics applications. It is considered to be one of the most capable power devices, which has been rapidly applied and developed in high-temperature and high-pressure solar power regulators, motor driven cars, rail transport vehicles and aerial vehicles.

SiC trench gate MOSFETs have a lower $R_{on,sp}$ and demonstrate better device performance due to cell area and miss three terminal active device resistors with amplification functions compared to SiC planar gate MOSFETs. However, the conventional SiC trench gate MOSFET has high electric fields at the bottom corner of the gate trench. With the SiC trench gate MOSFET, 3.0 MV/cm is currently used as the largest electric field of the gate-oxide layer. When the largest electric field of the gate-oxide layer surpasses 3 MV/cm, the device will reach the avalanche breakdown voltage. To relieve the high electric field in the gate-oxide layer, in recent years, several novel structures have been reported to address this problem.[11–18] Kagawa *et al.*[11] reported a gate bottom p-well trench MOSFET. Song *et al.*[12] put forward a trenched MOSFET construction with an L-shaped gate, which could be used to reduce the electric field at the sole angle of the trench. Seok *et al.*[13] reported a paired p-base construction, which can prevent gate oxides from entering and prevent congestion in the electric field. However, these novel structures introduce JFET regions and increase specific on-resistance. Thus, an n-type current diffusion layer with a relatively large doping concentration is squeezed between the p-base and n-drift region, and a p-type region is wrapped by it. The current will promote the dispersion from the MOS channel to the drift region, and the JEFT effect will be attenuated, which is caused by the p-well region.

The double-trench structure (DT-MOS) with a p-type region beneath the source trench is suggested to shield the field near the gate bottom.[18] The DT-MOS achieves a low $R_{on,sp}$ and alleviates the electric field crowding in the gate trench oxide layer. However, it has a large gate–drain capacitance (C_{gd}), contributed by the bottom of the gate trench. In recent years, Infineon's MeV ion-implanted asymmetric cell trench MOSFETs, such as the conventional asymmetric cell trench MOSFET (CA-TMOS)[19] and asymmetric cell structure tilt implanted 4H-SiC trench MOSFET,[20] have been proposed.

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A parasitic PiN bipolar diode is formed in the trench MOSFET. When working as a freewheeling diode in power electronic modules or systems, such as DC–AC converters, the reverse recovery charge is so redundant that the power loss of the trench MOSFETs is increased and the power converting efficiency is reduced. The integrated freewheeling diode (FWD) concept removes the extrinsic FWD, reducing as far as possible the role of parasitic interconnections. Several studies have reported the integration of junction barrier Schottky diodes in SiC power MOSFETs.[21–23] Han *et al.*[21] reported a 4H-SiC trench MOSFET integrated with a mesa-side wall SBD. Jiang *et al.*[22] reported a splitgate (SG) MOSFET, which only has a half-plane MOSFET element. Wei *et al.*[23] reported a birtratal superknot Schottky MOSFET. Furthermore, the combinative Schottky barrier diodes (SBD) mean that a MOSFET converts electricity into light over a remarkable area of the chip and adds the valid $R_{on,sp}$. However, it is essential to control the temperature to form the satisfying Schottky junction to trade off the leakage current and breakover voltage of the body diode. Moreover, the formation of SBD diodes on the sidewalls of the trenches brings with it difficulties in real fabrications.

Heterojunction diodes (HJD) are formed between polysilicon and SiC, which provide convenient conditions for device selection. Some researchers embed heterojunction diodes in power devices to improve the electrical performance of the devices.[24–29] Yu *et al.*[24] reported a novel SiC power MOSFET structure. Yoon[25] proposed a SiC MOSFET insted heterojunction diode, which provided some protection against the electric field. Yang *et al.*[26] proposed a SiC power gate trench MOSFET formed on the basis of heterojunctions. These proposed devices demonstrated reverse recovery characteristics.

In this article, an asymmetric cell SiC gate trench MOSET with an SG structure and p^+-poly Si/SiC HJD was studied for the first time. The SG structure of the SGHJD-TMOS structure can effectively reduce the gate–drain capacitance and reduce the high gate-oxide electric field. Moreover, the integrated p^+-poly Si/SiC HJD substantially improves body diode characteristics and reduces switching losses without degrading the static characteristics of the device and taking up the extra chip area.

2. Device structure and mechanism

The cross-sections of the CA-TMOS without the spilt gate and p^+-poly Si/SiC HJD are shown in Fig. 1(a).[30,31] Figure 1(b) shows a schematic cross-section view of the improved SGHJD-TMOS. To facilitate the comparison between the CA-TMOS and SGHJD-TMOS, except for the parameters of the spilt gate and heterojunction freewheeling diode, other configurable factors are consistent with the CA-TMOS. The main structural arguments of the two structures are shown in Table 1.

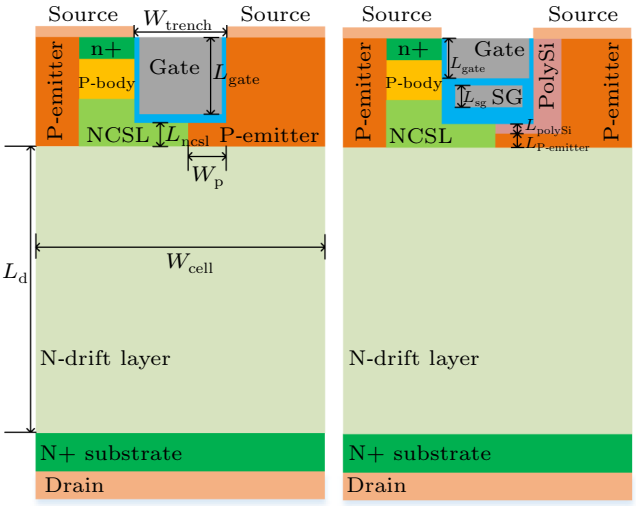


Fig. 1. Schematic cross sections of the two structures: (a) CA-TMOS and (b) SGHJD-TMOS.

The main features of the novel SGHJD-TMOS have an SG connected to the source and a p^+-poly Si/SiC heterojunction shielded region. An SG connected to the source in the gate trench decouples the drain–gate interaction. As a result, the C_{gd} and gate–drain charges (Q_{gd}) are significantly reduced, resulting in higher switching speed and lower switching loss. The p^+-poly Si/SiC heterojunction shielded region wraps the gate trench. It makes sure that the p^+-poly Si/SiC heterojunction shielded region has a strong shielding effect on the gate trench. At the same time, the p^+-poly Si/SiC heterojunction diode has the same unipolar function as the SBD. The p^+-poly Si/SiC heterojunction diode has a low forward-conduction voltage drop (V_F) and, unlike the SBD, the p^+-poly Si/SiC heterojunction diode has no charge barrier drop.

Figure 2 illustrates a feasible manufacturing course flow for the SGHJD-TMOS construction. An n-type drift layer was grown on a SiC n+ substrate. Then, the NCSL layer grows along the outer layer of the drift layer, and the p-emitter region is formed by ion implantation on the left and right sides of the NCSL layer, which is shown in Fig. 2(a). The formation of the p^+-poly Si is achieved by ion implantation. Thus, the p^+-poly Si/SiC heterojunction shielded area takes shape, which should look like Fig. 2(b). Similar to the CA-TMOS, the p-body and n+ source are formed as an extensional growth on the NCSL layer, as shown in Fig. 2(c). The SG is formed after corroding the sluice trench, as shown in Fig. 2(d). A gate and an insulating dielectric layer are formed, as shown in Fig. 2(e). Forming an ohmic metal layer, it is divided into front and back sides. It then forms a metal layer, which sits on top, as shown in Fig. 2(f).

Table 1. Parameters of the apparatus in simulations.

Major parameter	CA-TMOS	SGHJD-TMOS
Gate trench depth (L_{gate})	1.1 μm	0.75 μm
N-drift layer thickness (L_d)	12.0 μm	12.0 μm
Gate-oxide thickness	50 nm	50 nm
P-emitter region width under trench (W_p)	0.8 μm	0.8 μm
NCSL thickness under trench (L_{ncsl})	0.4 μm	0.4 μm
Split-gate thickness (L_{sg})	–	0.25 μm
p^+-poly Si shielded region thickness under trench (L_{polysi})	–	0.3 μm
p-emitter shielded region thickness under trench ($L_{p\text{-}emitter}$)	0.4 μm	0.1 μm
Cell width (W_{cell})	2.50 μm	2.50 μm
Trench width (W_{trench})	1.0 μm	1.0 μm
P-body region concentration	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}
N-drift layer concentration (N_d)	8×10^{15} cm^{-3}	8×10^{15} cm^{-3}
NCSL concentration (N_{ncsl})	2×10^{16} cm^{-3}	2×10^{16} cm^{-3}

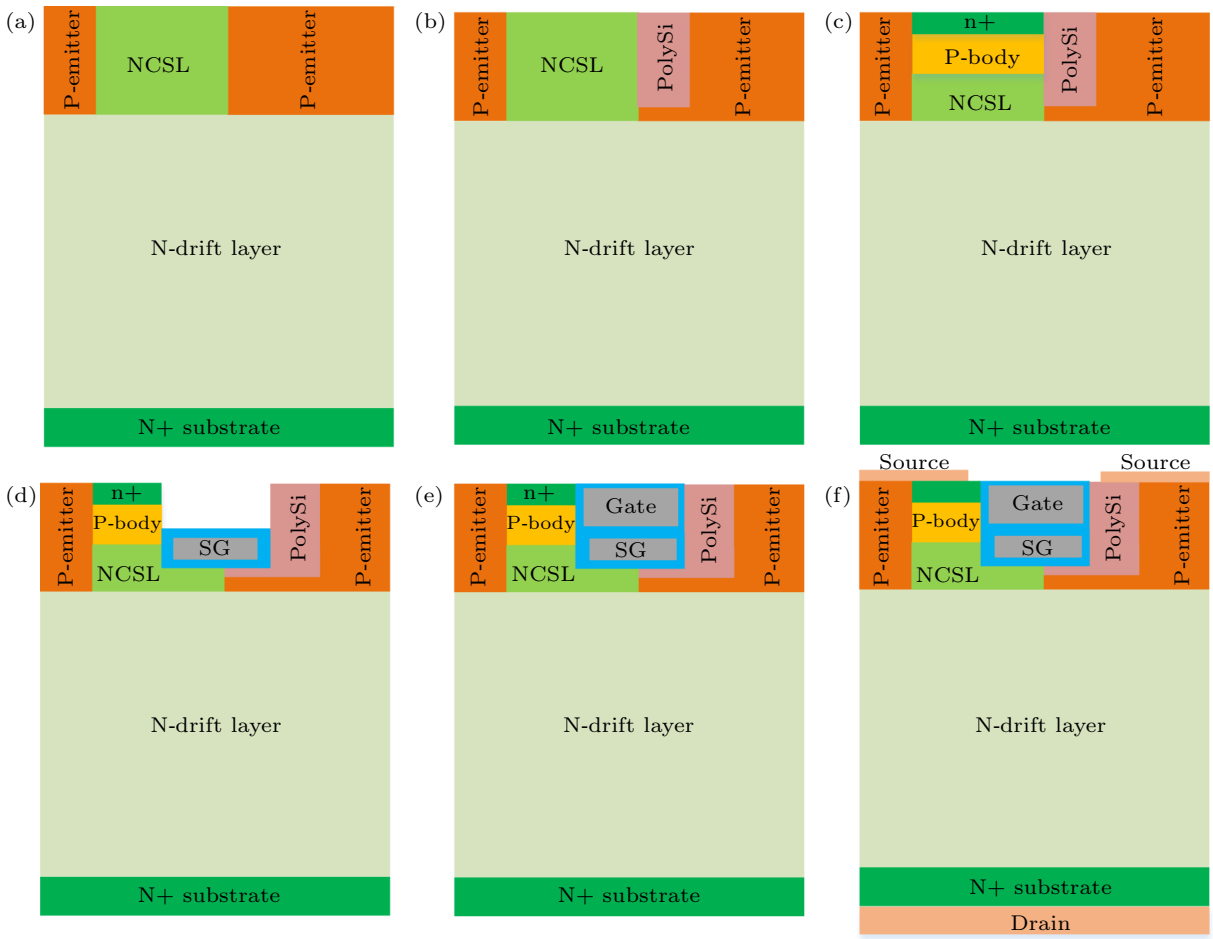


Fig. 2. The feasible manufacturing process description.

3. Results and discussion

The static and dynamic characteristics of the CA-TMOS and SGHJD-TMOS were simulated by utilizing Silvaco TCAD simulations.[32] Several models were utilized in this article. These models include mobility models that consider the dependencies of the carrier concentration and electric field. The bandgap reduction model is essential for the presence of heavily doped regions. The Shockley–Read–Hall (SRH), Auger model, and impact SELB models were also adopted. The SRH and the Auger models are recombination models, and the impact SELB is a Selberherr model that is applicable in most circumstances.

The static and dynamic characteristics of the CA-TMOS and SGHJD-TMOS were simulated in this section. Before the discussion and analysis, the optimization work of the SGHJD-TMOS structure must be carried out. For the SGHJD-TMOS structure, the different W_p of the p^+-poly Si/SiC heterojunction shielded region has a significant effect on the BV and

$R_{on,sp}$. Then, the different W_p of the p^+-poly Si/SiC heterojunction shielded region were simulated, as shown in Fig. 3. It can be seen that as the W_p increases from 0.2 μm to 1.0 μm, the BV increases significantly in the SGHJD-TMOS structure due to the enhanced shielding effect provided by the p^+-poly Si/SiC heterojunction shielded region. However, the $R_{on,sp}$ increases sharply after the W_p larger than 0.8 μm due to the increased JFET effect. Figure 4 shows the Baliga figure of merit (BFOM, $BV^2/R_{on,sp}$) values under different W_p. As can be seen from Fig. 4, the most suitable W_p was 0.8 μm.

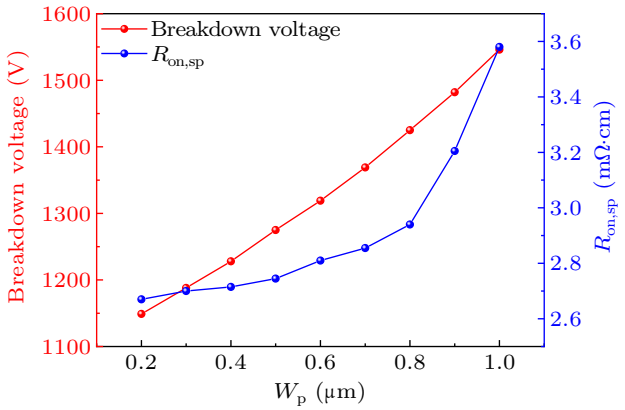


Fig. 3. BV and $R_{on,sp}$ of the SGHJD-TMOS structure for different W_p.

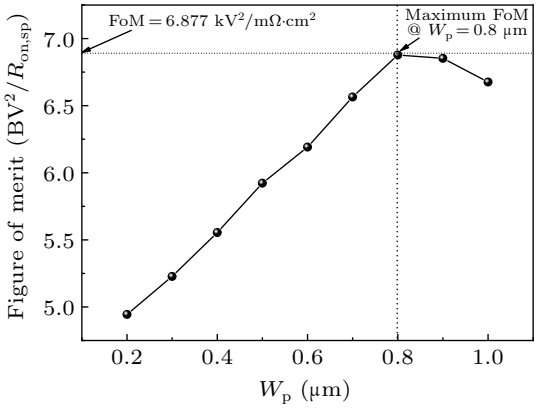


Fig. 4. Baliga figure of merit (BFOM, $BV^2/R_{on,sp}$) under different W_p.

To better reflect the effects of the L_{polysi} and $L_{p\text{-emitter}}$ on the BV, $R_{on,sp}$ and BFOM of the SGHJD-TMOS structure, the effects of TCAD simulation on the BV, $R_{on,sp}$, and BFOM of the SGHJD-TMOS structure, by changing the ratio of the L_{polysi} to $L_{p\text{-emitter}}$ values, was simulated, as shown in Fig. 5. It can be seen that with the increasing L_{polysi} to $L_{p\text{-emitter}}$ ratio, the BV of the SGHJD-TMOS was stable at first, and then gradually decreased. This is mainly because when the $L_{polysi}/L_{p\text{-emitter}}$ are low, no tunneling occurs to protect the poly Si region due to the thick p-emitter region, and the BV is mainly determined by the p-emitter region. However, when the L_{polysi} to $L_{p\text{-emitter}}$ ratio reached 3, the thickness of the p-emitter region gradually decreased and the poly Si region could not be protected effectively, resulting in a breakdown at the poly Si edge and a lower BV. In addition, it can be seen from Fig. 5 that the $R_{on,sp}$ of the SGHJD-TMOS decrease with the gradual increase of the L_{polysi} to $L_{p\text{-emitter}}$ ratio. This is mainly because the contact area between the poly Si region and N-type drift region increases with the increasing L_{polysi} to $L_{p\text{-emitter}}$ ratio and the space charge area generated by the p^+-poly Si/SiC shield in the N-type drift region decreases gradually. This reduces the JFET resistance between P-body and p^+-poly Si/SiC shielding, resulting in a gradual reduction in the $R_{on,sp}$. Finally, the BFOM of the SGHJD-TMOS structure is maximized when the L_{polysi} is 0.3 μm and the $L_{p\text{-emitter}}$ is 0.1 μm.

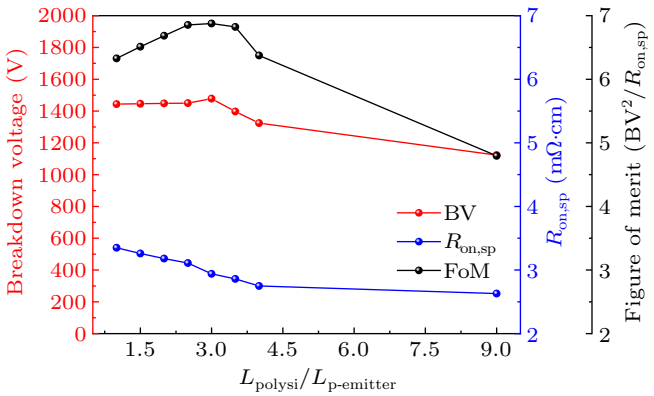


Fig. 5. Baliga figure of merit (BFOM, $BV^2/R_{on,sp}$) under different $L_{polysi}/L_{p\text{-emitter}}$.

3.1. On-state characteristics

The forward and reverse conduction *I*–*V* distinctions of the CA-TMOS and SGHJD-TMOS at V_{gs} = 16 V and V_{gs} = 0 V are shown in Fig. 6. As we know, the split-gate structure has a certain influence on specific on-resistance. However, as seen in Fig. 6, the ahead of schedule conduction *I*–*V* distinctions of the two constructions are almost the same. It also can be seen that the heterojunction diode was integrated with the improved structure, making it belong to a lower turn-on voltage. Thus, the V_F for the diode of the CA-TMOS is 2.9 V, while the SGHJD-TMOS structure is only 1.8 V at the empty present thickness of −150 A/cm^2.

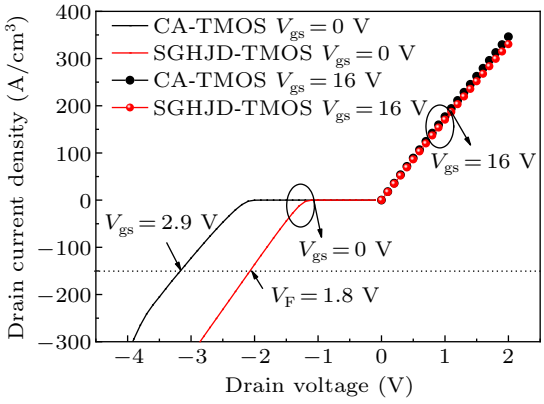


Fig. 6. The *I*–*V* characteristics of forward and reverse conduction for the CA-TMOS and SGHJD-TMOS at V_{gs} = 16 V and V_{gs} = 0 V.

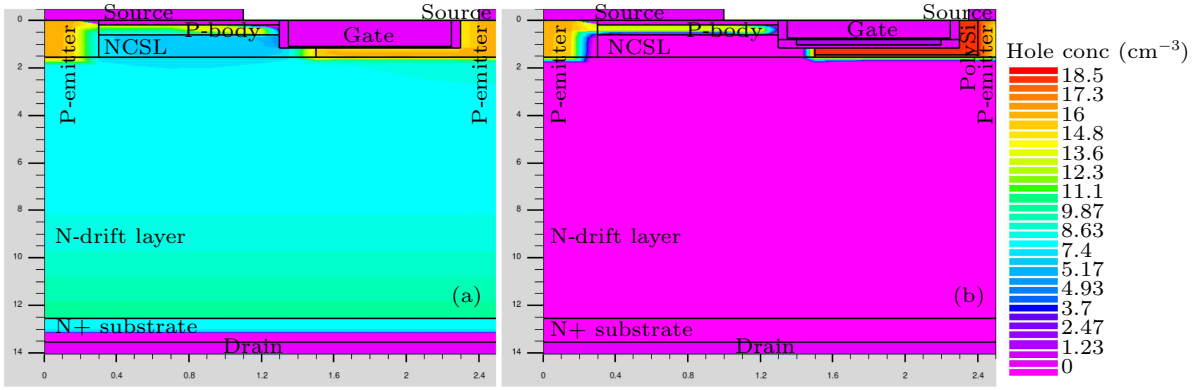


Fig. 7. The hole concentration distribution of (a) the CA-TMOS construction and (b) the SGHJD-TMOS construction at the drain current density of -150 A/cm^2.

Conventional SiC power diodes are always applied as free-rotating diodes in DC–DC circuit applications. Figure 7 shows the hole-concentration distribution of the CA-TMOS and SGHJD-TMOS at the drain current density of -150 A/cm^2. As seen in Fig. 7, the hole concentration of the SGHJD-TMOS structure is lower than the CA-TMOS structure at the drift region. The compared results show that the heterojunction diode successfully bypasses the conduction of the PiN body diode. A large number of holes are injected into the drift region in the CA-TMOS, while there are few holes injected into the drift in the SGHJD-TMOS structure. Therefore, the SGHJD-TMOS structure has a better low V_F in the diode conduction mode.

3.2. Off-state characteristics

The breakdown voltage performance curves for the CA-TMOS structure and SGHJD-TMOS are displayed in Fig. 8. The improved SGHJD-TMOS structure, as shown in Fig. 8, has a slightly higher BV than the CA-TMOS structure. For the SGHJD-TMOS structure and the CA-TMOS, the BV values are 1478 V and 1402 V, respectively. At the same time, the corresponding electric field distributions of the two structures are shown in Figs. 9(a) and 9(b). It can be seen that, although the two devices have comparable BVs, the electric field of the CA-TMOS is much higher than that of the SGHJD-TMOS. The electric field at the BV is 2.8 MV/cm and 1.6 MV/cm for the SGHJD-TMOS and CA-TMOS, respectively. When considering good long-time reliability, the higher electric field at the BV for the CA-TMOS will induce gate-oxide breakdown or degradation. Due to the fact that the SG structure with the thicker gate-oxide layer at the bottom in the SGHJD-TMOS reduces the high electric field at the trench corner, the limiting factor of the breakdown is shifted from the gate-oxide breakdown for the CA-TMOS to the avalanche breakdown for the SGHJD-TMOS. As a result, the above results demonstrate that the improved SGHJD-TMOS structure exhibits improved static performance.

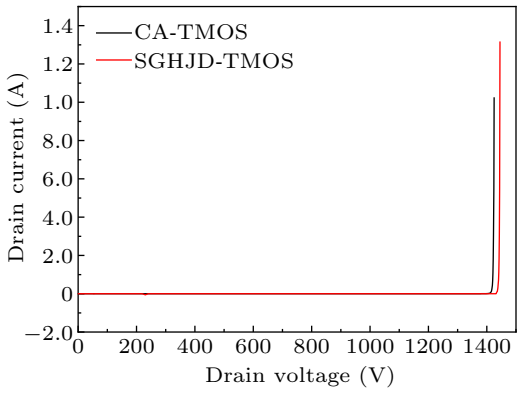


Fig. 8. Breakdown voltage characteristic curves of the CA-TMOS and SGHJD-TMOS.

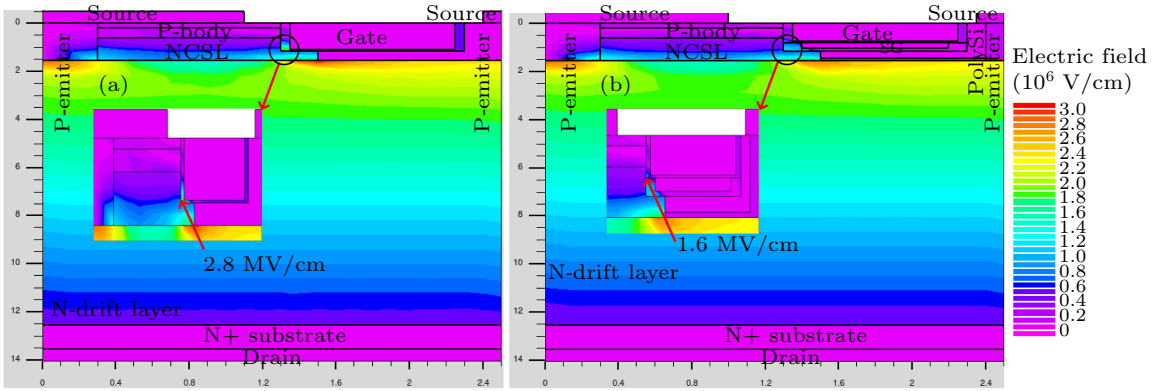


Fig. 9. Distributions of the electric field at the breakdown voltages: (a) the CA-TMOS, and (b) the SGHJD-TMOS.

3.3. Reverse transfer capacitance and gate charge characteristics

Figure 10 shows the typical C_{gd}, gate–source capacitance (C_{gs}), and drain–source capacitance (C_{ds}) of the SGHJD-TMOS and CA-TMOS at $f = 1$ MHz. As seen in Fig. 10, the C_{gd}, C_{gs}, and C_{ds} of the SGHJD-TMOS are smaller than those of the CA-TMOS. The decrease in gate depth and the decoupling of the gate and drain interaction result in a significant decrease in C_{gd} and C_{gs} due to the SG structure of the SGHJD-TMOS. With the much smaller C_{gd}, the SGHJD-TMOS demonstrates a superior high-frequency figure of merit.

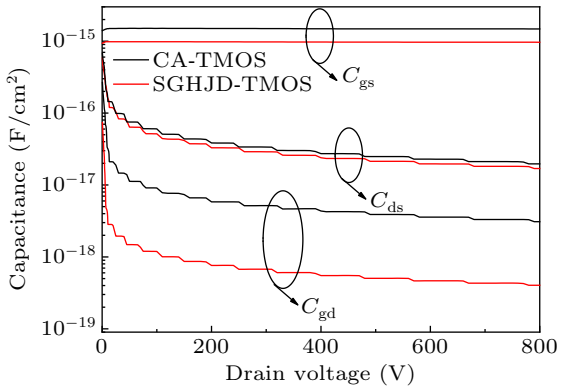


Fig. 10. The C_{gd}, C_{gs}, and C_{ds} curves of the CA-TMOS and SGHJD-TMOS.

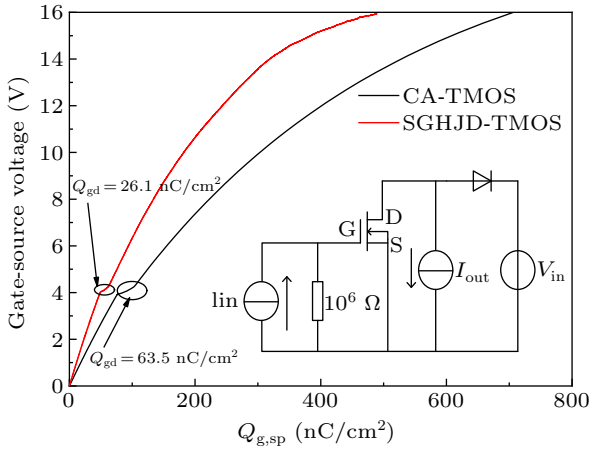


Fig. 11. The gate–charge characteristic curves of the CA-TMOS and SGHJD-TMOS.

The gate–charge characteristics of the CA-TMOS and SGHJD-TMOS are shown in Fig. 11. The test circuit used in the TCAD simulation is in the lower right corner of Fig. 11. As seen in Fig. 11, the SGHJD-TMOS structure exhibits a smaller Q_{gd}. Compared with 63.5 nC/cm^2 for the CA-TMOS, the Q_{gd} for the SGHJD-TMOS is only 26.1 nC/cm^2. The Q_{gd} of the SGHJD-TMOS is smaller than 143% of the CA-TMOS due to the fact that the p$^+$-poly Si/SiC HJD and SG structure splits the gate and reduces the gate–drain overlap area. The high-frequency figure of merit (HF-FOM, $R_{on,sp} \times Q_{gd,sp}$) is usually an effective criterion that is used to evaluate the performance of SiC power MOSFET devices in high-frequency switching applications. From TCAD simulation calculation, the HF-FOM of the CA-TMOS structure is 184.7 mΩ·nC. However, the SGHJD-TMOS structure has a better HF-FOM with a value of 76.7 mΩ·nC, which decreases by 140.8% compared with the CA-TMOS structure.

3.4. Dynamic characteristics

To illustrate the dynamic characteristics of the SGHJD-TMOS structure, the double-pulse test circuit shown in Fig. 12 is used to evaluate its switching losses in conjunction with those of the CA-TMOS and SGHJD-TMOS as a comparison. The switching characteristics of the two structures are shown in Fig. 13. As seen in Fig. 13, both of the losses during turn-on and turn-off are reduced in the SGHJD-TMOS structure due to the lower Q_{gd}. The switching speed of the SGHJD-TMOS with a heterojunction diode is much faster than the CA-TMOS with an external JBS diode, which results in a much smaller switching loss. At the same time, the CT-MOS needs a longer period to arrive at a high V_{ds} and high I_{ds}. The T_{OFF} is defined as the turn-off delay time and turn-off fall time. The T_{ON} is defined as the turn-on delay time and turn-on fall time. Figure 14 shows the switching energy losses for the CA-TMOS and SGHJD-TMOS. It can be discerned that in the SGHJD-TMOS structure, the losses during both turn-on (E_{on}) and turn-off (E_{off}) are reduced. In the SGHJD-TMOS structure, the calculated values of E_{on} and E_{off} are 35.6 mJ/cm^2 and 30.7 mJ/cm^2, respectively, which are 21.1% and 12.2% reductions, respectively, in the counterparts of the CA-TMOS. The E_{on} and E_{off} can be expressed as

$$E_{on} = \int_{T_1}^{T_2} V_{ds} \cdot I_{ds}\, dt, \tag{1}$$

$$E_{off} = \int_{T_3}^{T_4} V_{ds} \cdot I_{ds}\, dt, \tag{2}$$

where V_{gs} (on) is 10% of its value at time T_1, V_{dd} is 10% of its value at time T_2, V_{gs} (on) is 90% of its value at time T_3, and I_{ds} is 2% of its value at time T_4.

Furthermore, Table 2 summarizes the basic characteristics of the SGHJD-TMOS and CA-TMOS, including the $R_{on,sp}$, BV, C_{gd} (C_{rss}), Q_{gd}, V_F, E_{on}, E_{off}, and HF-FOM.

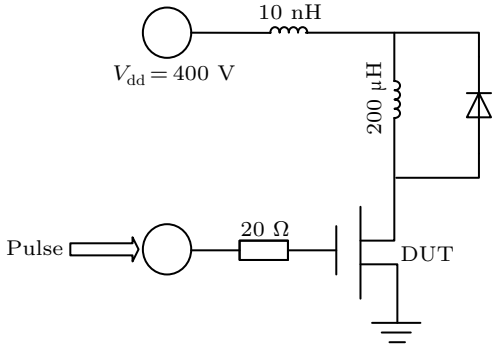


Fig. 12. The double-pulse test circuit.

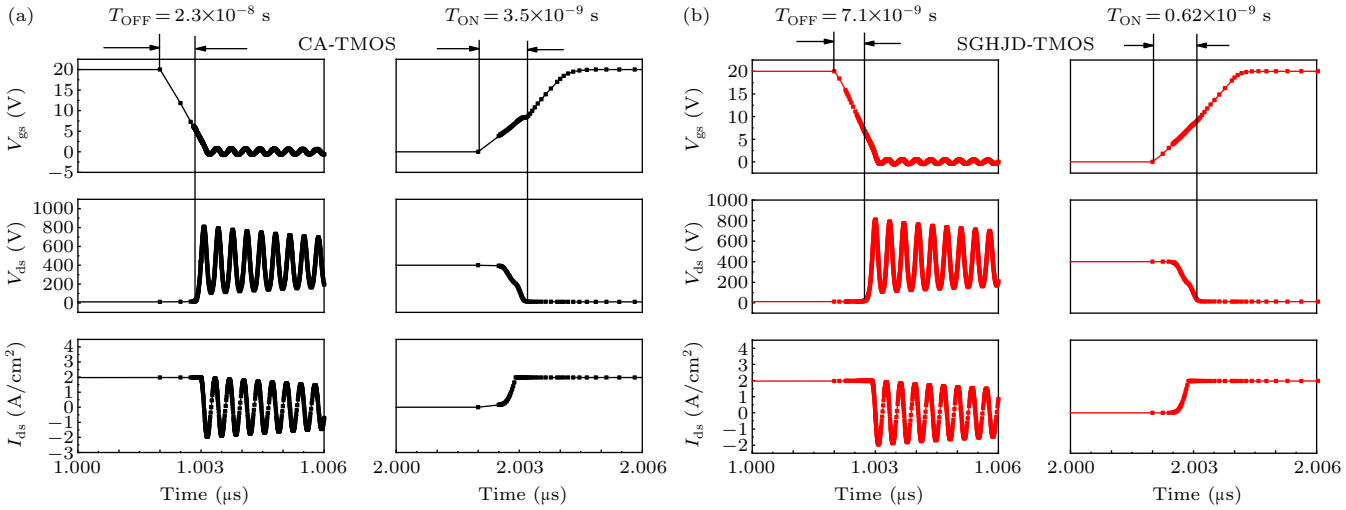


Fig. 13. Switching waveforms of (a) the CA-TMOS, and (b) the SGHJD-TMOS.

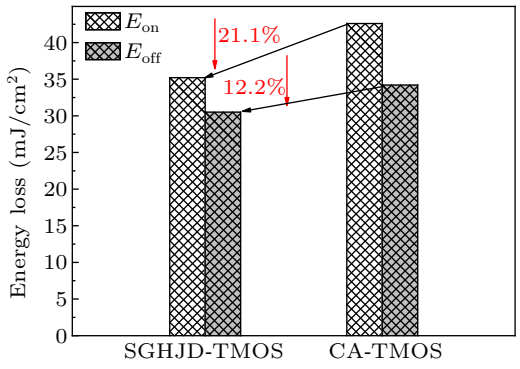


Fig. 14. Switching energy loss of the CA-TMOS and SGHJD-TMOS.

Table 2. Performance comparison of the CA-TMOS and SGHJD-TMOS.

Parameters	CA-TMOS	SGHJD-TMOS
[a]$R_{on,sp}$	2.91 mΩ·cm^2	2.94 mΩ·cm^2
BV	1402 V	1478 V
[b]C_{gd} (C_{rss})	357 pF/cm^2	46.5 pF/cm^2
Q_{gd}	63.5 nC/cm^2	26.1 nC/cm^2
[c]V_F	2.9 V	1.8 V
$R_{on,sp} \times Q_{gd}$	184.7 mΩ·nC	76.7 mΩ·nC
E_{on}	42.6 mJ/cm^2	35.2 mJ/cm^2
E_{off}	34.2 mJ/cm^2	30.5 mJ/cm^2

[a]$R_{on,sp}$ at $V_{gs} = 16$ V, $V_{ds} = 1.0$ V, [b]C_{gd} (C_{rss}) at $V_{ds} = 600$ V, $f = 1$ MHz, [c]V_F at $V_{gs} = 0$ V, $J_D = -150$ A/cm^2.

4. Conclusion

A new 4H-SiC gate trench MOSFET with an SG structure and integrated p$^+$-poly Si/SiC heterojunction freewheeling diode has been studied numerically in this article. The new structure is characterized by embedding a p$^+$-poly Si region and SiC n-drift layer in the right gate trench wall of a CA-TMOS structure and using a split-gate structure for the trench gate. The p$^+$-poly Si/SiC shield region surrounding the gate trench could effectively alleviate the high electric field around the gate trench. Compared with the CA-TMOS, the SGHJD-TMOS offers an ultralow gate-oxide electric field of 1.6 MV/cm and a forward conduction voltage drop V_F of 1.8 V. Moreover, the SGHJD-TMOS structure exhibits a lower gate–drain capacitance C_{gd}, gate–source capacitance C_{gs}, drain–source capacitance C_{ds}, and gate–drain charge Q_{gd} due to the fact that the SG reduces the gate depth and decouples the interaction between the drain and gate. Thus, the HF-FOM for the SGHJD-TMOS is reduced by 140.8%. The E_{on} and E_{off} of the SGHJD-TMOS are 35.6 mJ/cm^2 and 30.7 mJ/cm^2, respectively, which are 21.1% and 12.2% reductions, respectively, in the counterparts of the CA-TMOS. As a result, the enhanced performance makes the SGHJD-TMOS a competitive candidate for high-efficiency and high-power density applications.

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