Optimal impurity distribution model and experimental verification of variation of lateral doping termination

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Based on the charge balance principle, an optimal impurity distribution variation of lateral doping termination (OID-VLD) and its ion-injection mask design method are proposed and verified. The comparative simulations and experiments show that OID-VLD can achieve better blocking ability and reliability than the traditional VLD (T-VLD). Vertical double diffusion MOSFET (VDMOS) with OID-VLD achieved breakdown voltage (*BV*) of 1684 V and passed the 168 hours 100 °C–110 °C–120 °C–125 °C high-temperature reverse bias (HTRB) test, while VDMOS with T-VLD obtained *BV* of 1636 V and failed in the 20 hours 120 °C HTRB test.

Keywords: variation of lateral doping (VLD), junction termination, breakdown voltage, reliability

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1. Introduction

Power devices play an important role in the electric systems.[1–6] The junction termination region, enclosing the active region and helping achieve higher avalanche breakdown voltage and reliability, should be carefully considered when designing a power device. The size and fabricating complexity of the junction termination are two main factors to be considered. Commonly used termination structures include field limiting ring (FLR),[7] junction termination extension (JTE),[8] and variation of lateral doping (VLD).[9] Compared with the FLR termination, the VLD termination has the advantage of smaller size. Compared with the JTE termination, it achieves higher *BV* and is less sensitive to the fabricating process fluctuations. Therefore, VLD termination is widely used in the high-voltage power devices, and its optimization methods have been widely concerned by the industry.[10–19]

In recent years, to improve the blocking ability and reliability of VLD termination, a feasible idea is to use a hybrid VLD termination. Balestra *et al.* proposed a VLD termination structure using diamond-like carbon (DLC) passivation,[14] which reduces the charge effect of the passivation layer in the VLD termination region and enhances the reliability of the termination. Lin *et al.* proposed a VLD termination structure combined with a spiral poly resistive field plate (PRFP),[18] which has an 11% increase in *BV* and better temperature reliability than standard VLD terminations of the same size. These methods undoubtedly increase the complexity of the fabricating process. In fact, the blocking ability and reliability of the VLD termination are strongly dependent on its impurity distribution. However, there are only a few studies on it.[11,15]

In this paper, an optimal impurity distribution of VLD termination is deduced based on the charge balance principle. Technology computer-aided design (TCAD) simulations and experiments have confirmed its excellent reverse blocking performance and reliability in the power MOSFET.

2. Model and design

The structure of a VLD termination is shown in Fig. 1, whose impurity concentration gradually decreases from the boundary of main junction (point A) and VLD to the boundary of VLD and N-drift (point E). The ideal smooth variation of impurity concentration is difficult to obtain, so the actual VLD is formed by one-mask impurity ion implantation and high-temperature driving in. The impurity profile of T-VLD termination from point A to point E is linear, which is easy to design but cannot achieve optimal electrical performance.

In fact, the VLD region needs to be fully depleted to obtain the close-to-ideal avalanche breakdown. Therefore, the optimal doping concentration at any position within the VLD region can be found by the charge balance principle. A cartesian coordinate system is set as shown in Fig. 2(a), whose origin lies on point A. The boundary of the depletion region is identified as a circular arc (CD) of radius *R*, whose center is located at point O on the *y* axis. In the direction of the *y* axis, *h* is the distance from O to A, *d* is the junction depth decided by the fabrication process, and *r* is the vertical depletion width of the main junction decided by the epitaxial layer concentration and thickness. In the direction of the *x* axis, *L* is the length of

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the VLD region, and w is the lateral depletion width. h can be obtained from the geometric relationship

$$h = \frac{(L+w)^2}{2(d+r)} - \frac{d+r}{2}. \tag{1}$$

The ideal surface electric field distribution of the VLD region is rectangular since it is completely depleted, as shown in Fig. 2(b). Therefore, the minimum value of L is

$$L_{\min} = \frac{BV_{\mathrm{mj}}}{E_{\mathrm{c}}}, \tag{2}$$

where BV_{mj} is the breakdown voltage of the main junction that can be regarded as a parallel plane junction, which mainly depends on the resistivity and thickness of N-drift region. E_{c} is the critical breakdown electric field of silicon. Due to the difference between the actual electric field distribution and the ideal one, L needs to have enough margin. According to the simulation experiences, w is far less than r and usually less than half of $L_{\min}$.

According to the charge balance principle, the quantity of acceptor charges on the line MN has to be equal to that of the donor charges on the line LH. Assuming that the impurity concentration of the VLD region in the y axis direction is constant and in the x axis direction is $N(x)$, we can get

$$\int_{x_M}^{x_N} N(x)\frac{\sqrt{x_M^2+h^2}}{x_M}\mathrm{d}x = (R-|OM|-|MN|)N_{\mathrm{drift}}, \tag{3}$$

where x_M and x_N are the horizontal coordinate of point M and point N, and N_{drift} is the doping concentration of N-drift region. Since the spacing between $[x_M, x_N]$ is small, the impurity concentration variation from x_M to x_N is negligible. Using the midpoint concentration to represent the impurity concentration on line MN, equation (3) can be written as

$$N\left(\frac{x_N - x_M}{2}\right) \times |MN| = (R-|OM|-|MN|)N_{\mathrm{epi}}. \tag{4}$$

According to the geometric relationship between variables, equation (4) can be rewritten as

$$N\left(x_M + \frac{d}{2h}x_M\right) d\frac{\sqrt{x_M^2+h^2}}{h} = \left(R - \sqrt{x_M^2+h^2} - d\frac{\sqrt{x_M^2+h^2}}{h}\right) N_{\mathrm{epi}}. \tag{5}$$

Therefore, the optimal lateral concentration can be expressed as

$$N(x) = \frac{N_{\mathrm{epi}}}{d}\left[\frac{R(2h+d)}{\sqrt{4x^2+(2h+d)^2}} - h - d\right]. \tag{6}$$

It is shown that the optimal impurity concentration in the VLD region is approximately inversely proportional to its distance from the main junction.

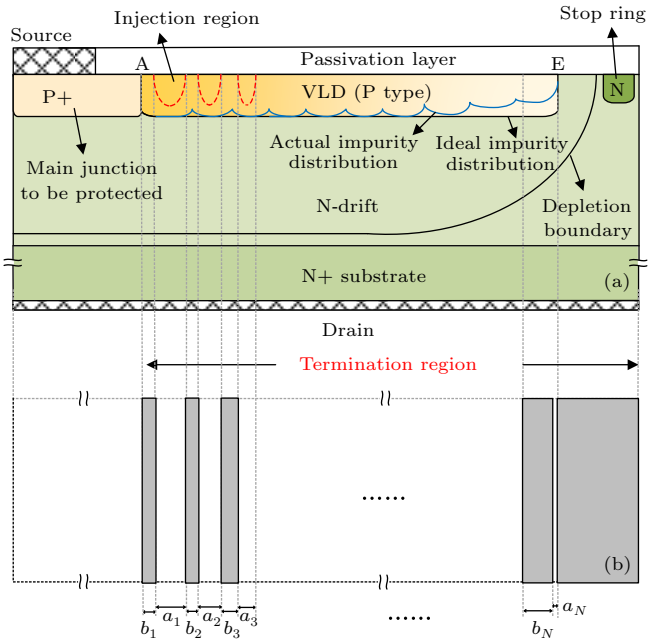


Fig. 1. The structure (a) and mask (b) of the VLD termination.

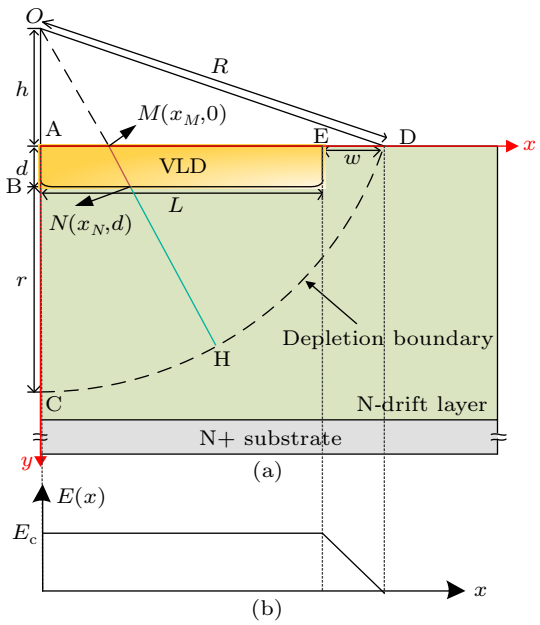


Fig. 2. Schematic diagram (a) and ideal surface electric field distribution (b) of the VLD termination.

The mask design method of the above impurity distribution is as follows: the mask is evenly divided into N segments, each with a width of L_{VLD}/N, as shown in Fig. 1(b). In the n-th segment, the width of clear region (a_n) and the width of dark region (b_n) always satisfy $a_n + b_n = L_{\mathrm{VLD}}/N$, $(n = 1,2,3,\ldots,N)$. Impurity ions are implanted into the clear regions and diffuse to their adjacent dark regions at high temperatures. The larger N, the smoother the impurity doping profile. Assuming the impurity implantation dose is D_{imp}, the effective implantation dose of the n-th segment $D_{\mathrm{eff}}(n)$ can be calculated by

$$D_{\mathrm{eff}}(n) = a_n\frac{N}{L_{\mathrm{VLD}}}D_{\mathrm{imp}}, \quad (n = 1,2,3,\ldots,N). \tag{7}$$

The continuous effective dose can be deduced by Eq. (6)

$$D_{\text{eff}}(x) = N_{\text{epi}}\left[\frac{R(2h+d)}{\sqrt{4x^2+(2h+d)^2}} - h - d\right]. \tag{8}$$

The multi-segment mask should be set to realize the doping profile in Eq. (6). Suppose $D_{\text{eff}}(0) = D_{\text{imp}}$, and then transform the continuous effective dose $D_{\text{eff}}(x)$ to the implantation dose of the n-th segment $D_{\text{eff}}(n)$. Substituting $D_{\text{eff}}(x)$ into Eq. (7), a_n can be obtained by

$$a_n = \frac{L_{\text{VLD}}}{N} \times \left[\frac{R(2h+d)}{r\sqrt{4\left(\frac{L_{\text{VLD}}}{N}n - \frac{L_{\text{VLD}}}{2N}\right)^2 + (2h+d)^2}} - \frac{h+d}{r}\right],$$
$$(n = 1, 2, 3, \ldots, N). \tag{9}$$

3. Simulation results and discussion

The reverse blocking and reliability performances of VDMOS with OID-VLD and T-VLD terminations are compared by TCAD simulation. The breakdown voltage of VDMOS cell (BV_{cell}) is 1730 V, whose width is 18 μm, N-drift is with resistivity of 62 Ω·cm and thickness of 140 μm. According to the estimation of ideal rectangular surface electric field, L of 90 μm can meet the requirement of BV. However, due to the fluctuation of impurity distribution, the surface electric field is not completely rectangular, so sufficient margin should be considered in the design. The length of VLD region L is set to 247 μm and it is divided into 19 segments ($N = 19$). For OID-VLD, w is set to 40 μm, and a_n is obtained according to Eqs. (1) and (9). For T-VLD, the first segment is totally clear, and the last segment is completely dark. The widths of clear regions are linear descent, as shown in Fig. 3.

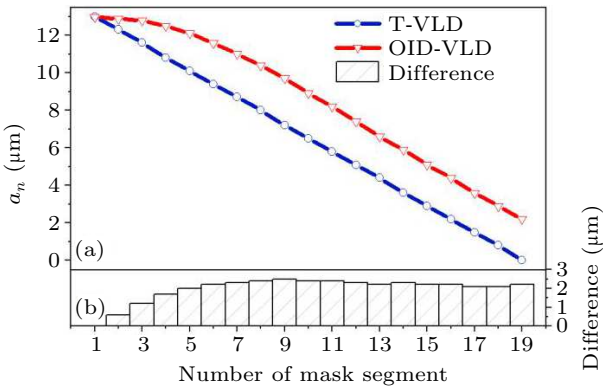


Fig. 3. (a) The clear area widths of OID-VLD (a_{n_OID}) and T-VLD (a_{n_trad}), (b) the difference of a_{n_OID} and a_{n_trad} ($a_{n_\text{OID}} - a_{n_\text{trad}}$).

As shown in Fig. 4, OID-VLD obtains the maximum breakdown voltage (BV_{max}) of 1650 V at D_{imp} of 3.7×10^{12} cm^{-2}, which is 95.38% of BV_{cell}. While T-VLD obtained BV_{max} of 1586 V at D_{imp} of 3.9×10^{14} cm^{-2}. The surface electric field and electrostatic potential profile of the two structures corresponding to their BV_{max} are shown in Fig. 4(c). OID-VLD has more uniform electric field distribution and its peak surface electric field is 5×10^3 V/cm lower than that of T-VLD. Lower peak surface electric field means less hot carriers generation which may inject into the oxide layer and higher reliability during breakdown.

When D_{imp} varies from 3×10^{12} cm^{-2} to 7×10^{12} cm^{-2}, the breakdown voltages of OID-VLD and T-VLD have the same changing trend and the maximum values of BV reduction for OID-VLD and T-VLD are 14% and 16%, respectively. The process window of OID-VLD is slightly bigger than that of T-VLD. As shown in Fig. 5, for both VLD terminations, with the decrease of dose, their electric field near the main junction side will rise, while that near the end will decrease. On the contrary, with the increase of dose, their electric field near the main junction will decrease, while that near the end will rise. In either case, BV will be reduced since it is the integral of the electric field. Therefore, a suitable D_{imp} must be found in the VLD design.

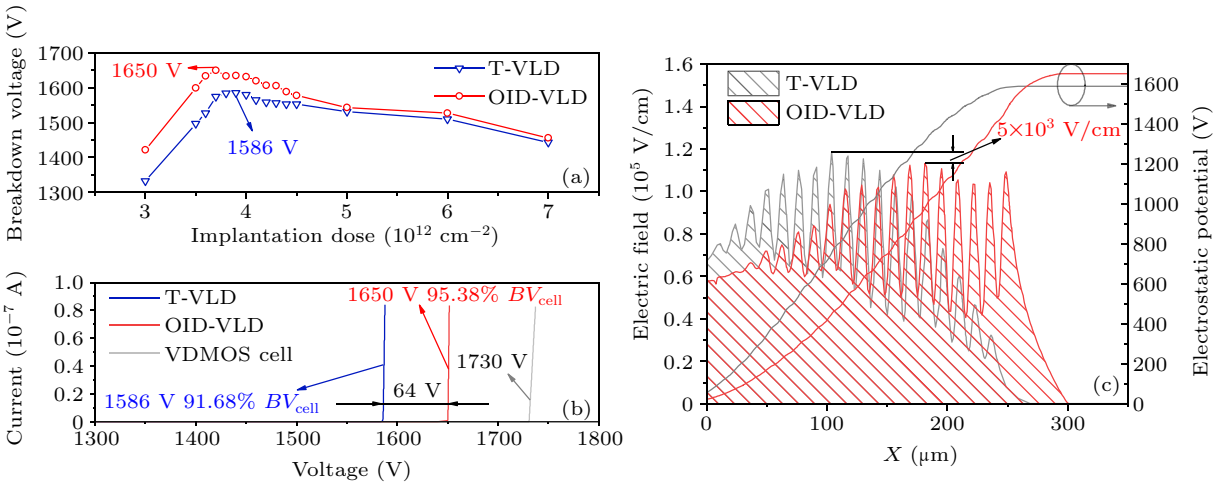


Fig. 4. (a) BV *versus* D_{imp}, (b) reverse I–V curves, (c) surface electric field and electrostatic potential profile at the dose of BV_{max} for OID-VLD and T-VLD.

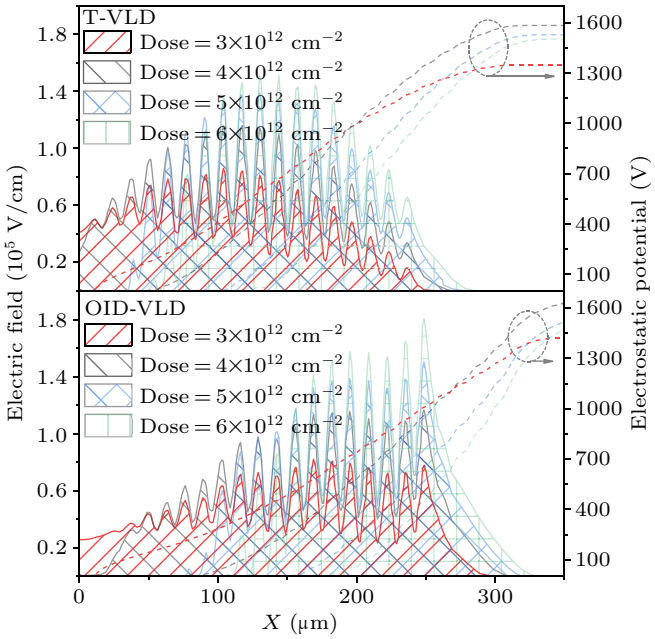


Fig. 5. The surface electric field *versus* $D_{\rm imp}$ for T-VLD and OID-VLD.

The influence of oxide charges in the passivation layer of termination, which may come from the fabrication process, or may gradually accumulate in the use, is an important reason for the reliability problems such as *BV* degradation. Therefore, positive oxide charges ($Q_{\rm ox}$) are added into the passivation layer in the simulation to evaluate the reliability of the VLD terminations.

As shown in Fig. 6(a), with the increase of $Q_{\rm ox}$, *BV* of each termination almost decreases. The reason is that the electric field near the main junction side rises, while that near the end decreases, in other words, the electric field distribution deviates from the optimal condition, as shown in Figs. 6(c) and 6(d). Obviously, the influence of increasing $Q_{\rm ox}$ on the surface electric field is similar to that of reducing $D_{\rm imp}$. This phenomenon also can be explained by the charge balance principle whose schematic diagram is shown in Fig. 7.

Without $Q_{\rm ox}$, the amount of negative acceptor charges in the VLD region ($Q_{\rm A}$) is exactly equal to that of the positive donor charges in the N-drift region ($Q_{\rm D}$),

$$Q_{\rm A} = Q_{\rm D}, \tag{10}$$

when there are positive charges in the passivation layer,

$$Q_{\rm A} = Q_{\rm D} + Q_{\rm ox}. \tag{11}$$

Since $Q_{\rm A}$ remains unchanged, $Q_{\rm D}$ becomes smaller and the depletion region in N-drift region is compressed and thus *BV* decreases.

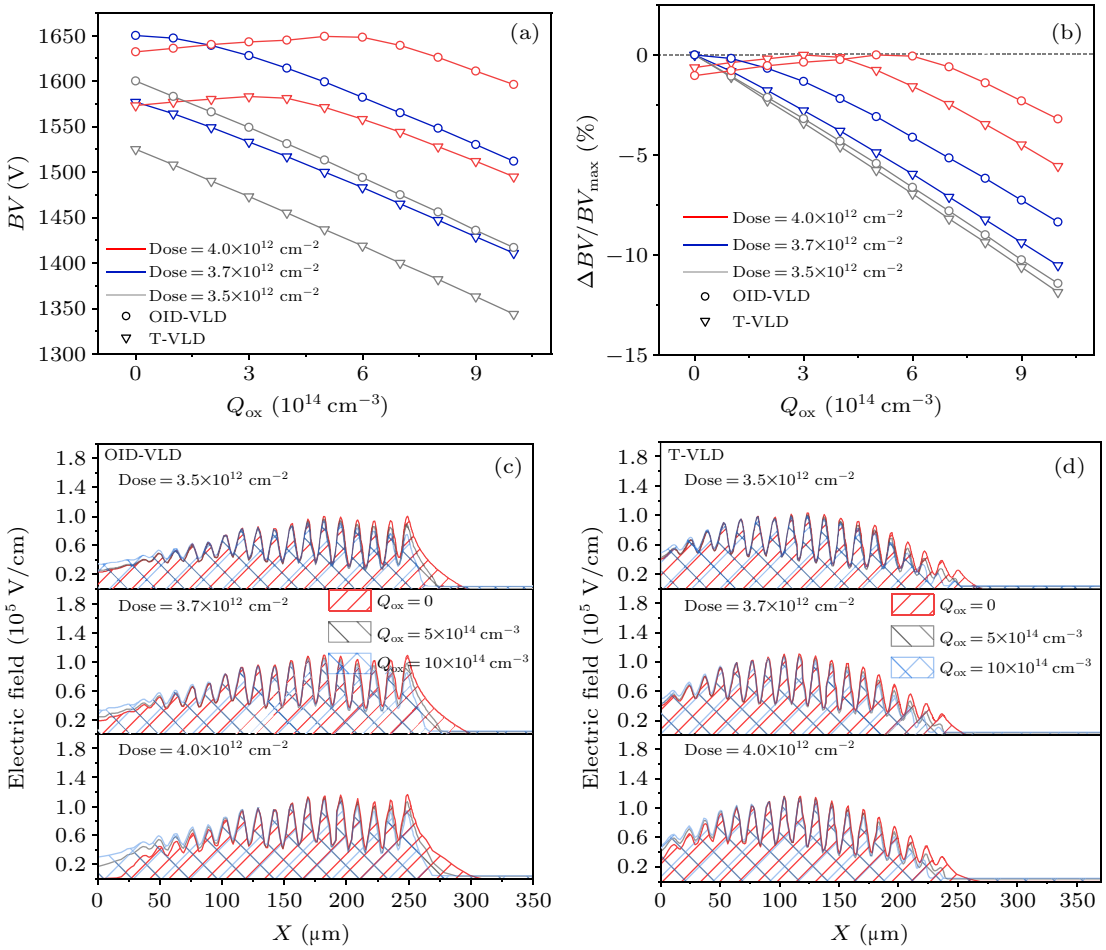


Fig. 6. (a) *BV versus* positive charge concentration in the passivation layer ($Q_{\rm ox}$), (b) the reduction rate of *BV* relative to $BV_{\rm max}$ ($\Delta BV/BV_{\rm max}$) *versus* $Q_{\rm ox}$, (c) the surface electric field *versus* $Q_{\rm ox}$ for OID-VLD, (d) the surface electric field *versus* $Q_{\rm ox}$ for T-VLD.

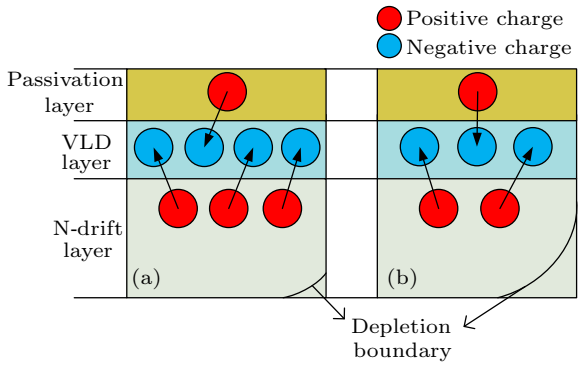


Fig. 7. Schematic diagram of the effect of Q_{ox} for higher VLD impurity concentration (a) and lower VLD impurity concentration (b).

Both T-VLD and OID-VLD are less affected by Q_{ox} at higher D_{imp} than at lower D_{imp} because Q_{ox} is much smaller than Q_D at high dose, which means that on the premise of meeting BV, selecting a higher D_{imp} is advantageous to improve the long-term reliability of the VLD termination.

At the same dose, OID-VLD is less affected by Q_{ox} than T-VLD. As shown in Fig. 6(b), $|\Delta BV/BV_{max}|$ of OID-VLD is smaller than that of T-VLD, especially at higher D_{imp}. There are two reasons: Firstly, even at the same dose, the introduced impurity concentration in OID-VLD is higher than that in T-VLD due to its larger clear region, as shown in Fig. 3(b). Secondly, the electric field peak of OID-VLD is closer to the end of VLD region, and Q_{ox} makes the electric field near the end decrease and that near the main junction rise, which causes the electric field distribution more uniform. Therefore, OID-VLD with larger impurity concentration can achieve better reliability performance than T-VLD.

4. Experimental results and discussion

VDMOS devices with OID-VLD and T-VLD were fabricated in 6-inch (1 inch = 2.54 cm) fab of Wuxi China Resources Huajing Microelectronics Co. LTD, using the same parameters as the TCAD simulation. The chip and layout of the device with OID-VLD are shown in Fig. 8(a). Limited by experimental conditions, only 4 boron implantation doses are used. Based on experience, the practical dose is set higher than the simulated one considering the absorption of boron by the oxide layer.

The measured reverse blocking characteristics are shown in Fig. 8(b). The device with OID-VLD has BV_{max} of 1684 V at boron dose of 9×10^{12} cm^{-2}, which is 48 V higher than that of T-VLD at the same boron dose. When the dose varies within the range of 6×10^{12} cm^{-2} to 1.5×10^{13} cm^{-2}, the maximum change rates of BV relative to BV_{max} are -6.5% and -7.3% for the devices with OID-VLD and T-VLD, respectively. The measured values of BV are slightly higher than the simulation ones, which may be due to the deviation between the resistivity of the epitaxial layer and its nominal value.

High-temperature reverse bias (HTRB) tests under three different conditions are performed to assess the reliability of the two terminations, as shown in Table 1. The chips are packaged with TO-200F. As the experimental conditions become more and more severe, the performances of the devices with different termination are different. The devices with OID-VLD passed the three tests, while those with T-VLD only passed the first one, whose leakage currents were not obtained in the last two tests due to failure.

As shown in Fig. 9(a), although both devices with OID-VLD and with T-VLD passed in test I, it is obvious that the devices with OID-VLD have lower average leakage currents. As shown in Figs. 9(b) and 9(c), with the increase of temperatures, the leakage currents of devices with OID-VLD increased, but still within the required range. Therefore, the OID-VLD termination can not only achieve higher BV, but also has better reliability.

Table 1. HTRB conditions and results.

	HTRB conditions	HTRB process	OID-VLD	T-VLD
Test I	$V_{DS}=1200$ V, $V_{GS}=0$ V, 5 devices	0–24 h:100 °C 24–47 h:110 °C 47–48 h:120 °C	pass	pass
Test II	$V_{DS}=1200$ V, $V_{GS}=0$ V, 5 devices	0–20 h:120 °C	pass	fail
Test III	$V_{DS}=1200$ V, $V_{GS}=0$ V, 5 devices	0–24 h:100 °C 24–48 h:110 °C 48–72 h:120 °C 72–168 h:125 °C	pass	fail

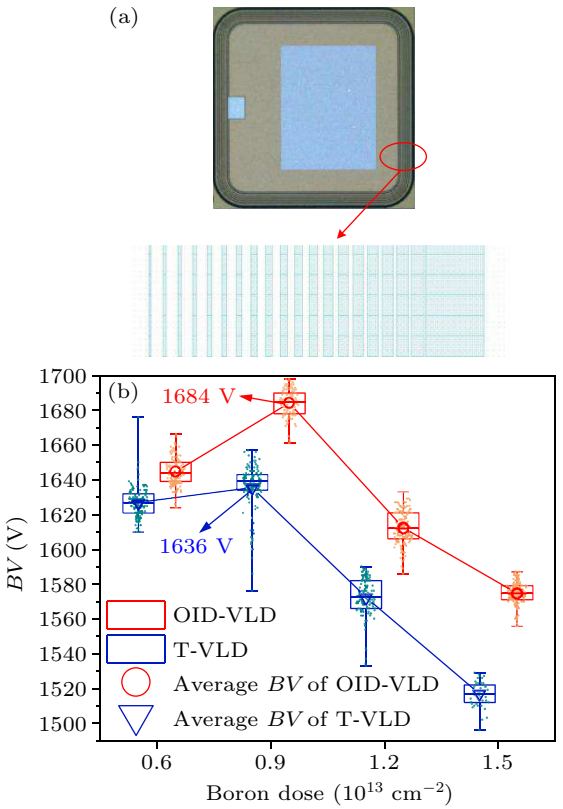


Fig. 8. (a) Chip layout of VDMOS device with OID-VLD termination and (b) *BV versus* boron dose for T-VLD and OID-VLD.

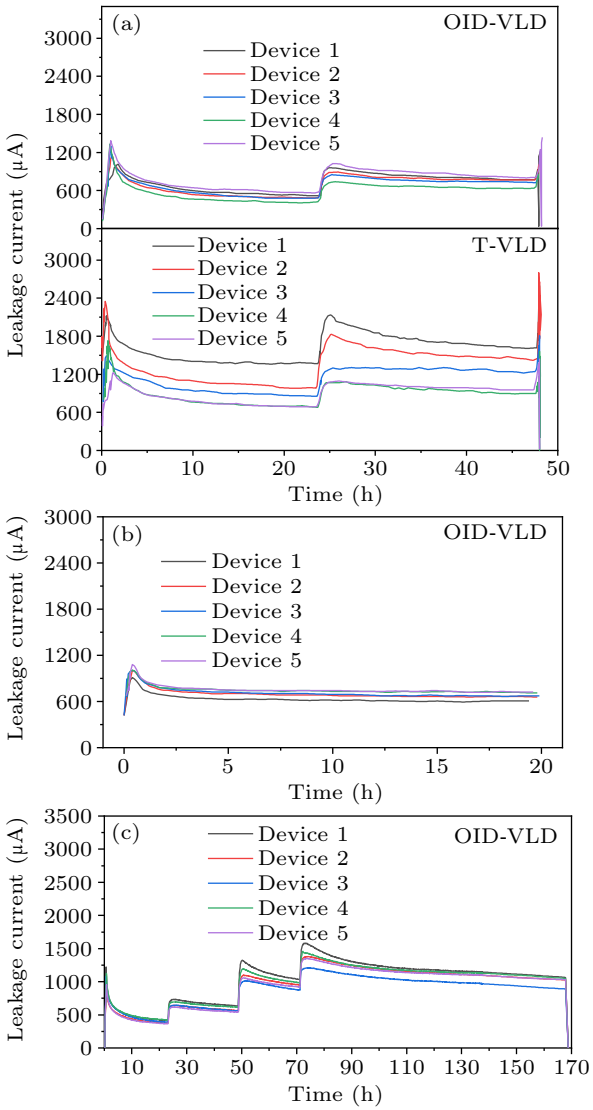


Fig. 9. HTRB tests under (a) test I, (b) test II, and (c) test III.

Explanation of HTRB failure is as follows: The movable positive charges in the passivation layer accumulate into the area with high electric field, causing the formation of inversion leakage channels on the surface of termination region and generating additional leakage currents. And the high temperature in the tests accelerates the process.[20] Positive feedback of current and temperature eventually causes thermal away. OID-VLD has a lower surface electric field and a higher concentration of surface impurities, making it more difficult to form inversion channels.

5. Conclusion

Based on the principle of charge balance, it is derived that the optimal impurity concentration in the VLD region is approximately inversely proportional to its distance from the main junction. Simulation and experimental results show that the OID-VLD has better blocking ability and reliability. A higher doping concentration is a benefit for long-term reliability of the VLD terminations, whether for OID-VLD or T-VLD. These rules can provide meaningful references for the design of VLD termination.

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