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Ambipolar performance improvement of the C-shaped pocket TFET with dual metal gate and gate–drain underlap

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Dual-metal gate and gate–drain underlap designs are introduced to reduce the ambipolar current of the device based on the C-shaped pocket TFET(CSP-TFET). The effects of gate work function and gate–drain underlap length on the DC characteristics and analog/RF performance of CSP-TFET devices, such as the on-state current (I_{on}), ambipolar current (I_{amb}), transconductance (g_m), cut-off frequency (f_T) and gain–bandwidth product (GBP), are analyzed and compared in this work. Also, a combination of both the dual-metal gate and gate–drain underlap designs has been proposed for the C-shaped pocket dual metal underlap TFET (CSP-DMUN-TFET), which contains a C-shaped pocket area that significantly increases the on-state current of the device; this combination design substantially reduces the ambipolar current. The results show that the CSP-DMUN-TFET demonstrates an excellent performance, including high I_{on} (9.03×10^{-4} A/μm), high I_{on}/I_{off} ($\sim 10^{11}$), low SS_{avg} ($\sim$ 13 mV/dec), and low I_{amb} (2.15×10^{-17} A/μm). The CSP-DMUN-TFET has the capability to fully suppress ambipolar currents while maintaining high on-state currents, making it a potential replacement in the next generation of semiconductor devices.

Keywords: tunnel field effect transistor, ambipolar current, dual metal gate, gate–drain underlap

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1. Introduction

With Moore's law, MOSFET devices have scaled to the nanometer size, the number of devices and components on a single chip has increased dramatically, and today we have a significant increase in the ability of data processing. However, to further scale, MOSFETs start to face a series of challenges: short-channel effects (SCEs), hot-carrier effects (HCEs), higher power consumption, etc. To meet these challenges, one of the solutions is to find new devices to replace MOSFETs. The tunneling field-effect transistor (TFET) is one of the promising devices to replace CMOS for low-power applications.[1] The conduction mechanism of TFETs is band-to-band tunneling (BTBT), which is the key phenomenon for the conduction of current in this quintessential reverse-biased gated p–i–n structure, unlike MOSFETs, where conduction is due to the transition of charge.[2] With a lower sub-threshold swing (SS), TFETs can break the 60 mV/decade limit at room temperature, and achieve lower off-state currents and better immunity to short-channel effects. However, there are still two main problems with TFETs: the low on-state current I_{on}, and the ambipolar characteristics. To address the low on-state current problem, researchers have now proposed a number of solutions, such as the introduction of heterostructures, including heterogeneous gate dielectrics,[3–5] source channel heterojunctions,[6–8] and heterogeneous gate materials;[9,10] the introduction of line tunneling structures to increase the tunneling area;[11–16] utilization of black phosphorus instead of silicon materials;[17,18] insertion of a metal strip in the gate oxide layer;[19] and the introduction of pocket structures.[20,21] Ambipolar conduction makes the TFET less effective in complementary circuits and restricts its utility in digital circuit design. Several solutions have been proposed to suppress ambipolar currents: using asymmetric doping,[22–24] gate–drain underlap,[23,25,26] gate–drain overlap,[27] heterogeneous dielectrics,[23,28,29] work function engineering,[23,30,31] recessed drains[32] and spacer engineering.[33]

To solve these issues, a TFET with a C-type pocket (CSP-TFET)[34] was proposed in previous work by our team, which improved the low on-state current while further reducing the sub-threshold swing; however, the ambipolar behavior was not fully suppressed. Further work is needed to optimize the structure of the device to completely suppress the ambipolar current while ensuring that the on-state current is not affected as much as possible, thus improving the performance of the device. Therefore, this work investigates the effects of both dual-metal gate and gate–drain underlap designs on the ambipolar characteristics of the device based on the CSP-TFET, respectively, and combines the two designs to propose the C-shaped

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pocket dual metal underlap TFET (CSP-DMUN-TFET). The effects of the work function of the metal gate and the gate–drain underlap length on the DC and analog/RF characteristics of the device are analyzed in detail. The optimum values of these two parameters are also determined to achieve a high on-state current with significant suppression of the ambipolar behavior.

The article is arranged as follows: Section 2 describes the basic structure of the proposed device, parameters, the model used for simulation and the calibration of the model. Section 3 discusses the DC and analog/RF characteristics of the device and the structure optimization process. Section 4 summarizes the work performed.

2. Device structure and simulation model

The C-type pocket TFET (CSP-TFET) structure is characteristically based on a conventional double-gate silicon-based tunneling field-effect transistor structure with a pocket region added to the source and channel regions with the opposite type of doping concentration to the source region. The aim of the mechanism is to enhance the electric field by fully depleting the pocket region under the action of the electric field, thus increasing the band–band tunneling rate between the source region and the channel and further improving the on-state current.

The structure parameters of the C-type pocket TFET with a dual-metal gate structure (CSP-DM-TFET) and the C-type pocket TFET with a gate–drain underlap (CSP-UN-TFET) proposed in this paper are as follows: to suppress ambipolar characteristics, the doping concentration of the source and drain are 1×10^{20} cm^{-3} and 5×10^{18} cm^{-3}, respectively. Also, the channel is doped with a doping concentration of 1×10^{17} cm^{-3}. All regions are assumed to be uniformly doped. SiO_2 was used as the gate oxide layer with a thickness of 2 nm. Based on the team's previous work,[34] we found that increasing the T_p and L_{p2} in the C-pocket would increase the leakage current and prevent the device from switching off, and increasing the T_p would also reduce the on-state current of the device. Therefore, the T_p and L_{p2} should not be large, and we also considered the fabrication issues.[35] Finally, the parameters of the C-type pocket were selected to be $L_{p1} = 30$ nm, $T_p = 2$ nm and $L_{p2} = 1$ nm. The device structures of the CSP-DM-TFET and CSP-UN-TFET are shown in Fig. 1.

All the electrical characteristics simulations were carried out by Synopsys Sentaurus TCAD. The Fermi–Dirac model, the bandgap narrowing model, the doping-dependent mobility model, the carrier Shockley–Read–Hall (SRH) model, and the Auger model were used in the simulation. Since the silicon thickness (T_{si}) is 20 nm (larger than 7 nm), quantum effects are not considered in this simulation. In this paper, we employ the dynamic non-local band-to-band tunneling (BTBT) model, which can consider the spatial variation of energy bands and apply to arbitrary tunneling potentials with abrupt or asymptotic heterojunctions, and can simulate the tunneling process more accurately. The non-local BTBT model used in this paper is calibrated using the work by Boucart and Ionescu.[3] The calibration of transfer characteristics is depicted in Fig. 2.

Table 1. The device parameters.

Variable	Parameter	Simulation value
T_{si}	silicon body thickness	20 nm
T_p	pocket 1 thickness	2 nm
L_{p1}	pocket 1 length	30 nm
L_{p2}	pocket 2 length	1 nm
L_S	source length	50 nm
L_D	drain length	50 nm
L_{ch}	channel length	49 nm
L_g	gate length	50 nm
N_{ch}	channel doping (n-type)	1×10^{17} cm^{-3}
N_s	source doping (p-type)	1×10^{20} cm^{-3}
N_d	drain doping (n-type)	5×10^{18} cm^{-3}
N_p	pocket doping (n-type)	1×10^{20} cm^{-3}
φ_1	S-gate work function	4.5 eV
φ_2	D-gate work function	4.0–4.6 eV
$L_{\varphi 2}$	D-gate length	$L_{DG} \times L_g$ nm
L_{under}	gate–drain underlap	~ 25 nm
T_{ox}	gate oxide thickness	2 nm

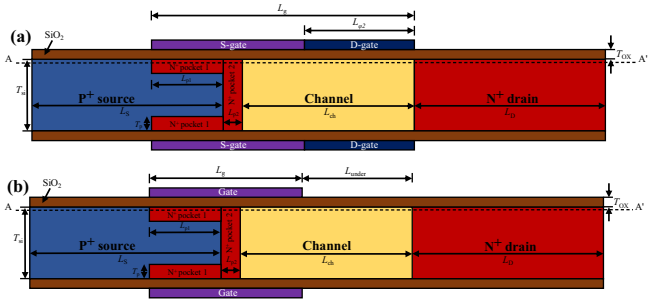


Fig. 1. A 2-D schematic view of (a) the CSP-DM-TFET and (b) the CSP-UN-TFET.

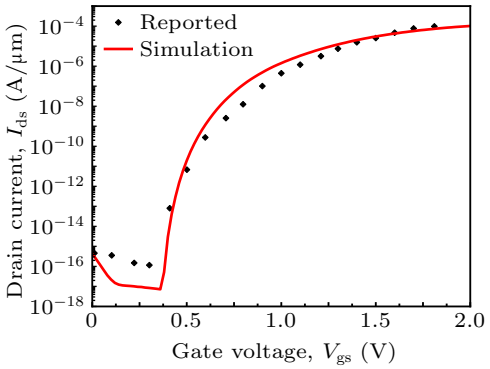


Fig. 2. Calibration of the TCAD model parameters obtained by comparing the simulated and experimental I_{ds}–V_{gs} characteristics of Ref. [3].

3. Results and discussion

The effects of the D-gate work function φ_2, the D-gate length $L_{\varphi 2}$, and the gate–drain underlap length L_{under} on de-

vice performance are investigated to obtain better suppression of ambipolar characteristics. The I_{on}, I_{amb}, I_{on}/I_{off}, and SS_{avg} are important indicators of DC characteristics, and g_m, f_T, and GBP are important indicators of analog/RF characteristics. The drain voltage V_{DS} is set to 1 V, and the gate voltage V_{gs} is varied from −1.5 V to 2 V. The currents in the states $V_{DS} = 1$ V, $V_{gs} = 2$ V, $V_{DS} = 1$ V, $V_{gs} = -1.5$ V and $V_{DS} = 1$ V, $V_{gs} = 0$ V are defined as the on-state current I_{on}, the ambipolar current I_{amb} and the off-state current I_{off}, respectively. Note that in this work, the energy band diagrams and electric field diagrams are obtained at the location of 1 nm (line A–A′ in Fig. 1) below the interface of the silicon and gate oxide layer along the channel direction.

3.1. DC characteristics analysis

3.1.1. Effect of φ_2 and $L_{\varphi 2}$ on the device

Figure 3 shows the energy band diagram of the CSP-TFET device in the on, off, and ambipolar states. When a positive voltage is applied to the gate, the energy band in the channel bends downwards, resulting in a partial overlap between the source valence band and the channel conduction band, and carriers tunneling from the valence band to the conduction band to form a current. This phenomenon is called band-to-band tunneling (BTBT). Similarly, when a negative voltage is applied to the gate, the energy band of the channel bends upwards, causing the drain valence band and the channel conduction band to partially overlap, generating a tunneling current. Since the device conducts in both gate polarities, this characteristic is called ambipolarity. This current is created when a negative voltage is applied to the gate and is called the ambipolar current. Ambipolarity is undesirable as it causes malfunction of the inverter-based logic circuits.[36]

Thus this work takes two designs to suppress ambipolar currents, namely, the dual metal gate and the gate–drain underlap, and analysis the effects of these two designs on the ambipolar characteristics of the CSP-TEFT. The present work focuses on the suppression of ambipolar currents and therefore focuses on the channel–drain junction.

The transmission characteristics of the CSP-DM-TFET are shown in Fig. 4. We set L_{p1} as 30 nm and L_{DG} as 0.5 (L_{DG} is the D-gate gate length factor, which is the proportion of D-gate to the total channel area gate length), change the D-gate gate work function φ_2 from 4.0 eV to 4.6 eV, and keep the S-gate gate work function at 4.5 eV. It can be seen from Fig. 4 that the ambipolar current decreases as the D-gate gate work

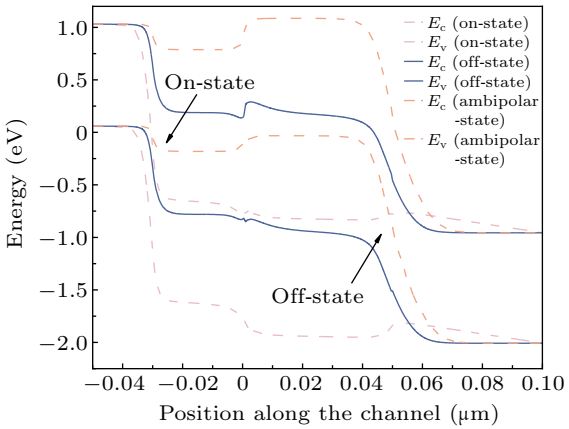


Fig. 3. Energy band diagrams of CSP-TFET devices in the on-state ($V_{DS} = 1$ V, $V_{gs} = 2$ V), off-state ($V_{DS} = 1$ V, $V_{gs} = 0$ V) and ambipolar state ($V_{DS} = 1$ V, $V_{gs} = -1.5$ V), respectively.

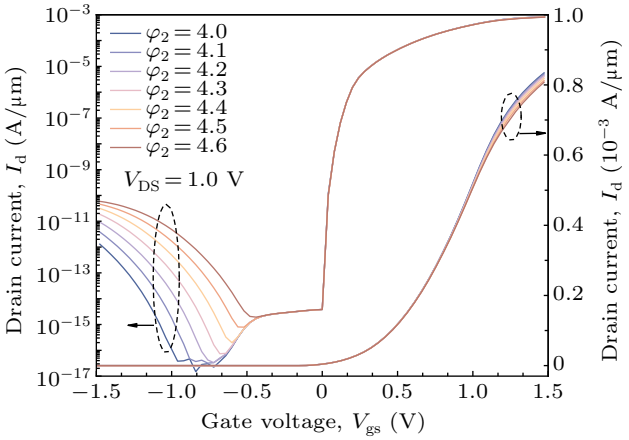


Fig. 4. Effects of the work function φ_2 on the transmission characteristics of CSP-DM-TFET devices, where the left Y-axis corresponds to the logarithmic curve and the right Y-axis to the linear curve.

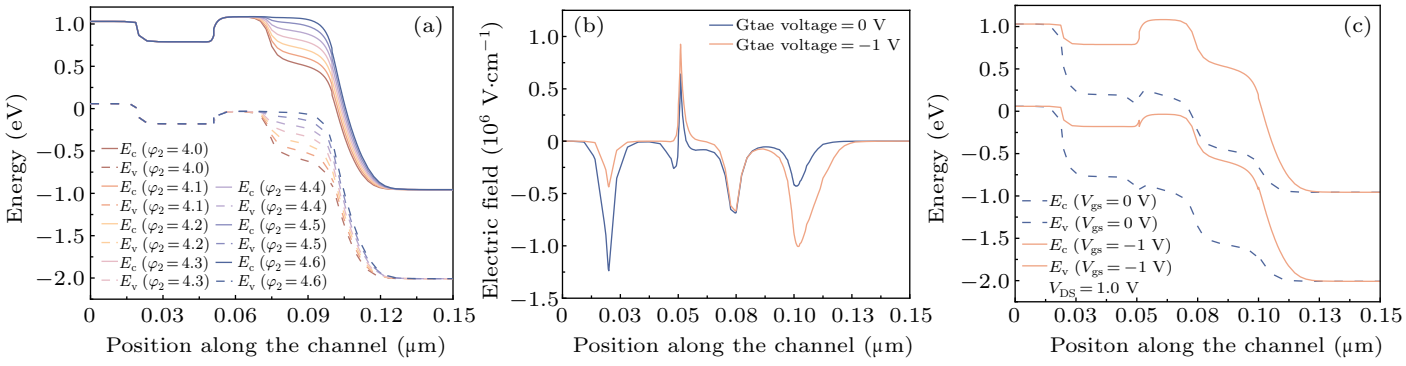


Fig. 5. (a) An energy band diagram of the CSP-DM-TFET in the ambipolar state corresponding to the variation of the work function φ_2 from 4.0 eV to 4.6 eV ($V_{DS} = 0$ V, $V_{gs} = -1.5$ V). (b) The lateral electric field intensity of the CSP-DM-TFET in the off-state ($V_{DS} = 0$ V, $V_{gs} = 0$ V) and in the ambipolar state ($V_{DS} = 0$ V, $V_{gs} = -1.5$ V). (c) An energy band diagram corresponding to the CSP-DM-TFET in the off-state ($V_{DS} = 0$ V, $V_{gs} = 0$ V) and the ambipolar state ($V_{DS} = 0$ V, $V_{gs} = -1.5$ V).

function φ_2 decreases. This is due to the fact that as the D-gate work function φ_2 continues to decrease, it leads to a reduction in the degree of energy band bending, an increase in the width of the tunneling barrier, and an increasing depletion width at the drain-channel junction, as shown in Fig. 5(a), which reduces the incidence of tunneling and suppresses the ambipolar current.

Furthermore, it can be seen from Fig. 4 that as the negative gate voltage continues to increase, the ambipolar current shows a decreasing trend and then increases. The reason for this, as shown in Fig. 5(b), is that the existence of the C-type pocket, as well as the gate full overlap structure, results in a high lateral electric field in the pocket region of the device in the off-state, leading to a high leakage current. As the negative gate voltage increases, the leakage current is suppressed. In other words, the leakage current is dominant in the negative gate voltage range of 0 V to −1 V. As shown in Fig. 5(c), as the negative voltage rises, the energy band gradually bends upwards, the tunneling barrier decreases, and the reverse conduction takes place. At this point, the tunneling current at the drain–channel junction becomes dominant.

To further optimize the CSP-DM-TFET, the effect of the $L_{\varphi 2}$ on the ambipolar and on-state currents is analyzed. The $L_{\varphi 2}$ is the length of the D-gate and is defined as $L_{\mathrm{DG}} \times L_{\mathrm{g}}$ ($0 < L_{\mathrm{DG}} \leq 1$). The effect of the L_{DG} on the DC characteristics of the CSP-DM-TFET with L_{p1} at 30 nm, L_{p2} at 1 nm, and φ_1 and φ_2 at 4.5 eV and 4.0 eV, is shown in Fig. 6(a). The L_{DG} varies from 0.1 to 0.9, with the ambipolar current decreasing with the increasing L_{DG} until it goes to 0.6. It can be seen in Fig. 6(b) that as the L_{DG} increases, the degree of energy band bending at the channel/drain junction decreases, leading to an increase in the tunneling barrier and suppression of the ambipolar current. As the L_{DG} continues to increase beyond 0.6, there is no significant change in the ambipolar current, but the leakage current in the off-state increases and the device cannot be switched off. As shown in Fig. 6(c), due to the increased L_{DG}, which brings the D-gate with its lower work function closer to the source–channel junction, the electric field strength near the source–channel junction is increased, thus reducing the tunneling barrier width and allowing the device to have a higher leakage current in the off-state. In addition, I_{on} slightly increases with the increasing L_{DG}. Based on the above analysis, the L_{DG} was optimally set to 0.6, with $I_{\mathrm{on}} = 9.66 \times 10^{-4}$ A/μm, $I_{\mathrm{amb}} = 6.94 \times 10^{-17}$ A/μm, $\mathrm{SS_{avg}} = 17.7$ mV/dec, and $I_{\mathrm{on}}/I_{\mathrm{off}} \approx 1 \times 10^{11}$. In this work, the average subthreshold swing is used as a performance metric. Bhuwalka[37] and Boucart and Ionescu[3] proposed a definition for calculating $\mathrm{SS_{avg}}$ with the following equation:[38]

$$\mathrm{SS_{avg}} = \frac{V_{\mathrm{TH}} - V_{\mathrm{OFF}}}{\log\left(\frac{I_{\mathrm{TH}}}{I_{\mathrm{OFF}}}\right)}, \tag{1}$$

where V_{TH} is the threshold voltage, whose value is the voltage corresponding to a drain current I_{TH} of 10^{-7} A/μm. And V_{OFF} takes the value of the gate voltage corresponding to a drain current I_{off} of 10^{-14} A/μm.

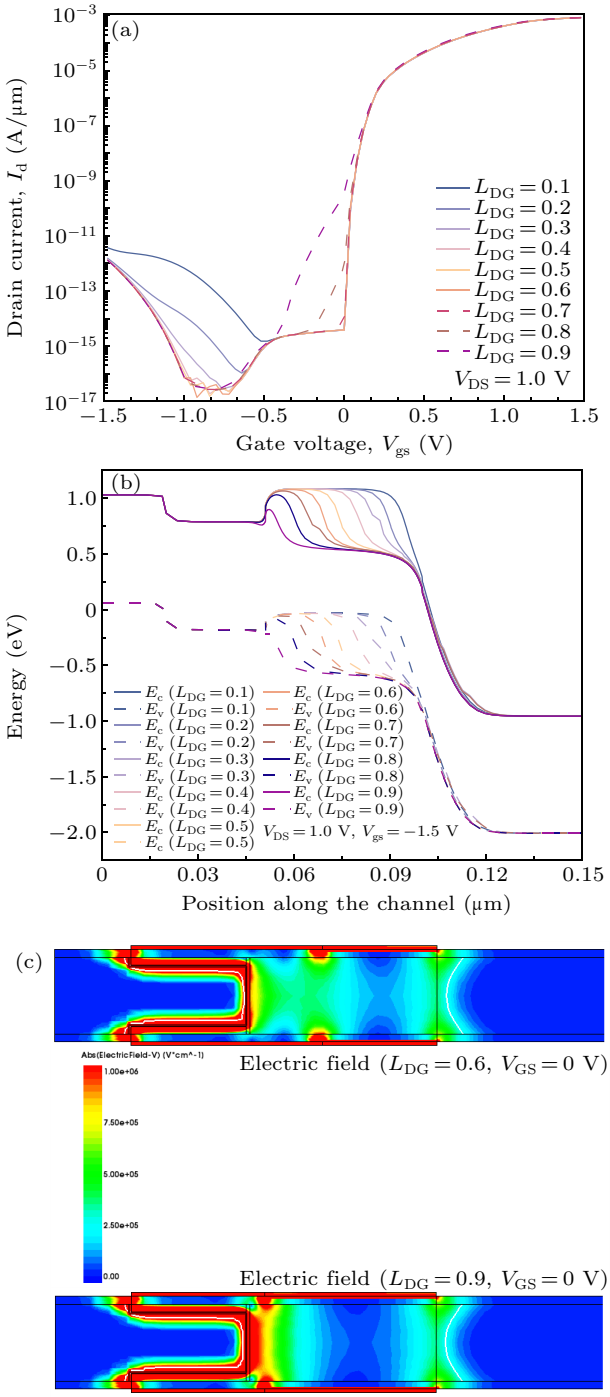


Fig. 6. (a) The effect of the L_{DG} change from 0.1 to 0.9 on the transfer characteristics of the CSP-DM-TFET devices. (b) An energy band diagram of the CSP-DM-TFET in the ambipolar state ($V_{\mathrm{DS}} = 0$ V, $V_{\mathrm{gs}} = -1.5$ V) corresponding to the change of the L_{DG} from 0.1 to 0.9. (c) Electric field distribution of CSP-DM-TFETs when the L_{DG} is 0.6 and 0.9, respectively.

3.1.2. Effect of L_{under} on the device

The CSP-UN-TFET retains full overlap of the gate at the source, varying the value of the L_{under} from 5 nm to 25 nm,

and its transfer characteristics are shown in Fig. 7(a). As the length of the L_{under} increases, the ambipolar current decreases. When it reaches 25 nm, the ambipolar current decreases by about six orders of scale. As shown in Fig. 7(b), the decreased ambipolar current is caused by gate–drain underlap, which results in a reduced electric field at the channel/drain junction. As the L_{under} increases, the electric field density at the channel-drain junction becomes smaller, which reduces the probability of tunneling and thus suppresses the ambipolar current. In addition, from the energy band diagram, as shown in Fig. 7(c), the energy band bending at the channel–drain junction decreases as the L_{under} increases, which increases the width of the tunneling barrier. Similarly, when the L_{under} is 25 nm, the ambipolar current decreases with an increasing negative gate voltage in the 0 to −1 V range. Because the leakage current dominates in this range, there is a relatively small increase in the tunneling current at the channel/drain junction. As the negative gate voltage continues to increase after −1 V, the tunneling current at the channel/drain junction dominates, at which point it rises slightly as the negative gate voltage increases. Compared to the CSP-DM-TFET, the CSP-UN-TFET is more effective at suppressing ambipolar currents, which remains low by $\sim 10^{-16}$ orders of scale at the gate voltage of −1.5 V. Furthermore, as shown in Fig. 7(a), the on-state current I_{on} decreases as the length of the L_{under} increases, but the reduction is limited. Therefore, to suppress the ambipolar current more effectively, the L_{under} length is set to 25 nm. The DC characteristics of the CSP-UN-TFET device in this case are $I_{on} = 8.34 \times 10^{-4}$ A/μm, $I_{amb} = 2.79 \times 10^{-17}$ A/μm, $SS_{avg} = 16.9$ mV/dec, and $I_{on}/I_{off} \approx 1 \times 10^{11}$.

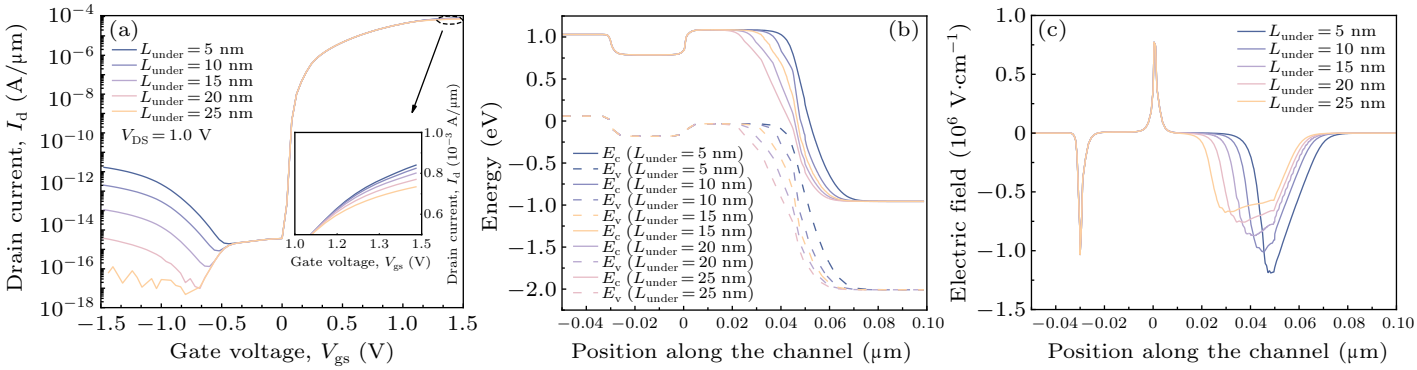


Fig. 7. (a) The effect of the L_{under} change from 5 nm to 25 nm on the transfer characteristics of CSP-UN-TFET devices. CSP-UN-TFET devices in the ambipolar state ($V_{DS} = 1$ V, $V_{gs} = -1.5$ V) with the L_{under} change from 5 nm to 25 nm, corresponding to (b) the energy band diagram, and (c) the lateral electric field.

In summary, the ambipolar characteristics of both the CSP-DM-TFET and CSP-UN-TFET devices are suppressed. But compared to the CSP-DM-TFET, the CSP-UN-TFET can suppress the ambipolar current better with the disadvantage of the reduced I_{on}.

Therefore, to ensure that the ambipolar currents are suppressed without affecting the on-state currents as much as possible, a combination of these two methods is used to compensate for the negative effects on the on-state currents caused by the gate–drain underlap structure. During the combination process of optimization, the following principles were applied: minimal reduction of the on-state current and complete suppression of the ambipolar current. The finalized improved device CSP-DMUN-TFET structure is shown in Fig. 8. The device parameters are: L_{DG} of 0.4, L_{under} of 20 nm, and φ_2 of 4.0. Figure 9 shows a comparison of the transfer characteristic curves of the CSP-DM-TFET, CSP-UN-TFET, and CSP-DMUN-TFET devices. It can be seen that the ambipolar current of the CSP-DMUN-TFET device remains at the same level as that of the CSP-UN-TFET, and the I_{on} of the CSP-DMUN-TFET is larger than that of the CSP-UN-TFET. In this case, the DC characteristics of the CSP-DMUN-TFET device are $I_{on} = 9.03 \times 10^{-4}$ A/μm, $I_{amb} = 2.15 \times 10^{-17}$ A/μm, $SS_{avg} = 13.3$ mV/dec, and $I_{on}/I_{off} \approx 1 \times 10^{11}$.

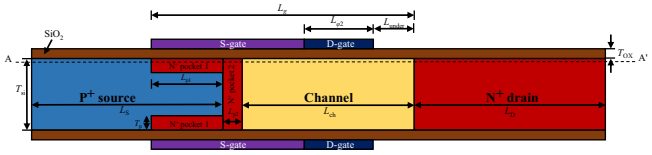


Fig. 8. A 2-D schematic view of the CSP-DMUN-TFET.

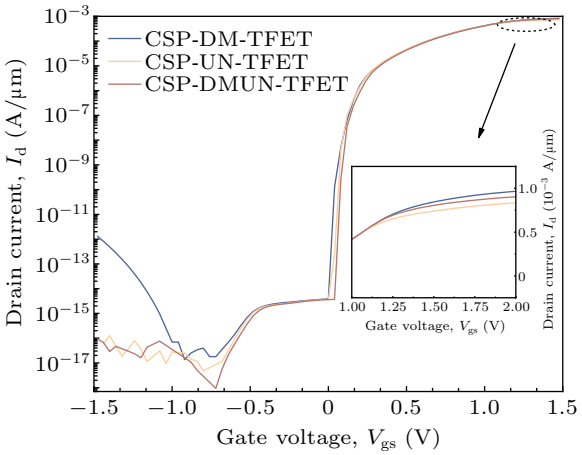


Fig. 9. A comparison of transmission characteristics curves for the CSP-DM-TFET, CSP-UN-TFET, and CSP-DMUN-TFET devices.

3.2. Analog/RF characteristics analysis

In this section, the effects of φ_2 and L_{under} on the analog/RF characteristics of the CSP-DM-TFET and CSP-UN-TFET devices are investigated, including the transconductance (g_{m}), cut-off frequency (f_{T}), gain–bandwidth product (GBP), etc., respectively. These parameters are extracted at the frequency of 1 MHz. The g_{m} is an important indicator that is used to measure the analog characteristics of devices,[39] and a higher g_{m} indicates better performance for analog applications. Analysis of the analog parameter g_{m} plays a critical role in obtaining a higher f_{T} and GBP.[40]

Figures 10(a) and 10(b) shows the effect of φ_2 and L_{under} parameters on the g_{m} of the CSP-DM-TFET and CSP-UN-TFET devices, respectively. It can be seen from Figs. 10(a) and 10(b) that as the gate voltage increases, the drain current increases, which leads to an increase in the g_{m}. However, due to the decrease in carrier mobility, the higher the V_{gs} voltage is, the lower the g_{m} is. Furthermore, it can be noted that the L_{under} has a greater effect on the g_{m} than the φ_2, as a larger L_{under} reduces the drain current.

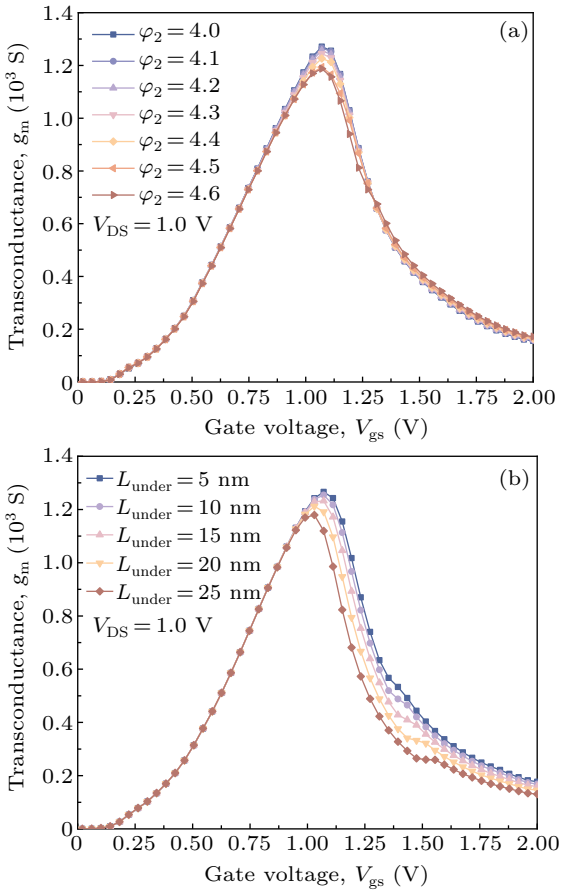


Fig. 10. (a) Variation of φ_2 from 4.0 eV to 4.6 eV, corresponding to the g_{m} of the CSP-DM-TFET device. (b) Variation of L_{under} from 5 nm to 25 nm, corresponding to the g_{m} of the CSP-UN-TFET device.

Figures 11(a) and 11(b) show the effect of φ_2 and L_{under} on the C_{gd} of the CSP-DM-TFET and CSP-UN-TFET devices, respectively. It can be seen from Fig. 11(a) that varying the φ_2 has a greater effect on the C_{gd} of the CSP-DM-TFET device at low voltages. As the lower work function increases, the coupling between the gate and drain, C_{gd}, gradually increases as φ_2 decreases, affecting the switching speed of the device. In addition, the C_{gd} decreases with the increasing L_{under}, as seen in Fig. 11(b), due to the fact that the gate–drain underlap structure increases the distance between the gate and drain regions, weakens the capacitive coupling, and reduces the effective charge concentration in the uncovered region of the gate.[41,42]

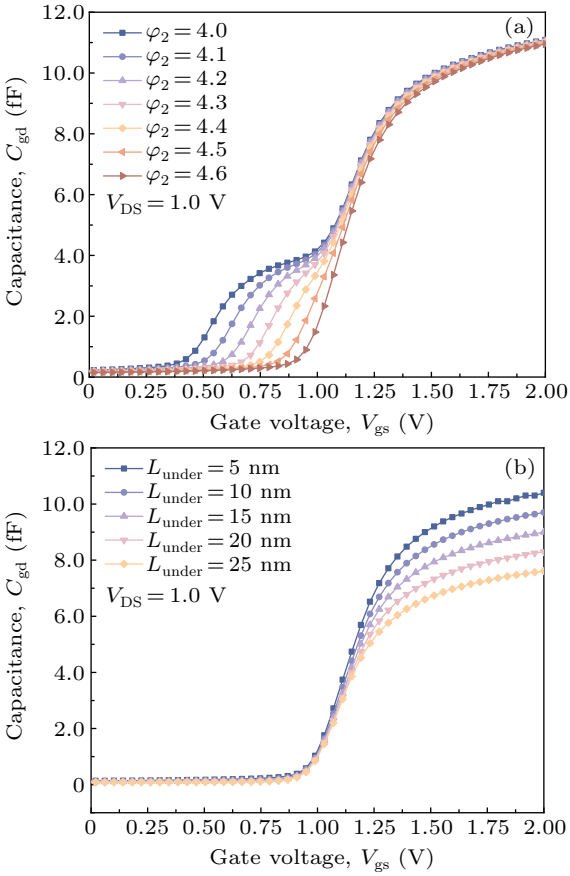


Fig. 11. (a) The change of φ_2 from 4.0 eV to 4.6 eV, corresponding to the variation of the C_{gd} of the CSP-DM-TFET device. (b) The change of L_{under} from 5 nm to 25 nm, corresponding to the variation of the C_{gd} of the CSP-UN-TFET device.

The cut-off frequency is the frequency at which the current gain becomes unity, and plays a significant role in deciding the device performance at high frequency,[43] as shown below:

$$f_{\text{T}} = \frac{g_{\text{m}}}{2\pi C_{\text{gs}}\sqrt{1+2\left(\frac{C_{\text{gd}}}{C_{\text{gs}}}\right)}} \cong \frac{g_{\text{m}}}{2\pi\left(C_{\text{gs}}+C_{\text{gd}}\right)} \cong \frac{g_{\text{m}}}{2\pi C_{\text{gg}}}. \quad (2)$$

As can be seen from Eq. (2), f_{T} is positively proportional to g_{m} and inversely proportional to C_{gg}.

As shown in Fig. 12, the f_{T} increases as the V_{gs} increases initially and after the f_{T} reaches its peak, it begins to fall sharply, due to the fact that the g_{m} begins to fall after reaching its maximum value and is accompanied by an increase in

the C_{gd}. From Fig. 12(a), it can be seen that changing the φ_2 has an apparent effect on the f_T of the CSP-DM-TFET device, due to the fact that a decrease in the φ_2 increases the coupling between the gate–drain and the C_{gd} increases. When the φ_2 is 4.0 eV, it obviously reduces the cut-off frequency of the CSP-DM-TFET. Figure 12(b) shows that the effect of the L_{under} is not very significant on the f_T, because both the g_m in the numerator and the C_{gd} in the denominator decrease as the L_{under} increases.

Another important parameter for RF analysis is the GBP, which signifies the product of gain and bandwidth at a constant DC gain value 10.[44] The value of the GBP is expressed as follows:

$$\mathrm{GBP} = \frac{g_m}{2\pi 10 C_{gd}}. \tag{3}$$

As shown in Figs. 12(c) and 12(d), the tendency of the GBP is similar to that of the f_T.

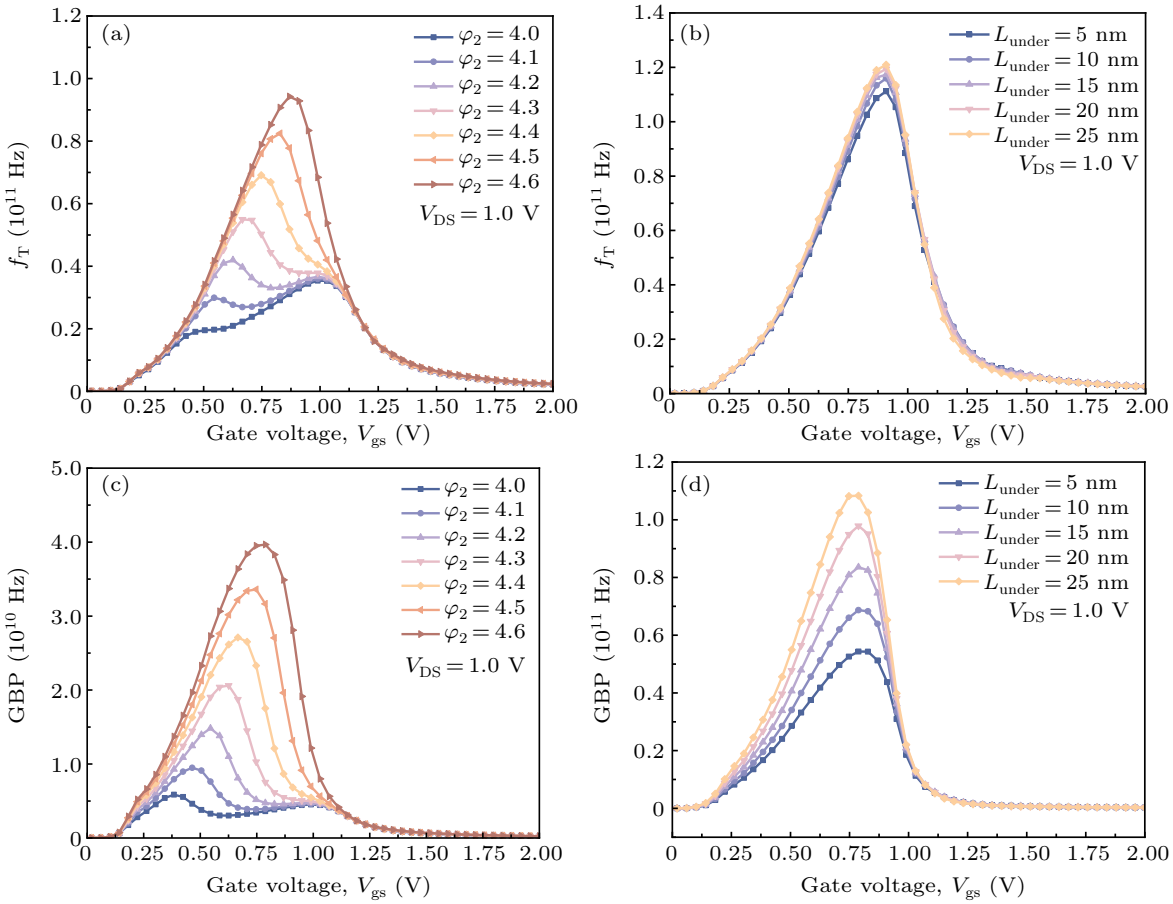


Fig. 12. (a) and (c) The change of φ_2 from 4.0 eV to 4.6 eV, corresponding to the variation of the f_T and GBP of the CSP-DM-TFET device, respectively. (b) and (d) The change of L_{under} from 5 nm to 25 nm, corresponding to the variation of the f_T and GBP of the CSP-UN-TFET device, respectively.

In summary, the CSP-DM-TFET device reduces the analog/RF characteristics by increasing the gate–drain capacitance due to the use of a lower work function in the D-gate. The CSP-UN-TFET improves the analog/RF performance by reducing the gate drain capacitance due to the presence of the underlap in the gate–drain. The CSP-DMUN-TFET device proposed in this work combines the advantages of both designs, with an analog/RF performance somewhere between the above two devices: $g_m = 1.27 \times 10^{-3}$ S, $f_T = 5.99 \times 10^{10}$ Hz, GBP $= 2.06 \times 10^{10}$ Hz.

4. Conclusion and perspectives

This work investigated the effects of dual metal gate and gate–drain underlap designs on the ambipolar characteristics of devices based on silicon-based dual-gate CSP-TFETs. Both designs are capable of suppressing ambipolar currents, with the gate–drain underlap being more effective, but with a small reduction in the on-state current, while the dual metal gate barely effects the on-state current. In addition, the dual metal gate structure causes a degradation of the analog/RF performance of the device compared to the gate–drain underlap structure. Therefore, a combination of both designs is proposed for the CSP-DMUN-TFET. Due to the full gate overlap in the pocket area, the CSP-DMUN-TFET has a high on-state current while being able to fully suppress ambipolar currents: $I_{on} = 9.08 \times 10^{-4}$ A/μm, $I_{amb} = 2.15 \times 10^{-17}$ A/μm, $\mathrm{SS_{avg}} = 13.3$ mV/dec, $I_{on}/I_{off} \approx 1 \times 10^{11}$, $g_m = 1.27 \times 10^{-3}$ S, $f_T = 5.99 \times 10^{10}$ Hz, GBP $= 2.06 \times 10^{10}$ Hz. The CSP-

DMUN-TFET effectively solves the problems of low on-state current and ambipolar characteristics of conventional dual-gate TFETs and is more suitable for low-power applications.

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