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Citation:CChin. Phys. B, 2023, 32 (**6**): 068103. DOI: 10.1088/1674-1056/acb766
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Chin. Phys. B, 2012, 21 (**3**): 038102. DOI: 10.1088/1674-1056/21/3/038102

Morphological features and nanostructures generated during SiC graphitization process

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(Received 5 December 2022; revised manuscript received 24 January 2023; accepted manuscript online 31 January 2023)

Surface morphological features and nanostructures generated during SiC graphitization process can significantly affect fabrication of high-quality epitaxial graphene on semiconductor substrates. In this work, we investigate the surface morphologies and atomic structures during graphitization process of 4H-SiC (0001) using scanning tunneling microscopy. Our high-magnified scanning-tunneling-microscope images exhibit the appearance and gradual developments of SiC (1×1) nanostructures after 1100 °C cleaning treatments, irregularly distributed among carbon nanocaps and $(\sqrt{3}\times\sqrt{3})$ reconstruction domains. A model for the formation and growth progression of SiC (1×1) nanostructures has been proposed. When post-annealing temperature reaches 1300 °C, the nanoholes and nanoislands can be observed on the surface, and multilayer graphene is often detected lying on the top surface of those nanoislands. These results provide profound insights into the complex evolution process of surface morphology during SiC thermal decomposition and will shed light on fabrication of SiC nanostructures and graphene nanoflakes.

Keywords: scanning tunneling microscopy (STM), SiC graphitization, epitaxial graphene, nanostructures

PACS: 81.05.ue, 61.48.Gh, 68.37.Ef, 79.60.Jv **DOI:** 10.1088/1674-1056/acb766

1. Introduction

Graphene, composed of two-dimensional honeycomb lattice formed by sp^2-hybridized carbon atoms, combines extreme mechanical strength, exceptionally high electronic/thermal conductivities, and many other supreme properties.[1,2] These unique properties of graphene make it highly attractive to develop applications in electronics, high frequency devices, photonic detection, and sensors, as well as energy storage.[3] For realizing practical applications of graphene-based devices, ideal fabrication methods should fulfill the requirement for controllable production of large-scale high-quality epitaxial graphene. So far, the commonly used methods for fabricating graphene include physical preparations,[1,4] chemical preparations,[5–7] and doping method.[8] Among various above-mentioned methods, thermal decomposition of semi-insulting SiC substrates has the advantage of being highly compatible with existing semiconductor processing technologies and is a promising approach to achieve wafer-size fewlayer graphene.[9] The epitaxial growth of graphene on SiC surfaces keeps to a bottom-up route: After surface pretreatments of SiC substrate, Si atoms are the first to sublimate from substrate surface under elevated temperature and ultra-high vacuum, and then the remaining C atoms reconstitute into a graphene layer, taking advantage of the fact that Si atoms have a higher saturation vapor pressure than C atoms.[10]

Over the past two decades, there have been extensive studies focusing on the growth conditions and production processes of epitaxial graphene on SiC. In order to promote the growth quality of large-scale monolayer graphene, Emtsev *et al.* used 1 atmosphere Ar as protective gas to confine sublimation of Si atoms on the 6H-SiC (0001) surface at a temperature more than 1600 °C.[11] In some research works, surface reconfigurations and nanostructures of SiC-based graphene materials were followed with interest by means of scanning tunneling microscopy (STM), electron diffraction, and photoelectron spectroscopy.[12–14] For graphene layers on 4H-SiC, various morphological features (such as step bunching, terrace pits and fingers) were observed and explored by Bolen and the coworkers.[15] Chagas *et al.* detected the triangular graphene nanoholes and nanoplateaus on SiC substrates after H-atom intercalation, showed their dual electronic response, and put forward that these nanostructures have potential applications in information storage devices of two-dimensional materials.[16] The cognition about graphene nanostructures is usually based upon the vast amount of knowledge established in the past years on the graphitization process of graphene monolayer and bilayer structures, and many theoretical and experimental investigations have addressed possible applications of these nanostructures.[17–19] However, there is still lack of research about the generation and morphological evolution of various nanostructures all through the thermal decomposition of SiC, as well as the understanding of their thermodynamics and kinetics. During the formation of epitaxial graphene, the amorphous C atoms undergo mandatory graphitization process to form hybrids sp^2 orbit.[20,21] Therefore, the detailed information about the localized surface morphologies and individual growth features is worth examining during SiC graphitization

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process, and further exploration is warranted in order to know whether annealing procedures promote or hinder graphitization.

In this work, STM operated in ultrahigh vacuum is utilized *in situ* to investigate the morphological evolution and surface atomic structure during the graphitization process of 4H-SiC (0001) substrates. The structural characteristics of various nanostructures are observed and described in detail on the clean SiC surfaces after annealing at different temperatures. Appearance and growth evolution of SiC (1×1) nanostructures during 1100 °C annealing duration are demonstrated thoroughly, and the formation mechanism of SiC (1×1) nanostructures has been discussed, as well as their growth developments. These surface nanostructures and nanoislands can play a significant role for formation and distribution of an epitaxial graphene layer on SiC. The detailed analysis and understanding about SiC graphitization process can fill the gaps between fabrication of high-quality large-scale epitaxial graphene and graphene nanostructures on SiC substrates.

2. Experimental detials

Commercial 4H-SiC (0001) wafers with a size of 10 mm×5.0 mm×0.26 mm and an N-doped density of $\sim 10^{18-19}$ cm^{-3} were used as substrates. The samples were placed into high-purity deionized water and ethanol solution for ultrasonic cleaning, blown dry with pure N_2 gas, and then were introduced into an Omicron ultra-high vacuum (UHV) STM system with a base pressure better than 2×10^{-10} mbar. The samples were annealed at 950 °C for 30 min to remove adsorbed atoms and surface contaminations, and afterwards they were annealed at 1100 °C for 6 min, 10 min, and 10 min in succession to obtain a clean SiC surface. In order to probe the surface morphological features adequately during thermal decomposition of SiC, the clean substrates were subsequently post-annealed at 900–1300 °C for 10 min. These samples were annealed by means of direct-current heating, and sample temperature was measured with an infrared pyrometer. During heating treatments, the system pressure was always maintained below 1.0×10^{-9} mbar. After each annealing, the samples were transferred to perform STM observations. All STM measurements were performed at room temperature, using tungsten tips electrochemically etched in a 2 mol NaOH solution. During measurement, bias voltage was in the range from +3 V to −3 V, with tunneling current at 0.2 nA–1.5 nA. Matrix 3.1 was used as data processing system, and SPIP software was utilized to display and analyze the STM results.

3. Results and discussion

According to previous works and our experience, 4H-SiC (0001) substrates were heated *in situ* at 1100 °C for different time intervals after being introduced into our Omicron UHV STM system, to remove surface oxides and contaminations. Although a few experimental results have been demonstrated in previous works, the morphological features and the initial graphitization process of SiC substrates are still unclear after the 1100 °C clean treatments.[9,22,23] STM images shown in Figs. 1(a)–1(c) clearly illustrate the gradual developments of overall surface morphology of clean SiC substrates. As shown in Fig. 1(a), the SiC surface is amorphous and incomplete after 6 min annealing at 1100 °C. No characteristic features can be well probed, especially at the upper part of Fig. 1(a). With the increase of annealing time, the surface terraces and steps become more and more defined, and lastly the two-layer structure of surface steps can be recognized in Fig. 1(c). The adjacent step spacing is measured to be 100 nm in average, and the whole height of steps is 0.50 ± 0.03 nm. These steps are composed of two Si–C bilayers along the (0001) direction, since the height of one Si–C bilayer is known as 0.25 nm.[24] In the ABAC stacking of 4H-SiC (0001), the first A atomic layer is less spaced from the second B layer while the second B layer is more spaced from the third A layer. This stacking constitution can result in the widths of difference of neighboring terraces on the sample surface with a miscut angle to the (0001) direction, and a two-layer structure will be exhibited at the step border similar to that in Fig. 1(c).

Occasionally small pits are found on the terraces, as highlighted by white circles in Fig. 1. The size of pits is 10–50 nm and the depth is about 0.4 nm. As the annealing time increases, the number of pits increases, large pits can be seen in a few areas on the substrate (as shown in Fig. 1(d)), which can cover two or three adjacent terraces across steps with a size even more than 200 nm, and the step orientation is disturbed by existing pits. Sometimes the triangular shaped nanostructure can be detected inside the large pit, with a quite smooth top surface. It is also shown in our experiments that the annealing temperature can induce similar morphological development on SiC before graphene formation. Hannon *et al.* have demonstrated that the formation mechanism of these large pits is pinning of SiC steps at $6\sqrt{3}$ buffer layer domains during thermal decomposition of steps at high temperature.[25] These thermal etch pits existing on SiC surface usually influence the nucleation of graphene and hinder the formation of large-scale graphene film with good homogeneity. Guo *et al.* have shown that the domain boundaries are frequently generated between the graphene islands nucleating in the defective SiC region, due to different crystalline orientations, when these islands expand in size and encounter.[26] It is also verified that the defects in SiC substrates can cause and facilitate the pit formation.[25,26] Therefore, in addition to the optimal growth procedure, high-quality SiC substrates are an important requirement for fabrication of highquality epitaxial graphene.

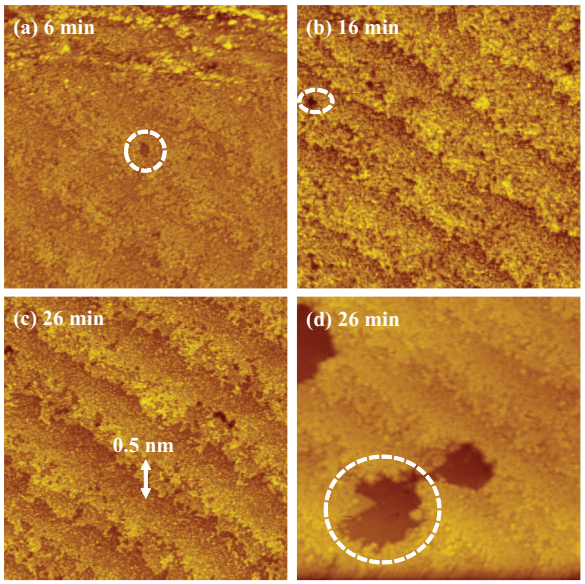


Fig. 1. STM images (400 × 400 nm) acquired on the clean surfaces of 4H-SiC (0001) after annealed at 1100 °C for (a) 6 min, (b) 16 min, [(c), (d)] 26 min.

It is well-known that the breakage of Si–C bonds occurs when a SiC substrate is heated to 1000 °C, and Si atoms sublimate from the surface, usually leaving a thin C-rich layer on the substrate.[25,27] Any characteristic STM image cannot be obtained on the SiC substrate thermally annealed below 1100 °C in UHV without Si flux.[27] After annealing at 1100 °C as clean treatments, the surface atomic features of SiC substrates have been probed detailedly in this work. Figure 2 shows the typical STM images acquired on the clean substrates after annealing at 1100 °C for 16 min and 26 min. It is clearly observed from Fig. 2(a) that many dome features with size of 1.0–2.0 nm are distributed densely over the entire surface, and an ordered atomic reconstruction is occasionally probed situated among the domes. The inset in Fig. 2(a) shows this atomic reconstruction with an in-plane period of 0.52 nm, corresponding to $\sqrt{3} \times 0.309$ nm, where 0.309 nm is the bulk lattice constant of 4H-SiC. This surface reconstruction is identified as the $(\sqrt{3} \times \sqrt{3})$ structure on SiC (0001). The dome features magnified in Fig. 2(b) show a cobweb-like pattern on their surfaces with period of 0.2–0.3 nm, which corresponds to a hexagonal network with C–C bonds of the so-called "carbon nanocaps", indicating that some Si atoms have been pyrolyzed and desorbed from the surface.[28] With the annealing time increasing, the C nanocaps gradually decrease in number, and a few regions can be found with comparatively flat surfaces among the nanocaps. In the flat region shown in Fig. 2(c), a reconstruction with a period of 1.8 nm is measured as in the inset of Fig. 2(c), consistent with the (6×6) reconstruction of SiC (0001), and it can be inferred that $6\sqrt{3}$ buffer layer is formed in this region. As displayed in Fig. 2(d), it is also noticed that the C nanocaps begin to assemble together and coalesce. The increase of annealing temperature is also found to have the same effects on the developments of SiC surface morphologies. As mentioned by Hirai *et al.*, the $(\sqrt{3}\times\sqrt{3})$ structure can exist only in a certain temperature range.[27] C nanocaps shown in Fig. 2(b) undergo a graphitization process, resulting in the morphology evolution to Fig. 2(d) after annealing at 1100 °C for a long duration, and more C–C bonds aligned virtually parallel to the surface.[28] At the same time the $6\sqrt{3}$ reconstruction can be observed, indicating the nucleation and growth of buffer layer on the surface.

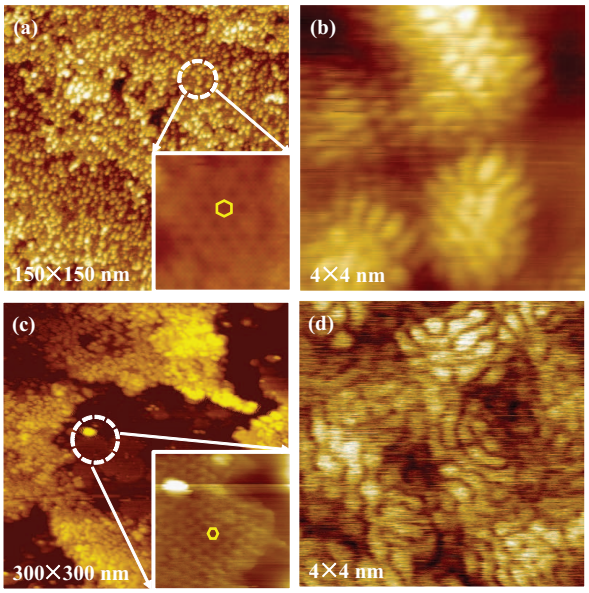


Fig. 2. Typical STM images obtained on the clean SiC (0001) surface after annealing at 1100 °C: [(a), (b)] for 16 min, [(c), (d)] for 26 min. Insets in (a) and (c) are the atomically resolved images observed inside the white dashed circles, and the tunneling conditions are $V_s = -1.6$ V, $I = 800$ pA and $V_s = -2.0$ V, $I = 700$ pA, respectively. The magnified STM images of C nanocaps existing on the substrate surface are given in (b) and (d) for $V_s = -2.0$ V, $I = 500$ pA (b) and $V_s = -0.5$ V, $I = 700$ pA (d).

Our STM observations about the surface morphological features during 1100 °C cleaning treatments of SiC substrates have revealed the presence of nanostructures, which usually appear on the substrate surface after annealing for 26 min. Randomly distributed throughout the sample surface, these nanostructures usually have atomically smooth surfaces and well-defined edges. The typical nanostructures formed during 1100 °C annealing for 26 min are shown in Fig. 3. Some have a regular triangular shape, like one exhibited in Fig. 3(a). The lateral dimensions of these nanostructures are roughly in the range of 10–100 nm, and their heights vary mainly in the 0.1–0.4 nm range. In Fig. 3(b), a nanostructure is displayed in a multilayer configuration, with a step height of 0.20 ± 0.02 nm between the upper and lower terraces. The upper terrace of this nanostructure can be seen to cover a large area. Sometimes a small number of nanowires are observed to exist on the smooth surface of nanostructures, as shown in Fig. 3(c), and this kind of nanostructure is usually found lying upon the same terrace as its neighbors but has a very clean surface without any nanocaps or clusters on it. These nanowires are

about 1.0 nm in width and 0.15 nm in height, and the adjacent nanowires usually elongate with an azimuthal orientation angle of 60° between them. The nanowires display the morphological characteristics similar to the carbon nanowires reported by Yu Aristov.[29] However, carbon nanowires were often found on β-SiC surfaces in the previous studies, less on a hexagonal SiC lattice.[29,30] To our knowledge, this kind of nanostructures has not been investigated attentively.

To get more information about the atomic structure and formation process of the nanostructures, we have probed the nanostructures thoroughly, as shown in Fig. 4(a). The triangular nanostructure is about 21 nm in size, with three interior angles of 60°, and its height is about 0.4 nm. There are some white dots decorated along the contours of nanostructure, about 0.2 nm higher than the middle of structure shown in the inset of line profile. In Fig. 4(b), the highly resolved STM image shows an ordered structure with a lattice period of 0.31 nm, consistent with the bulk lattice constant of 4H-SiC. The nanostructure is identified as SiC (1×1) crystalline structure, and is referred to as "SiC (1×1) nanostructure" in this work. For the multilayer nanostructures, SiC (1×1) structure can be ascertained on the upper and lower terraces.

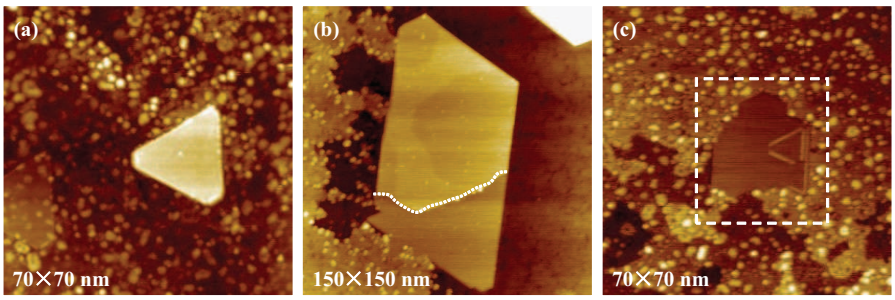


Fig. 3. STM topography images of the typical nanostructures observed on the clean surface of 4H-SiC (0001) after 1100 °C annealing for 26 min.

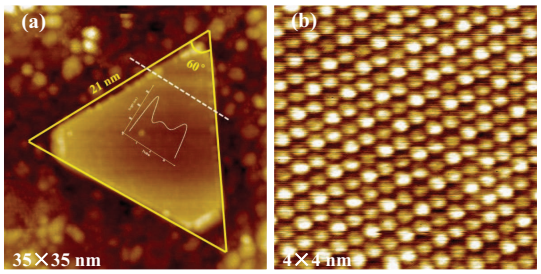


Fig. 4. (a) A triangular nanostructure formed after the SiC (0001) substrate annealed at 1100 °C for 26 min. (b) Atomic structure acquired on the top surface of the nanostructure exhibited in (a). Image parameters: $V_s = 0.85$ V, $I = 650$ pA.

It is well established that during the graphitization process of SiC (0001), the formation sequence of surface phase can be expressed as follows: $(3\times3)_{\mathrm{SiC}} \rightarrow (1\times1)_{\mathrm{SiC}} \rightarrow \left(\sqrt{3}\times\sqrt{3}\right)_{\mathrm{SiC}} \rightarrow \left(6\sqrt{3}\times6\sqrt{3}\right)_{\mathrm{SiC}} + (1\times1)_{\mathrm{graphene}} \rightarrow (1\times1)_{\mathrm{graphene}}$.[31] Under Si flux atmosphere, the (3×3)–(1×1) phase transition is believed to be a discordant transition in which the ordered Si tetramer network is replaced by a disordered lattice gas of Si adsorbates. The (1×1)–$\left(\sqrt{3}\times\sqrt{3}\right)$ transition involves the thermal desorption of about two layers of Si, due to the fact that the $\left(\sqrt{3}\times\sqrt{3}\right)$ structure consists of Si atoms adsorbed at the T_4 site, directly on the bulk terminated SiC substrate.[31,32] Our STM results show that SiC (1×1) nanostructures can be formed on the large terrace or inside the thermal etch pits after annealing at 1100 °C for a long time, and the nanowires are also observed to grow on the nanostructures. Some of SiC (1×1) nanostructures are shown to consist of a few atomic layers. The predominant shape of SiC (1×1) nanostructures is triangular due to their growth kinetics, the other shapes are derived from the triangular one.[33] According to our experimental results and other reported works,[16,31] we propose a model for the formation and growth progression of SiC (1×1) nanostructures at 1100 °C cleaning treatment, as schematically shown in Fig. 5. The red circles indicate Si atoms and the grey circles indicate C atoms. (a) At the beginning, 1100 °C heating causes the Si atoms to desorb from the substrate and the surface atoms become active. (b) C atoms aggregate into the nanocaps or clusters. The $\left(\sqrt{3}\times\sqrt{3}\right)$ structure exists among the nanocaps, and afterwards the (6×6) configurations appear randomly distributed on the surface. (c) During the annealing duration, thermal-decomposition-induced defects result in the appearance of regions with high and low atomic densities. For a low-density region, the nearby C atoms and the remaining Si atoms will converge toward to this region. The atoms in the high-density region diffuse and even sublimate around. On the Si terminal layer of SiC (0001), excessive Si atoms are incorporated into the SiC terraces and lead to faceting and twinning. When C atoms migrate to these regions, Si and C atoms can recrystallize into SiC clusters and the nucleation of SiC (1×1) nanostructure occurs on these terraces. Previous studies about graphene growth on SiC (0001) have demonstrated that Si atoms captured at the graphene/SiC interface can recrystallize into SiC clusters and two-dimensional SiC island then nucleates on the surface terraces.[34,35] (d) With further annealing, the nanowires grow on the smooth surface of SiC (1×1) nanostructure. Then, the nanostructure develops gradually into a multilayer nanostructure on the surface.

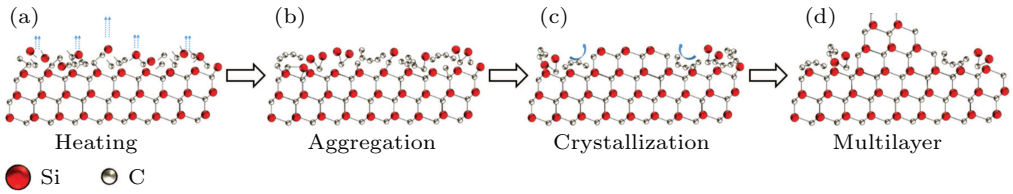


Fig. 5. Schematic diagram for the proposed progression of the SiC (1 × 1) nanostructure formation and growth during 1100 °C cleaning treatments: (a) heating, (b) aggregation, (c) crystallization, (d) nanowire and multilayer growth.

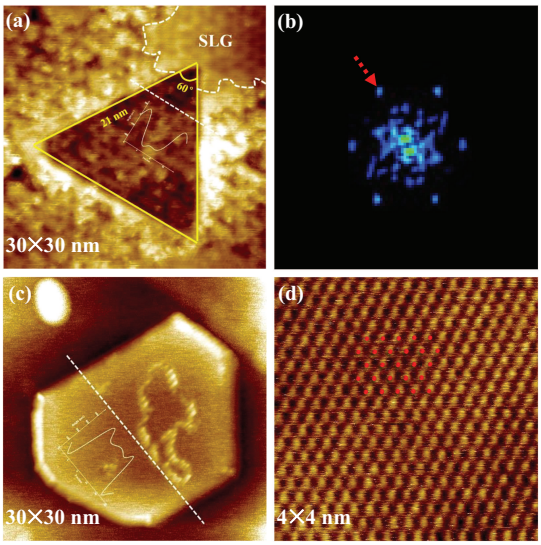


Fig. 6. STM images of 4H-SiC (0001) surface after annealing at 1300 °C for 10 min. Two typical nanostructures are often observed on the surface: (a) the triangular nanohole and (c) the elliptical-like nanoisland. (b) FFT pattern corresponding to the interior of the triangular nanohole in (a). (d) The STM images with atomic resolution obtained on the nanoisland surface in (c). $V_s = -0.3$ V, $I = 300$ pA.

After 1100 °C cleaning treatments, SiC substrates are subsequently post-annealed at 900 °C–1300 °C for 10 min, respectively. Our STM measurements have shown that 900 °C–1100 °C post-annealing cannot generate different surface morphological features from those on clean SiC surface. When samples annealed at 1200 °C and 1300 °C, the number of SiC (1 × 1) nanostructures gradually decreases, due to the thermal decomposition of SiC expedited at high temperature. It is shown that the diffusion length of C atoms will increase to several hundreds of nanometers or even more when heating temperature higher than 1200 °C.[36] The C atoms migrate and reconfigure on the surface and the whole substrate surface is covered by $6\sqrt{3}$ buffer layer and graphene layer. After 1300 °C post-annealing, two other nanostructures are usually observed, which are shown in Fig. 6. In Fig. 6(a), an equilateral triangular nanohole with a size of ∼ 21 nm and a depth of ∼ 0.23 nm is detected on the surface after 1300 °C annealing. It can be found that the hole is close to a single-layer graphene domain marked by the white dashed line. As shown in Fig. 6(b), six points of $6\sqrt{3}$ reconstruction are found in the fast Fourier transform (FFT) pattern of the surface structure inside the triangular nanohole, confirming that the interior of the nanohole exhibits a (6 × 6) structure. The elliptical-like nanoisland in Fig. 6(c) is about 22 nm average in size and 0.50 nm in height. In Fig. 6(d), the magnified STM image acquired on the nanoisland surface shows that the measured lattice period is 0.25 nm and coincides with the graphene lattice constant. It is demonstrated that this nanoisland is covered with graphene, and the ring defects of graphene can be recognized. Unlike a monolayer graphene, no contrast variations induced by the underlying $6\sqrt{3}$ buffer layer can be detected in Fig. 6(d), and only three of the six C atoms in the benzene ring are visible in the STM image, indicating that a multilayer graphene exists on the surface. In the previous work, it is shown that the nanoislands and nanoholes covered with graphene can exhibit different electronic responses, and the formation of regions with different electronic responses is potentially important for high-density data storage.[16] The emergence and extension of graphene on the nanostructures will allow us to achieve the graphene nanoflakes, which may have potential applications in nanoscale spintronics and optical nanodevices.[18,19,37,38]

4. Conclusions

In summary, we have investigated the surface morphological features and their atomic structures during the SiC (0001) graphitization process under vacuum using scanning tunneling microscopy. It is observed that 1100 °C annealing treatments can cause carbon nanocaps and thermal etch pits appear on the substrate surface. Our experimental results also demonstrate the appearance and gradual evolution of SiC (1 × 1) nanostructures during 1100 °C annealing duration. The formation mechanism and growth progression of SiC (1 × 1) nanostructures have been discussed. When post-annealing temperature reaches 1300 °C, triangular nanoholes and nanoislands can be detected on the surface due to thermal decomposition of SiC, with multilayer graphene covering on the nanoislands. These results give us a better understanding about the growth characteristics of specific surface nanostructures during SiC graphitization. This work also sheds light on fabrication of high-quality epitaxial graphene at lower temperature and formation of graphene nanoflakes.

Acknowledgement

Project supported by the Natural Science Foundation of Shanghai Science and Technology Committee (Grant No. 18ZR1403300).

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