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Investigation of heavy ion irradiation effects on a charge trapping memory capacitor by C–V measurement

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Heavy ion irradiation effects on charge trapping memory (CTM) capacitors with TiN/Al_2O_3/HfO_2/Al_2O_3/HfO_2/SiO_2/p-Si structure have been investigated. The ion-induced interface charges and oxide trap charges were calculated and analyzed by capacitance–voltage (C–V) characteristics. The C–V curves shift towards the negative direction after swift heavy ion irradiation, due to the net positive charges accumulating in the trapping layer. The memory window decreases with the increase of ion fluence at high voltage, which results from heavy ion-induced structural damage in the blocking layer. The mechanism of heavy ion irradiation effects on CTM capacitors is discussed in detail with energy band diagrams. The results may help to better understand the physical mechanism of heavy ion-induced degradation of CTM capacitors.

Keywords: charge trapping memory (CTM), high-k dielectric stack, heavy ion irradiation, reliability

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1. Introduction

Non-volatile memories are one of the key components of modern electronic systems, which have important applications in the aerospace field.[1,2] Among all of the non-volatile memories, floating gate (FG)-based memories are the most widely used. With the increasing demand for device storage capacity and performance, the feature size of the memory cell is constantly decreasing. The FG structure faces many problems such as leakage current increase, parasitic coupling effects[3–5] etc. Charge trapping technology with oxide–nitride–oxide (ONO) or high-k dielectric stack structure was used to alleviate these problems.[6] Charge trapping technology can reduce the leakage current with the trapping layer, which has abundant traps to store charges separately. However, due to the limitation of the thickness of traditional tunnel oxide, the ONO structure also faces a trade-off between the erasing/programming speed and the data retention time.[7] The high-k dielectric stack structure relies on its small equivalent oxide thickness and rich charge trap density to improve the storage characteristics of the CTM.[8–11] Thus, the high-k dielectric stack structure is an important development direction of CTM technology. Many material systems, such as HfO_2,[7] ZrO_2,[12] HfAlO,[13] and $SrTiO_3$[14] etc., have been reported to be utilized as the charge-trapping layers in a CTM capacitor. Among them, the HfO_2/Al_2O_3/HfO_2 structure has received increased attention due to its advantages of good endurance, data retention, high speed, and so on.

There are many studies[15,16] on radiation effects on FG-based memories. It was reported that the charge loss in the floating gate induced by radiation would shift the threshold voltage of cell. This can seriously affect the reliability of devices. Compared to the FG structure, the ONO structure has better radiation tolerance.[17–19] There are a series of rad-hard SONOS memories for space and military applications. There are some reports[20,21] focused on the single-event effects on CTM induced by heavy ion irradiation. In these reports, single event upset induced by heavy ion irradiation was studied in detailed. Device testing during irradiation can study the transient effects caused by heavy ions. Besides, heavy ion irradiation can also cause structural damage to device materials. The structural damage has a permanent effect on the performance of the device. However, to our best knowledge, the influence of the structural damage induced by heavy ion irradiation on CTM has rarely been reported. Up to now, investigations on the influence of heavy ion irradiation effects on CTM with HfO_2/Al_2O_3/HfO_2 structure are still very limited and the mechanism is still an open question.

In this paper, heavy ion irradiation effects on TiN/Al_2O_3/HfO_2/Al_2O_3/HfO_2/SiO_2/p-Si-based CTM capacitors are investigated. The mechanism of the effect of heavy ion irradiation on the electrical properties of the capacitor is discussed.

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2. Experimental details

The structure of the CTM capacitor used in this experiment is shown in Fig. 1. The radius of the capacitor is 100 μm. P-type silicon (100) with a resistivity of 8 Ω–12 Ω was used to fabricate the charge trapping memory. Then, a 4 nm SiO_2 film was thermally grown in a dry O_2 atmosphere as the tunneling layer due to its good interface properties. The high-k dielectrics layers (5 nm HfO_2/2 nm Al_2O_3/5 nm HfO_2) were deposited onto SiO_2 as charge trapping layer. The 10 nm Al_2O_3 blocking layer was deposited to avoid backward injection. All the oxide films were deposited *in situ* by atomic layer deposition at a substrate temperature of 250 °C. The postdeposition annealing process was carried out in an N_2 atmosphere at 700 °C for 1 min. Due to bandgap engineering, the charge trapping layer with this structure provides a large memory window, fast program/erase speed and good data retention compared to the single HfO_2 trapping layer. Fundamental test information about the CTM capacitor with this new structure has been published previously.[22] The devices were fabricated by the Institute of Microelectronics, Chinese Academy of Sciences (IMECAS).

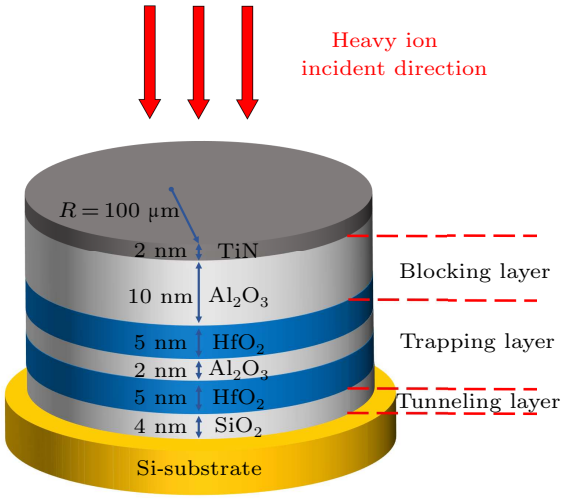


Fig. 1. Illustration of charge trapping memory capacitor.

The CTM capacitor has three operating states: (i) initial state; (ii) program (PGM) state; and (iii) erase (ERS) state. The initial state means the device without charge injection. The program process supplies a sufficiently positive voltage on the device so the carrier can cross the tunneling layer into the trapping layer and is trapped in the trapping layer.[23] The charge trap density in 2 nm Al_2O_3 film was negligible.[22] A negative bias is applied to the electrode and the erase process is completed by injecting holes into the trapping layer. After the first program process, the CTM capacitor is changed from the initial state to the PGM state. In the next operations, the CTM capacitor switches between PGM state and ERS state.

The heavy ion irradiation experiments were performed at the Heavy Ion Research Facility in Lanzhou (HIRFL) in the Institute of Modern Physics (IMP), Chinese Academy of Sciences (CAS). In this work, the charge trapping memories were irradiated with 12.5 MeV/u Ta ions. The ions pass through a 28 μm aluminum foil before reaching the capacitor surface and the $(\mathrm{d}E/\mathrm{d}x)_e$ of ion is 47.3 keV/nm in HfO_2 , 32.8 keV/nm in Al_2O_3 and 22.5 keV/nm in SiO_2 calculated by SRIM2013 code.[24] The CTM capacitors were irradiated at an ion flux of 1×10^7 ions/cm^2·s, and the fluence ranged from 1×10^8 ions/cm^2 to 1×10^{10} ions/cm^2. After conversion, the number of ions irradiated on the capacitors was from 3×10^4 to 3×10^6. Under these experimental conditions, ions cannot overlap. CTM capacitors were electrically floating during irradiation. High frequency (100 kHz) C–V characteristics were measured by a Keithley 4200A semiconductor characteristic analyzer at room temperature.

3. Experimental results and discussion

Figure 2 illustrates the C–V hysteresis curves of an unirradiated capacitor with different sweeping gate voltage ranges. The voltage at half of the maximum capacitance is defined as V_t. The difference in V_t between the program state and erase state is defined as the memory window. There is a 1.26 V memory window in a sweeping voltage of ±15 V. When the sweeping voltage increased to ±17 V, ±19 V and ±21 V, the memory window is 2.4 V, 4.0 V and 4.7 V, respectively. The memory effect can be clearly observed in this capacitor.

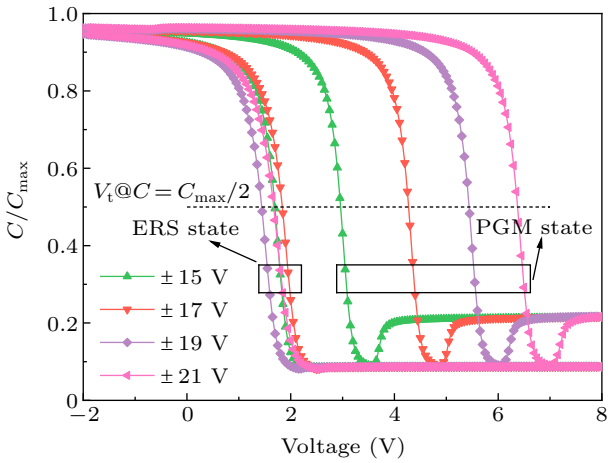


Fig. 2. The C–V curves of an unirradiated CTM capacitor with different sweeping gate voltage ranges.

Figure 3 shows the normalized C–V curves of CTM capacitors in the initial state after exposure to different ion fluences. The C–V curves shift toward the negative direction in Fig. 3, which suggests the net positive charges increased. The values of flat-band voltage (V_{FB}) and mid-gap voltage (V_{mg}) for different ion fluence were extracted from Fig. 3. The variation of net interface charge (ΔN_{it}) and net oxide trap charge (ΔN_{ot}) in the trapping layer can be calculated by the following

formula:[25,26]

$$\Delta N_{\rm it} = \frac{\left[C_{\rm ox}\left(\Delta V_{\rm FB} - \Delta V_{\rm mg}\right)\right]}{qA}, \tag{1}$$

$$\Delta N_{\rm ot} = \frac{-C_{\rm ox}\Delta V_{\rm mg}}{qA}, \tag{2}$$

where $\Delta V_{\rm FB}$ and $\Delta V_{\rm mg}$ are the difference of $V_{\rm FB}$ and $V_{\rm mg}$ before and after irradiation, $C_{\rm ox}$ is the oxide capacitance measured in accumulation, q is the electron charge (1.6×10^{-19} C) and A is the gate electrode area (3.14×10^4 μm^2).

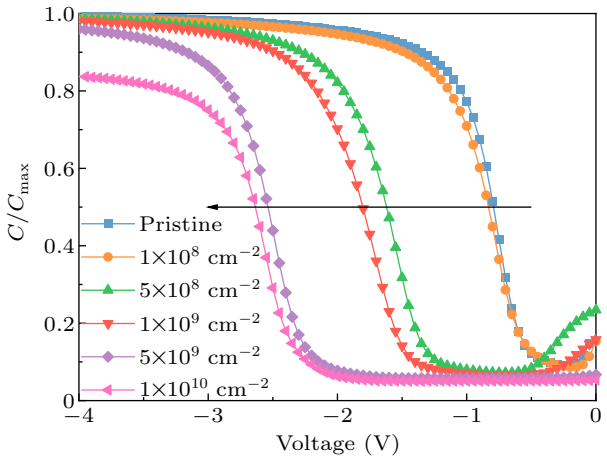


Fig. 3. The *C*–*V* curves of CTM capacitors in the initial state at different ion fluences.

Figure 4 shows the $V_{\rm FB}$, $V_{\rm mg}$, $\Delta N_{\rm it}$ and $\Delta N_{\rm ot}$ changing as a function of ion fluence. It can be seen that $\Delta N_{\rm ot}$ increases under irradiation, whereas $\Delta N_{\rm it}$ shows no obvious difference before and after irradiation. Therefore, this indicates that irradiation has a greater effect on bulk oxide than on the interface in CTM capacitors. In order to analyze the mechanism of the ion-induced variation of $\Delta N_{\rm it}$ and $\Delta N_{\rm ot}$, we calculated the vacancy density introduced by heavy ion irradiation using a SRIM model. The deduced vacancy density generated by ion irradiation is about 2.5×10^{18} cm^{-3} at the largest fluence of 1×10^{10} ions/cm^2, which is less than the intrinsic vacancy density in the trapping layer (about 10^{19} cm^{-3} [27,28]). It can be concluded that the positively charged vacancies induced by ion irradiation in the trapping layer are not the main reason for the increase of net positive charges. Thus, the increase of net positive charges in the oxide can be explained by the trapping effects of holes. In the initial state of a CTM capacitor, almost all charge traps in the trapping layer are empty. Heavy ions generate electron–hole pairs along their trajectory. Some electron–hole pairs recombine and others move in capacitors. The mobility of electrons is higher than that of holes, so the electrons are quickly ejected from the trapping layer, whereas the holes are captured in the trapping layer during transport. The accumulation of holes in the trapping layer causes the increase of net positive charges in the oxide. With the reduction of hole traps, $\Delta N_{\rm ot}$ gradually saturates due to the limited number of intrinsic hole traps in the trapping layer. The decrease of $\Delta N_{\rm ot}$ at a fluence of 1×10^{10} ions/cm^2 is attributed to the degradation of the dielectric properties of the oxide layer induced by irradiation;[29] as shown in Fig. 3, the capacitance in the accumulation region of the CTM capacitor decreased after irradiation with up to 1×10^{10} ions/cm^2.

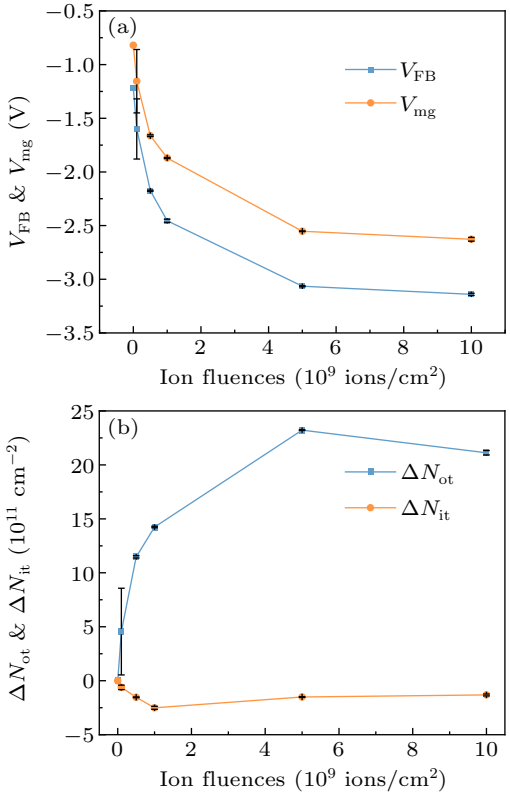


Fig. 4. (a) The $V_{\rm FB}$ and $V_{\rm mg}$ as a function of ion fluence. (b) $\Delta N_{\rm it}$ and $\Delta N_{\rm ot}$ of the CTM at different ion fluences.

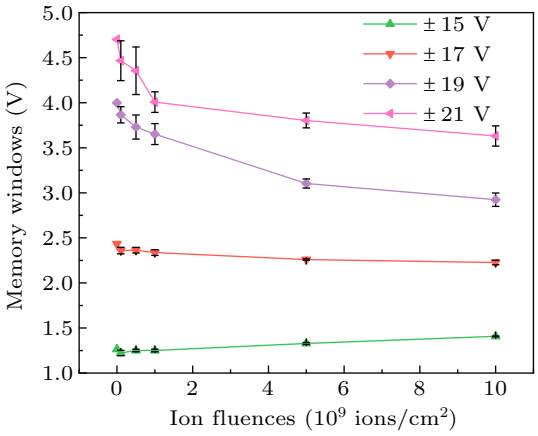


Fig. 5. The relationship between memory window and ion fluence at different sweeping voltages.

The memory characteristics of the CTM capacitors are usually characterized by the memory window. Figure 5 shows the relationship between memory window and ion fluence at different sweeping voltages. When the sweeping voltage is low, the memory window is still small and independent of ion

fluence. As the sweeping voltage is changed from ±17 V to ±21 V (high voltage), the memory window decreases with the increase in ion fluence. With the increase in applied voltage, the degradation trend of the memory window becomes more and more obvious.

In order to determine the factors affecting the memory window of the CTM capacitor, we analyzed the process of memory window formation with the help of the energy band diagram. Figure 6 illustrates the schematic energy band diagrams of the TiN/Al_2O_3/HfO_2/Al_2O_3/HfO_2/SiO_2/p-Si structure in the program process. In the program process, a positive voltage is supplied to the top electrode. Many electrons tunnel through the tunneling layer into the trapping layer (defined as J_{e1} in Fig. 6). There are many intrinsic bulk traps and interface states in the trapping layer. The electrons in the trapping layer are trapped to complete the charge storage process (defined as J_{e2} in Fig. 6). Because the blocking layer is very thick, only a few electrons in the trapping layer tunnel through the blocking layer into the TiN gate (defined as J_{e3} in Fig. 6). The erase process is the converse. A negative bias is applied to the electrode and the erase process is completed by injecting holes into the trapping layer. The difference of V_t between these two processes is defined as the memory window which characterizes the charge trapping capability of the capacitor. Through the above analysis, it was found that the memory windows of CTM capacitors were mainly affected by the charge trap process (J_{e2} process) and the charge loss process (J_{e3} process) in the program process.

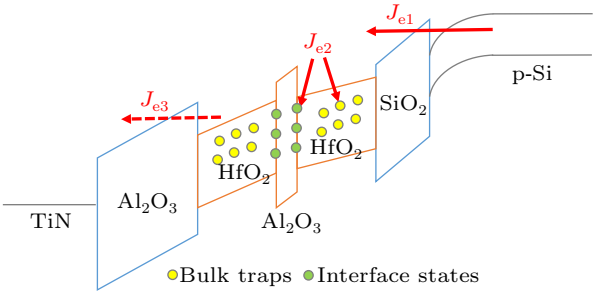


Fig. 6. Energy band diagram of TiN/Al_2O_3/HfO_2/Al_2O_3/HfO_2/SiO_2/p-Si memory structure in the program process.

The damage induced by irradiation in the tunneling layer and trapping layer does not contribute much to the change in the memory window. The tunneling layer is used to help facilitate electron tunneling in the program process at high voltage. The structural damage in the tunneling layer has negligible influence on the reduction of the memory window after irradiation. Besides, the deduced number of vacancies induced by irradiation in the trapping layer is very small compared to the number of intrinsic traps. It means that the J_{e2} process of CTM capacitors has very little impact on the variation of the memory window. We suggest that the irradiation-induced structural damage in the blocking layer is the main reason for the reduction of the memory window. On the one hand, the defects in the blocking layer induced by irradiation become the auxiliary tunneling centers of electrons. The auxiliary tunneling centers lead to the discharge of the trapping layer. This process is called trap-assisted tunneling (TAT).[30] The TAT process enhances the charge loss process (J_{e3} process in Fig. 6). The probability of charge stored in the trapping layer tunneling out through the TAT process is related to the defect concentration[31–34] and supply voltage.[35,36] The larger the defect concentration, the higher the supply voltage, and the more influential the J_{e3} process is. On the other hand, it was reported that ion latent tracks induced by heavy ion irradiation can induce the degradation of blocking layers and increase leakage current.[37–41] The $(\mathrm{d}E/\mathrm{d}x)_e$ of Ta ions is about 32.8 keV/nm in Al_2O_3, which exceeds the threshold value to form the latent tracks (6 keV/nm–10 keV/nm[42,43]). Thus, Ta ions can generate a localized region of physical damage (latent track) in the blocking layer, which enhances the J_{e3} process. The capacitance in the accumulation region of the CTM capacitor decreased after being irradiated with up to 1×10^{10} ions/cm^2 which means the dielectric constant of the oxide layer decreases with the irradiation fluence.[29] It was reported that the degradation of dielectric properties is due to structural damage of the oxide, thus it was proved that the structural damage induced by heavy ions does occur in the oxide dielectrics.

In summary, heavy ion irradiation has two effects. Firstly, heavy ions have a strong ionization ability. Heavy ions can ionize a large number of electron–hole pairs during irradiation. Secondly, heavy ions deposit a large amount of energy and generate high temperatures along their trajectories, which cause permanent structural damage within the material. The degradation of CTM capacitors caused by heavy ion irradiation is mainly reflected in two aspects: the threshold voltage shifts to the negative direction after irradiation and the memory window of the irradiated capacitors decreases with the increase of ion fluence. The negative shift of threshold voltage is due to the influence of the ionization process of heavy ions. Threshold voltage shifts caused by oxide trap charges can be recovered by program–erase operations. The decrease of the memory window is due to the structural damage induced by heavy ion irradiation in the blocking layer (Al_2O_3). The impact of the structural damage induced by heavy ion irradiation is permanent which cannot be recovered by other operations. In aerospace applications, more attention should be paid to the impact of permanent damage caused by heavy ion irradiation.

4. Conclusion

The effects of heavy ion irradiation on CTM capacitors have been investigated in this paper. It was observed that the *C*–*V* curves shifted toward the negative direction after heavy

ion irradiation, which is due to the increase of net positive charges in the trapping layer. The effects of irradiation on interface charges and oxide trap charges were analyzed in detail. Combined with SRIM simulation, the contribution of defects introduced by irradiation into the trapping layer to the threshold voltage shift was quantitatively analyzed. We believe that the threshold voltage shift is caused by the accumulation of holes. Furthermore, the memory window of CTM capacitors decreased with an increase in ion fluence and the degradation of storage characteristics was more serious at high voltage, which result from an enhanced charge loss process due to the formation of defects and latent tracks in the blocking layer. This work is helpful to understand the mechanism of CTM performance degradation induced by heavy ion irradiation.

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