

Narrowed $Si_{0.7}Ge_{0.3}$ channel FinFET with subthreshold swing of 64 mV/Dec using cyclic self-limited oxidation and removal process

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Citation: Chin. Phys. B, 2023, 32 (**7**): 077302. DOI: 10.1088/1674-1056/acad71
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Narrowed $Si_{0.7}Ge_{0.3}$ channel FinFET with subthreshold swing of 64 mV/Dec using cyclic self-limited oxidation and removal process

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(Received 29 October 2022; revised manuscript received 4 December 2022; accepted manuscript online 21 December 2022)

A narrowed $Si_{0.7}Ge_{0.3}$ channel fin field-effect transistor (FinFET) device is demonstrated in detail by using an accurate cyclic wet treatment process. The $Si_{0.7}Ge_{0.3}$ fin/per side of 0.63 nm in thickness can be accurately removed in each cycle by utilizing a self-limited oxidation with 40% HNO_3 solution in 40 s and oxidation removal can be achieved with 1% HF solution in 10 s. As a result, after the dummy gate removal, the fin width of $Si_{0.7}Ge_{0.3}$ can be narrowed from 20 nm to 8 nm by utilizing 10 cycles of this wet treatment process. Compared with the conventional $Si_{0.7}Ge_{0.3}$ FinFET under a similar process, the narrowed $Si_{0.7}Ge_{0.3}$ channel FinFET can realize a strong gate control capability by using this newly developed wet treatment process, because its subthreshold slope can be reduced by 24%, improving from 87 mV/dec to 64 mV/dec.

Keywords: $Si_{0.7}Ge_{0.3}$, FinFET, cyclic wet treatment, self-limited oxidation

PACS: 73.40.Qv, 73.22.–f, 73.90.+f **DOI:** 10.1088/1674-1056/acad71

1. Introduction

The demand for integrated circuits (ICs) with higher speed and lower power consumption has aroused great interest in technologies that provide higher mobility and better gate control capability in the channels of metal–oxide–semiconductor field-effect transistors (MOSFETs).[1] The present mainstream fin field-effect transistor (FinFET) technology, which was introduced to overcome limitations of planer technology, is facing serious scaling challenges beyond the 5-nm node.[2–4] To improve electrostatic integrity, the adoption of nanowire (NW) or nanosheet (NS) GAA device structure is expected to be necessary for shorter gate length in the future node.[5–7] Although GAA device with compatible processes is a natural extension of FinFET, it still requires some disruptive technological breakthroughs before mass production, such as inner spacer, S/D epitaxial grown, multiple Vt.[8–10] Meanwhile, SiGe high mobility channel FinFET has also been proposed as a promising candidate to replace Si FinFET due to its higher hole mobility, better negative bias temperature instability (NBTI) reliability than Si.[11] Moreover, the scaling of fin width to improve gate controllability and the increasing of fin height to improve driven capacity have been critical factors of FinFET devices. Therefore, the scaling of fin width of SiGe channel with high mobility needs further study, because there are relatively few relevant studies so far.

In this work, a narrowed $Si_{0.7}Ge_{0.3}$ FinFET device with an excellent subthreshold slope (SS) of 64 mV/dec is demonstrated by employing a precise cyclic wet treatment process, which is based on a self-limited oxidation in each cycle. More importantly, compared with the conventional $Si_{0.7}Ge_{0.3}$ FinFET, this narrowed $Si_{0.7}Ge_{0.3}$ channel FinFET can realize a strong gate control capability.

2. Experiment

The key fabrication steps of narrowed $Si_{0.7}Ge_{0.3}$ channel FinFET are presented in Fig. 1. After a standardized N-well formation, $Si_{0.7}Ge_{0.3}$ film was epitaxially grown on an Si substrate via a reduced pressure chemical vapor epitaxial deposition (ASM Epsilon 2000). Then, Si substrate/$Si_{0.7}Ge_{0.3}$ fin structure was patterned through the sidewall image transfer method under an optimized HBr/O_2 based plasma. Subsequently, shallow trench isolation (STI) filling and planarization were implemented, followed by a low-temperature STI densification annealing of 850 °C for 30 s. Then, $Si_{0.7}Ge_{0.3}$ fin was revealed by using a 1:100 diluted HF solution. After a conventional $Si_{0.7}Ge_{0.3}$ fin was prepared, a low-temperature SiO_2 deposition and dummy gate patterning were carried out. Afterwards, lightly doped drain (LDD) and source/drain (S/D) implantation with B and BF_2 dopant were implemented after spacer 1 and spacer 2 have been fixed. A low-temperature dopant activation of 850 °C for 30 s was performed to maintain the $Si_{0.7}Ge_{0.3}$ fin stability. After dummy gate removal, nitric acid (HNO_3) and hydrofluoric acid (HF) were separately used as oxidant and oxide remover agent to perform cyclic wet etching treatment on the exposed $Si_{0.7}Ge_{0.3}$ fin. After several cycles of self-limited oxidation and removal process were implemented, the narrowed $Si_{0.7}Ge_{0.3}$ fin with precisely controlled fin width was achieved. Afterwards, *in-situ* O_3 passivation combined with Al_2O_3/HfO_2 bilayer high-*k* dielectric (HK) and TiN-based metal gate (MG) was employed to form the gate stack by using an atomic-layer-deposition tool. Finally, the standard Si FinFET processing was adopted to complete the narrowed $Si_{0.7}Ge_{0.3}$ FinFET device fabrication.

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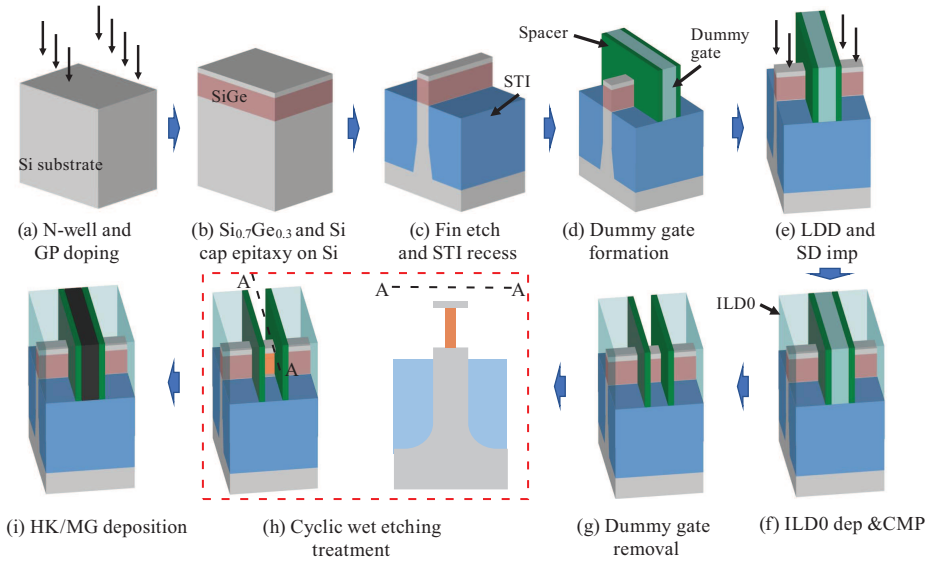


Fig. 1. Key process of narrowed $Si_{0.7}Ge_{0.3}$ channel FinFET.

3. Results and discussion

3.1. Conventional $Si_{0.7}Ge_{0.3}$ fin preparation

Epitaxially grown quality and fin etching profile of SiGe film are two key factors for the conventional SiGe fin structure. Figure 2(a) presents the ω–2θ HRXRD scan result of epitaxial grow of SiGe on Si substrate, showing well-defined interference sub-peaks (Kiessig frings) on both sides of SiGe peak, which are characteristics of high-quality SiGe film. Meanwhile, the fitting result shows that the thickness of SiGe film is 29.58 nm and the percentage of Ge atoms is 31.83%. Figure 2(b) shows the result of $Si_{0.7}Ge_{0.3}$ fin reveal after HBr/O_2 based plasma etching and STI recess. It is found that a completely vertical and uniform profile of Si substrate/$Si_{0.7}Ge_{0.3}$ fin with a width of $\sim$ 20.5 nm is attained.

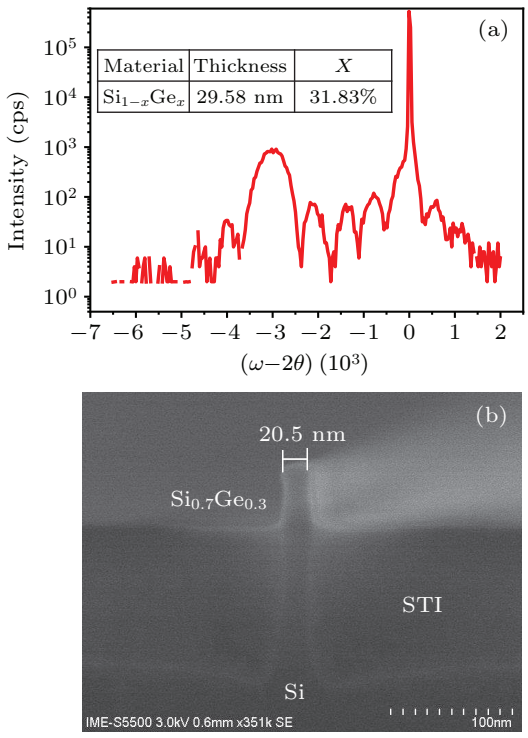


Fig. 2. (a) HRXRD spectra result on epitaxially grown SiGe. (b) SEM image of $Si_{0.7}Ge_{0.3}$ fin post fin reveal.

3.2. Narrowed $Si_{0.7}Ge_{0.3}$ fin preparation

It was reported that SiGe film is completely etched off by using HF/oxidizer based solutions, such as $HF:HNO_3:CH_3COOH$ and $HF:H_2O_2:CH_3COOH$, to release the channel of Si GAA device[12,13] However, these mixed solutions cannot be directly applied to the narrowing of $Si_{0.7}Ge_{0.3}$ fin, because the oxidation of $Si_{0.7}Ge_{0.3}$ fin and its removal occur at the same time, and the width of $Si_{0.7}Ge_{0.3}$ fin cannot be precisely controlled.

To precisely control the width of the narrowed $Si_{0.7}Ge_{0.3}$ fin, a novel cyclic wet treatment process is proposed, in which oxidant for self-limited oxidation and oxide remover agent are used separately. In our experiment, 40% HNO_3 solution is selected for self-limited oxidation and 1% HF solution is selected for oxide removal. It is found that the oxidation of $Si_{0.7}Ge_{0.3}$ fin can reach saturation when the immersion time of HNO_3 is longer than or equal to 40 s, and 0.63-nm $Si_{0.7}Ge_{0.3}$ fin/per side can be accurately removed in the following HF solution when its etching time is larger than 5 s as shown in Fig. 3(a). Therefore, self-limited oxidation with 40% HNO_3 solution for 40 s and this oxidation removal process with 1% HF solution for 10 s is chosen as the optimal process condition. Based on this cyclic wet treatment of self-limited oxidation/removal process, the precise control of $Si_{0.7}Ge_{0.3}$ fin width can be achieved by controlling the number of cycles. Figure 3(b) shows the SEM result of $Si_{0.7}Ge_{0.3}$ fin after 10 cycles of wet treatment post fin reveal. Comparing with Fig. 2(b), the width of $Si_{0.7}Ge_{0.3}$ fin is significantly narrowed with a high selectivity to Si cap layer. Meanwhile, it can also be seen that the $Si_{0.7}Ge_{0.3}$ fin height can be well maintained in

this newly developed process due to the high selectivity to Si cap.

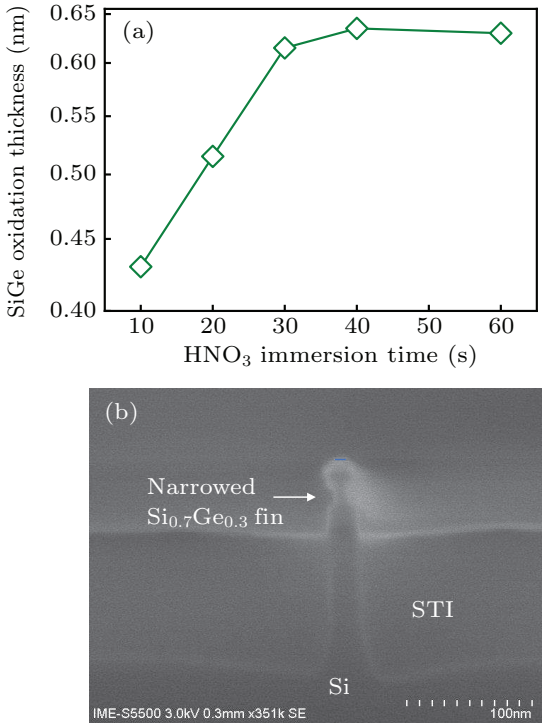


Fig. 3. (a) $Si_{0.7}Ge_{0.3}$ fin removal thickness/per side in each cycle, (b) SEM image of $Si_{0.7}Ge_{0.3}$ fin after 10 cycles of wet treatment.

Figure 4 shows the mechanism of precise cyclic wet treatment process of the $Si_{0.7}Ge_{0.3}$ fin. The oxidation characteristics of SiGe and Si in HNO_3 solution are different. For Si material, a stable and very thin SiO_x layer can be formed on its surface. However, SiO_x and GeO_x are simultaneously formed on the SiGe surface and the GeO_x will be dissolved in water, so the oxidation will not stop until sufficient SiO_x is formed.[14,15] Therefore, one cycle of self-limited oxidation is completed before this oxidation has been completely removed by the HF solution. This signature is consistent with the phenomenon that oxidation thickness of $Si_{0.7}Ge_{0.3}$ fin first increases and then turns saturated as HNO_3 solution immersion time going by. Therefore, a narrowed $Si_{0.7}Ge_{0.3}$ fin can be precisely achieved by controlling the number of wet treatment cycles.

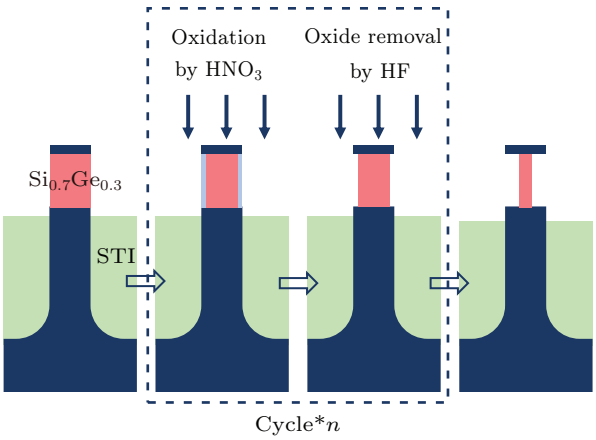


Fig. 4. Mechanism of precise cyclic wet treatment process of $Si_{0.7}Ge_{0.3}$ fin.

3.3. Narrowed $Si_{0.7}Ge_{0.3}$ FinFET device

This newly developed cyclic wet treatment process is successfully applied to the preparation of the narrowed $Si_{0.7}Ge_{0.3}$ FinFET. Comparing with the conventional $Si_{0.7}Ge_{0.3}$ FinFET integration process, the main difference of this narrowed $Si_{0.7}Ge_{0.3}$ FinFET is that this cyclic wet treatment process is inserted after the removal of dummy gate. More importantly, the HNO_3 solution or HF solution in this cyclic wet treatment process has sufficient selectivity to Si and other films (such as SiN spacers). Therefore, this cyclic wet treatment process is completely compatible with mainstream FinFET technology.

Figure 5 shows the EDS mapping analysis results of this narrowed $Si_{0.7}Ge_{0.3}$ fin under the HK/MG stack at the end of fabrication process. It is found that the width of $Si_{0.7}Ge_{0.3}$ fin is narrowed from 20 nm to 8 nm and the width of Si cap is almost unchanged. These results further confirm that this newly developed wet treatment process can accurately control the width of $Si_{0.7}Ge_{0.3}$ fin and has a high selectivity to Si. Moreover, the multilayer HK/MG is well wrapped around the narrowed $Si_{0.7}Ge_{0.3}$ fin, which may help to achieve an excellent gate controllability of this narrowed $Si_{0.7}Ge_{0.3}$ FinFET. In addition, after cyclic wet treatment, it is also found that the surface of $Si_{0.7}Ge_{0.3}$ fin is slightly concaved, which may have some influence on the performance of FinFET, such as gate control capacity. This slightly concaved $Si_{0.7}Ge_{0.3}$ fin profile can be further improved by developing new dry etching in the future.

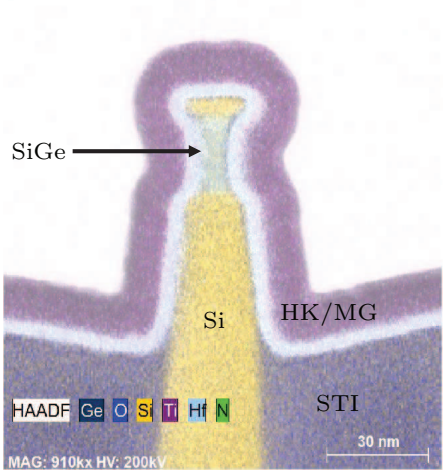


Fig. 5. EDX mapping analysis result of narrowed $Si_{0.7}Ge_{0.3}$ FinFET device.

The I_{DS}–V_{GS} curve of this narrowed $Si_{0.7}Ge_{0.3}$ FinFET is given in Fig. 6. I_{DS} of 421 μA/μm under $V_{DS} = V_{GS} = -0.8$ V, I_{ON}/I_{OFF} ratio of $\sim 3 \times 10^5$, and SS of 64 mV/dec are obtained. Comparing with the conventional $Si_{0.7}Ge_{0.3}$ FinFET with optimized electrical performance reported earlier,[16] its SS can be reduced by 24%, improving from 87 mV/dec to 64 mV/dec. These mentioned results indicate that a stronger gate control capability to the $Si_{0.7}Ge_{0.3}$ channel is attained after adopting a narrowed $Si_{0.7}Ge_{0.3}$ fin by utilizing a precise cyclic wet treatment process.

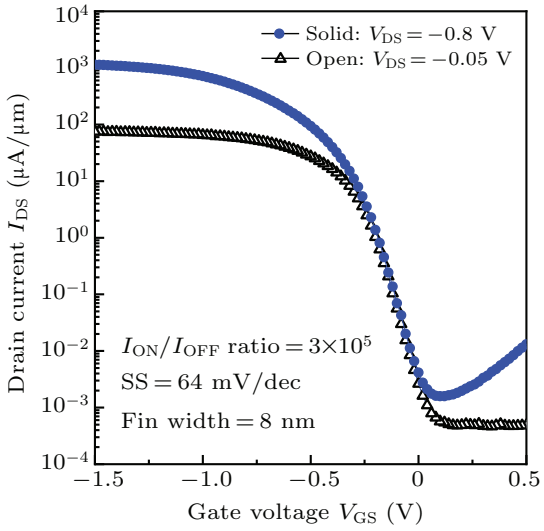


Fig. 6. Transfer characteristics of narrowed $Si_{0.7}Ge_{0.3}$ FinFET.

The key electrical property of the narrowed $Si_{0.7}Ge_{0.3}$ FinFET is compared with those of some reported SiGe FinFET/GAA devices.[3,17–23] Figure 7 summarizes the SS-I_{ON}/I_{OFF} benchmark of the reported SiGe FinFET/GAA devices. The I_{ON}/I_{OFF} ratio of the narrowed $Si_{0.7}Ge_{0.3}$ FinFET is higher than the average value of the comparison groups. Its SS is the smallest in SiGe FinFETs and comparable to that of the SiGe GAA device. This result proves that the cyclic wet treatment after dummy gate removal is a promising technology to further improve the gate control of $Si_{0.7}Ge_{0.3}$ FinFET. In addition, this novel wet treatment process can also provide a potential solution for realizing SiGe fins with different widths on the same wafer after introducing an additional mask.

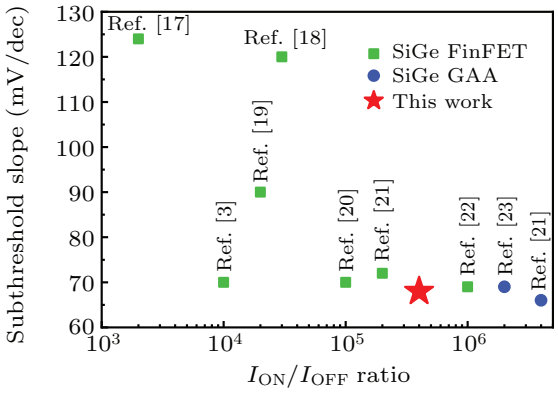


Fig. 7. The SS–I_{ON}/I_{OFF} benchmarks with reported SiGe FinFET/GAA devices.

4. Conclusions

In this work, a narrowed $Si_{0.7}Ge_{0.3}$ FinFET device with a stronger gate control capability is presented by utilizing a precise cyclic wet treatment process, which is based on a self-limited oxidation and removal technology in each cycle. This cyclic wet treatment after dummy gate removal is a promising technology to further enhance the gate control of $Si_{0.7}Ge_{0.3}$ FinFET.

Acknowledgement

Project supported by the Beijing Municipal Natural Science Foundation, China (Grant No. 4202078).

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