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Design optimization of a silicon-germanium heterojunction negative capacitance gate-all-around tunneling field effect transistor based on a simulation study

Weijie Wei(魏伟杰), Weifeng Lü(吕伟锋)†, Ying Han(韩颖), Caiyun Zhang(张彩云), and Dengke Chen(谌登科)

School of Microelectronics, Hangzhou Dianzi University, Hangzhou 310018, *China*

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The steep sub-threshold swing of a tunneling field-effect transistor (TFET) makes it one of the best candidates for low-power nanometer devices. However, the low driving capability of TFETs prevents their application in integrated circuits. In this study, an innovative gate-all-around (GAA) TFET, which represents a negative capacitance GAA gate-to-source overlap TFET (NCGAA-SOL-TFET), is proposed to increase the driving current. The proposed NCGAA-SOL-TFET is developed based on technology computer-aided design (TCAD) simulations. The proposed structure can solve the problem of the insufficient driving capability of conventional TFETs and is suitable for sub-3-nm nodes. In addition, due to the negative capacitance effect, the surface potential of the channel can be amplified, thus enhancing the driving current. The gate-to-source overlap (SOL) technique is used for the first time in an NCGAA-TFET to increase the band-to-band tunneling rate and tunneling area at the silicon–germanium heterojunction. By optimizing the design of the proposed structure via adjusting the SOL length and the ferroelectric layer thickness, a sufficiently large on-state current of 17.20 μA can be achieved and the threshold voltage can be reduced to 0.31 V with a sub-threshold swing of 44.98 mV/decade. Finally, the proposed NCGAA-SOL-TFET can overcome the Boltzmann limit-related problem, achieving a driving current that is comparable to that of the traditional complementary metal–oxide semiconductor devices.

Keywords: negative capacitance (NC), gate-all-around (GAA), silicon-germanium heterojunction, gate-to-source overlap (SOL)

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1. Introduction

Currently, reducing the power consumption of complementary metal–oxide semiconductor (CMOS) integrated circuits is an urgent problem that needs to be solved. One way to achieve this is to design CMOS devices with good switching characteristics that are defined by sub-threshold swing (*SS*).[1] The *SS* of a conventional metal–oxide–semiconductor field-effect transistor (MOSFET) cannot be lower than 60 mV/decade due to the Boltzmann limit defined by its conduction mechanism.[2,3] A negative capacitance field-effect transistor (NCFET) can meet this requirement because of the negative capacitance (NC) effect of ferroelectric materials.[4] Due to the NC effect, an NCFET can amplify the surface potential of the channel to increase the channel current.[5] Another promising solution to the aforementioned problem could be to use a tunneling field-effect transistor (TFET), which generates the current by injecting charge carriers from the source into the channel via band-to-band tunneling.[6] TFETs can easily obtain a sub-60 mV/decade *SS*. However, the TFETs have a low off-state current (I_{OFF}) and on-state current (I_{ON}), which results in poor driving capability.[7] To overcome this limitation, materials with a narrow band gap and high carrier mobility, such as germanium (Ge) and indium arsenide (InAs), could be used to form a heterojunction. A heterojunction can improve the band-to-band tunneling rate, thus increasing the channel current.[8,9] For sub-3-nm node devices, replacing the fin-type field-effect transistor with a gate-all-around (GAA) structure can further suppress the short-channel effect because of the improved gate control ability.[10–12]

In previous studies, NCGAA-TFETs were created by connecting a ferroelectric capacitor in series with a metal gate of a GAA-TFET.[13,14] Similarly, other studies used MATLAB simulations to combine the Landau–Khalatnikov equation with a GAA-TFET device model.[15] These techniques make the NCGAA-TFET ideal because they cannot reflect the ferroelectric material deposition on the oxide layer well. In addition, while depositing several materials between the oxide layer and the gate metal can improve device performance, it can also increase the fabrication complexity.[16] Furthermore, the vertical tunneling rate and tunneling area of an NC-TFET can be improved by partially moving the gate to the source, thus increasing the channel current.[17–20] In addition, the gate-to-drain extension can improve the bipolar effect of a double-gate tunneling field-effect transistor.[21] Moreover, the inner gate, outer gate, and gate–source overlap can be used to improve the electrical performance of a device, but this makes its structure complex.[22] Moreover, applying the gate-source overlap to a line TFET can also improve the analog performance.[23] However, many of the TFET structures de-

†Corresponding author. E-mail: lvwf@hdu.edu.cnn

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signed to enhance the channel current use compounds in heterojunctions, which increase the CMOS process complexity.

In this work, a GAA-TFET is combined with the NC effect, silicon–germanium (SiGe) heterojunction, and gate-to-source overlap (SOL), and a comprehensive investigation and analysis are conducted on the proposed NCGAA-SOL-TFET structure. The proposed structure can effectively increase the driving current and improve electrical performance. In addition, the electrical performance of the device can be easily optimized by adjusting the SOL length (L_{SOL}) and the thickness of the ferroelectric layer (T_{FE}).

2. Proposed structure design and simulations

A schematic of an NCGAA-SOL-TFET is presented in Fig. 1(a), where the thicknesses of HfO_2 (T_{OX}) and the ferroelectric layer (T_{FE}) are 1 nm and 4 nm, respectively; the channel length (L_G) is 15 nm; the source length (L_S) and drain length (L_D) are 20 nm; the radii (R) of the source, channel, and drain are 5 nm; and the gate-to-source overlap length (L_{SOL}) is 3 nm. The GAA-TFET is selected as a baseline device and used for performance comparison; its schematic is presented in Fig. 1(b). Germanium with a band gap of 0.66 eV is used as the source material, and silicon with a band gap of 1.12 eV is used as the construction material of the channel and drain; thus, a heterojunction is formed between the source and the channel. The doping concentrations of the source, channel, and drain are 1×10^{20} cm^{-3}, 1×10^{15} cm^{-3}, and 2×10^{19} cm^{-3}, respectively. The device structural parameters and process parameters are in accordance with the IRDS More Moore 2021 version for a 3-nm node.[24]

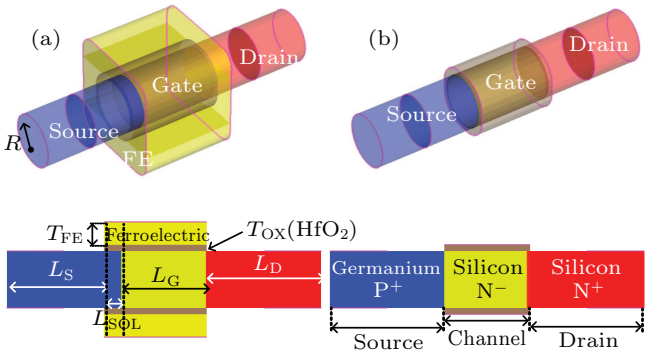


Fig. 1. (a) The NCGAA-SOL-TFET with SiGe heterojunction, SOL, and ferroelectric layer; (b) the GAA-TFET as a baseline device.

Furthermore, zirconium-doped hafnium dioxide (HZO) is used as a ferroelectric layer between the metal gate and the oxide layer. The material parameters of the HZO layer are as follows: $\alpha = -3\sqrt{3}E_c/(4P_r)$, $\beta = 3\sqrt{3}E_c/8P_r^3$, and $\gamma = 5\times10^{25}$ cm$^9\cdot$F$\cdot$C^{-4}, where the coercive electric field (E_c) is 1 MV/cm, and the remanent polarization (P_r) is 5 μC/cm^2.[25,26] The matching between ferroelectric capacitance ($C_{FE} = 2/3\sqrt{3}\times P_r/E_c\times T_{FE}$), oxide layer capacitance (C_{OX}), and transistor capacitance (C_{MOS}) is essential for exhibiting the hysteresis-free NC effect, and the condition of $C_{MOS} < |C_{FE}| < C_{OX}$ should be satisfied.[27,28] If C_{MOS} and C_{total} represent the total capacitance of the baseline device and its NC counterpart after stacking the ferroelectric material,[29] then it holds that

$$C_{total} = C_{MOS}\times\frac{C_{FE}}{C_{FE}+C_{MOS}}. \tag{1}$$

Excellent capacitance matching can be achieved when $C_{total} \gg C_{MOS}$, and this condition should be considered in device design and optimization. As shown in Fig. 2, C_{total} is larger than C_{MOS}, and peak capacitance occurs at a smaller V_{GS}. This indicates that the ferroelectric layer has exhibited a hysteresis-free NC effect. However, when V_{GS} is larger than V_{DS}, C_{total} is less than C_{MOS}, indicating that the capacitance C_{FE} does not match C_{MOS}.

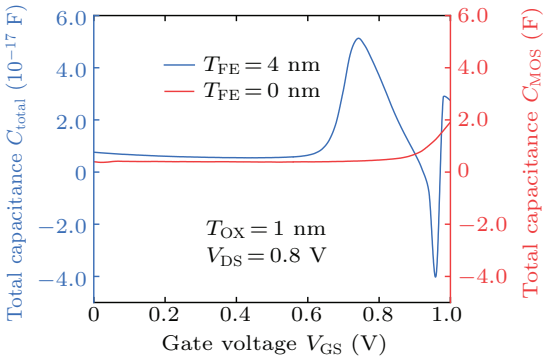


Fig. 2. The total capacitance for $T_{FE} = 4$ nm and $T_{FE} = 0$ at $T_{OX} = 1$ nm.

The channel current in the TFET is mostly generated by the band-to-band tunneling of carriers, which mainly occurs at the heterojunction formed at the interface between the source and the channel. When the conduction band in the channel is lower than the valence band in the source, the probability of carrier tunneling is increased. Thus, carrier tunneling mainly occurs in the region between the valence band of the source and the conduction band of the channel. Under the condition of a uniform electric field, G_{BTBT} denotes the band-to-band tunneling rate of the carrier, which is derived from the Kane model[30,31] as follows:

$$G_{BTBT} = \frac{A_k|E|^\theta}{\sqrt{E_g}}\exp\left(-B_k\frac{E_g^{\frac{3}{2}}}{|E|}\right), \tag{2}$$

where A_k, B_k, and θ are the tunneling parameters of the material; A_k and B_k are 4×10^{14} cm$^{-3}\cdot$s^{-1} and 1.9×10^7 V/cm for silicon and 9.1×10^{16} cm$^{-3}\cdot$s^{-1} and 4.9×10^6 V/cm for germanium, respectively; E is the electric field intensity under the current tunnel volume; and E_g is the band gap. In the technology computer-aided design (TCAD) simulations, the Fermi–Dirac distribution model is used for a high doping concentration, and the hydrodynamic model is employed

for nanodevices. The other models used in the TCAD simulations include the carrier high electric field velocity saturation model, the scattering model, the band gap narrowing model under high doping concentration, the SRH recombination model, the Auger recombination model, and the Landau–Khalatnikov ferroelectric equation. In addition, the nonlocal band-to-band tunneling model is used to judge the tunneling area based on the local variation in the energy band. The application of the listed physical models makes simulations conducted in this study more accurate and reliable. In addition, as shown in Fig. 3, the simulated transfer characteristics (I_{DS}–V_{GS} curve) of the GAA-TFET are calibrated using previous experimental data.[32]

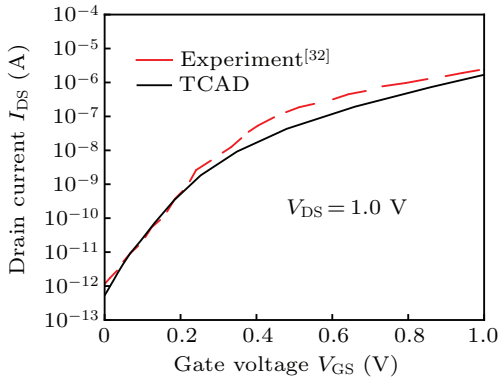


Fig. 3. Calibration of the I_{DS}–V_{GS} curve using the experimental data.

3. Results, analysis and discussion

3.1. Source overlap effect on device performance

The energy band diagrams of the GAA-TFET in the off state ($V_{GS} = 0$, $V_{DS} = 0.8$ V) are presented in Fig. 4(a). In this state, the valence band of the source is lower than the conduction band of the channel. Therefore, the band-to-band tunneling rate is low, and only a few electrons will tunnel into the channel to form the off-state current (I_{OFF}). The energy band in the on state ($V_{GS} = 1.0$ V, $V_{DS} = 0.8$ V), where the valence band of the source is higher than the conduction band of the channel, is presented in Fig. 4(b). Thus, a large number of electrons will tunnel into the channel to form the on-state current (I_{ON}). The transfer characteristics of the GAA-SOL-TFET are presented in Fig. 5(a), where it can be seen that when L_{SOL} increases, I_{ON} also increases. When L_{SOL} is larger than 1 nm, the sub-threshold current of the GAA-SOL-TFET is smaller than that of its GAA-TFET counterpart. However, as L_{SOL} increases, the increase in the saturation current is reduced. Furthermore, when the gate extends toward the source, the electric field on the left side of the heterojunction increases, as shown in Fig. 5(b). Moreover, the energy bands of the source–channel interface and the left side of the source–channel interface bend, which improves the band-to-band tunneling area and tunneling rate, increasing the current. When L_{SOL} increases to 5 nm, the current almost reaches the saturation level. As shown in Fig. 6, with the increases in L_{SOL}, the electric field is mainly concentrated on the gate corner edge, which decreases the electric field intensity at the heterojunction center. As a result, the tunneling area and the area of the region with a high tunneling rate stop increasing when $L_{SOL} > 5$ nm. The band-to-band tunneling generation rate and tunneling area along the central section of the GAA-SOL-TFET are presented in Fig. 7. As shown in Fig. 7, due to the effect of the electric field edge, when L_{SOL} increases, the area with a high band-to-band tunneling rate is gradually concentrated on the heterojunction surface. This reduces the band-to-band tunneling rate at the heterojunction center so that the channel current stops increasing gradually. In addition, with the energy band bending on the left side of the source–channel interface, the width of the depletion region of the heterojunction increases, thus increasing the total capacitance (C_{MOS}), as shown in Fig. 8. The tunneling junction is equivalent to a reverse-biased diode. When the gate voltage is large enough, a large number of carriers will accumulate in the channel, and the C_{MOS} will be dominated by these carriers. However, the carriers that dominate the current are those that tunnel from the source to the channel.[9]

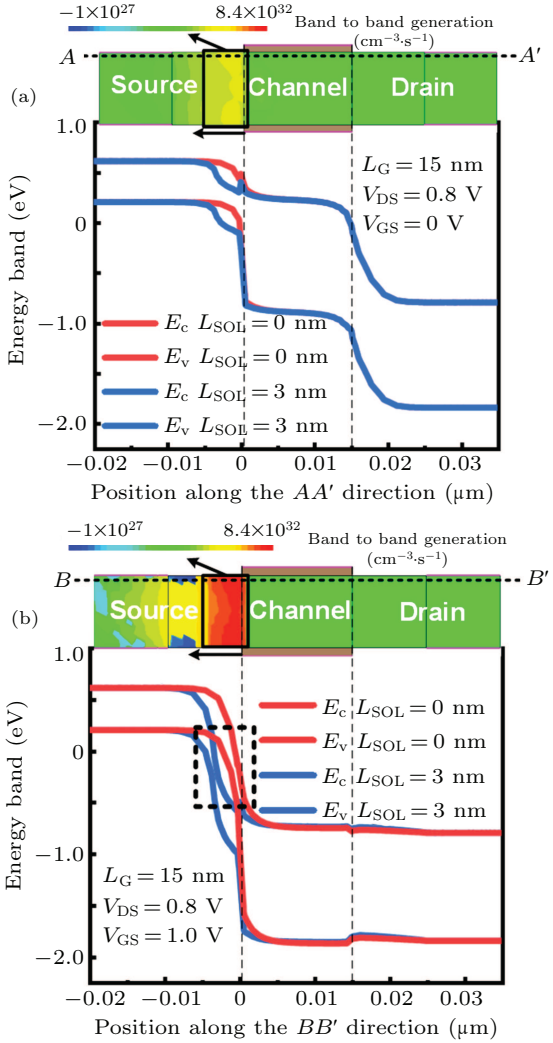


Fig. 4. Band diagrams of the GAA-TFET and GAA-SOL-TFET: (a) off state; (b) on state.

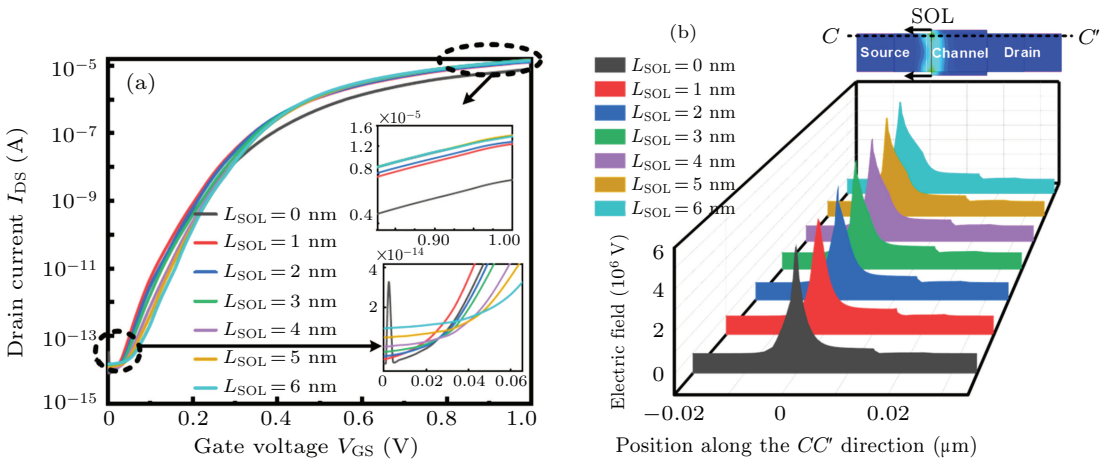


Fig. 5. (a) Transfer characteristics of the GAA-SOL-TFET at different L_{SOL} values; (b) variations in the electric field intensity of the GAA-SOL-TFET at different L_{SOL} values.

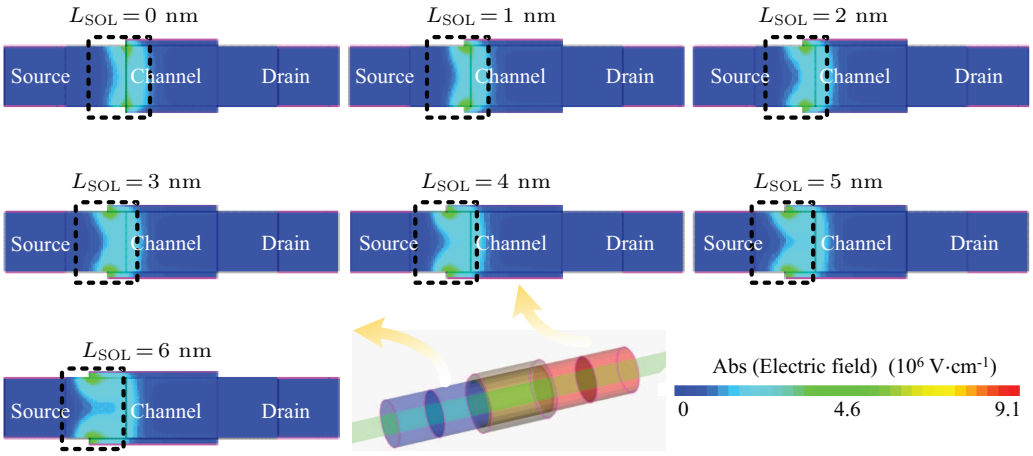


Fig. 6. The electric field intensity of the GAA-SOL-TFET at different L_{SOL} values.

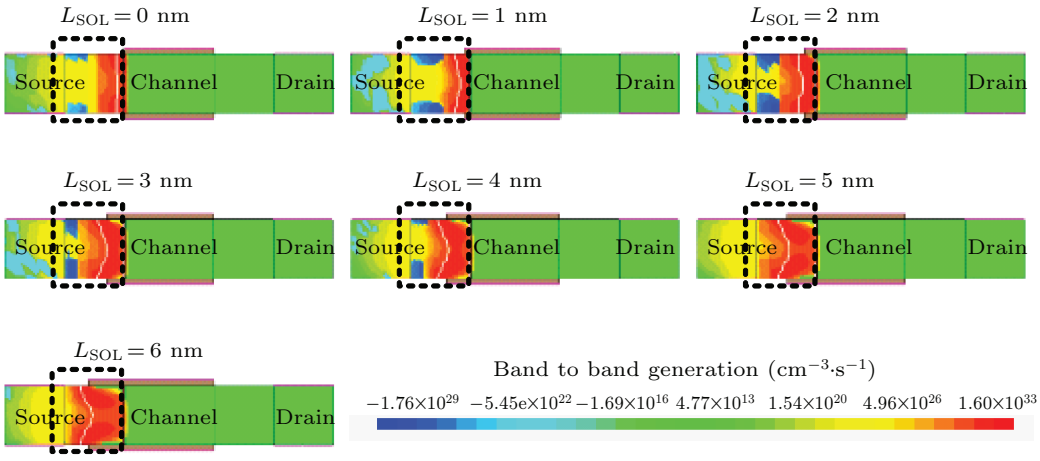


Fig. 7. The band-to-band generation tunneling and tunneling area of the GAA-SOL-TFET at different L_{SOL} values.

Therefore, C_{MOS} and channel current are not dominated by the same group of carriers, which is the main difference between the TFET and the MOSFET. As shown in Fig. 9, when L_{SOL} increases, although the *SS* of the device gradually increases, it still remains below 60 mV/decade. A steeper I_{DS}–V_{GS} curve indicates a faster device switching speed, indicating a smaller *SS*. In Fig. 5(a), it can be observed that the I_{DS}–V_{GS} curves at $L_{SOL} = 1$ nm and $L_{SOL} = 2$ nm are steeper than that of $L_{SOL} = 0$. However, at $L_{SOL} > 2$ nm, the I_{DS}–V_{GS} curve becomes flatter than that at $L_{SOL} = 0$. Therefore, at $L_{SOL} = 1$ nm and $L_{SOL} = 2$ nm, the *SS* is smaller than at $L_{SOL} = 0$, but it becomes larger when $L_{SOL} > 2$ nm. In addition, the threshold voltage (V_{th}) increases when L_{SOL} is less than 4 nm but decreases when L_{SOL} is larger than 4 nm while

still staying lower than that of the baseline device. Considering V_{th}, I_{ON}/I_{OFF}, and *SS*, the GAA-SOL-TFET achieves its optimal performance at $L_{SOL} = 3$ nm.

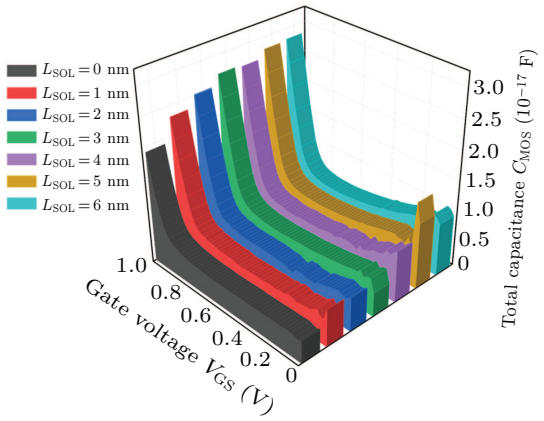


Fig. 8. The total capacitance of the GAA-SOL-TFET versus L_{SOL}.

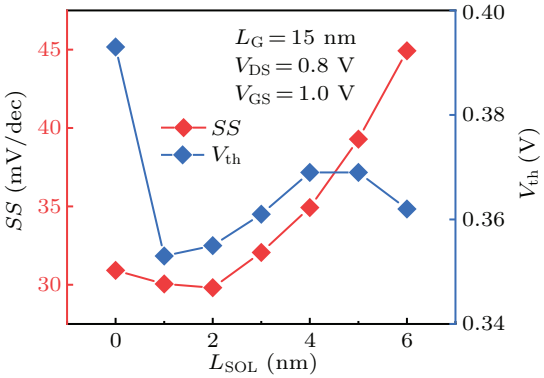


Fig. 9. The *SS* value versus L_{SOL} value; when L_{SOL} increases, the *SS* of the GAA-SOL-TFET increases but remains below 60 mV/decade. The V_{th} of the GAA-SOL-TFET fluctuates in a small range as L_{SOL} increases.

3.2. NCGAA-SOL-TFET design optimization

The variations in the channel surface potential at different T_{FE} values are presented in Fig. 10. As shown in Fig. 10, the surface potential in the NCGAA-SOL-TFET channel is amplified compared to that of the GAA-SOL-TFET.[33] The total capacitance increases due to the increase in L_{SOL}, which makes the capacitance-matching process more complex. As presented in Fig. 10, the potential amplification of the channel surface is almost the same at $T_{FE} < 4$ nm. This indicates that in the NCGAA-SOL-TFET, a larger T_{FE} amplifies the channel surface potential obviously.

The I_{DS}–V_{GS} curves of the NCGAA-SOL-TFET at different T_{FE} values are presented in Fig. 11(a). As shown in Fig. 11(a), in the subthreshold region, the I_{OFF} gradually improves with the increase in T_{FE}, except for $T_{FE} = 1$ nm. However, as T_{FE} increases, the variation trend of the saturation current becomes non-monotonic with V_{GS} when $V_{GS} > V_{DS}$. When $T_{FE} < 3$ nm, the saturation current increases slightly with V_{GS}, while it decreases at $T_{FE} = 5$ nm. At $T_{FE} = 4$ nm, the saturation current increases monotonically and obviously. The main reason for this can be found using Fig. 11(b) and formula (1). When V_{GS} is small, the change of C_{total} at $T_{FE} = 1$ nm fluctuates, indicating that the capacitance matching becomes poor. When V_{GS} is larger than V_{DS}, at $T_{FE} > 2$ nm, the C_{total} of the NCGAA-SOL-TFET is smaller than that of the GAA-TFET, which indicates poor capacitance matching. As shown in Fig. 12(a), for the NCGAA-SOL-TFET, the changes in the *SS* and V_{th} values show opposite trends when T_{FE} increases; namely, the *SS* first decreases and then increases, whereas the V_{th} first increases and then decreases. The reason for this change can be observed in Fig. 11(a). The results indicate that the I_{DS}–V_{GS} curve is the steepest at $T_{FE} = 0$, so the *SS* is the smallest at $T_{FE} = 0$. Moreover, the I_{DS}–V_{GS} curves at $T_{FE} = 1$ nm and $T_{FE} = 5$ nm are almost the flattest among all the curves.

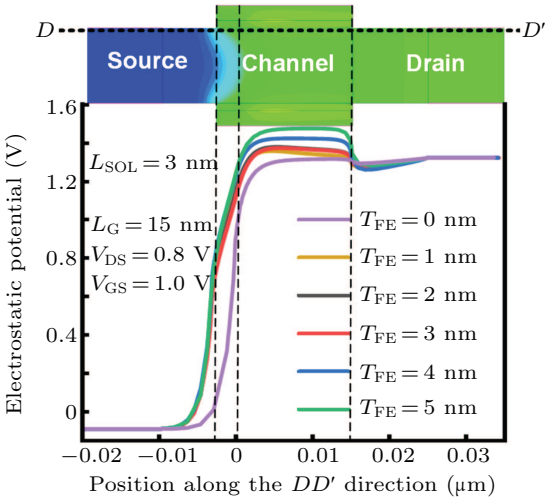


Fig. 10. Variations in channel surface potential in the NCGAA-SOL-TFET under different T_{FE} values.

As shown in Fig. 12(b), both I_{ON} and the peak-transconductance of the NCGAA-SOL-TFET are improved compared to the other devices, and the peak-transconductance appears at a lower gate voltage. The electrical characteristics in Table 1 show that I_{ON} and the peak-transconductance of the NCGAA-SOL-TFET are 2.32 times and 2.11 times larger than those of the other devices, respectively. In addition, V_{th} drops from 0.39 V to 0.31 V. It should be noted that both the NC effect and the SOL can enhance the driving capability, but the *SS* of the NCGAA-SOL-TFET is slightly larger than that of the GAA-TFET, resulting in a reduced I_{ON}/I_{OFF}. Therefore, different optimized designs should be used for different performance requirements. The GAA-SOL-TFET is suitable for devices with good switching performance, whereas the NCGAA-SOL-TFET is suitable for devices with a high driving current and a low threshold voltage.

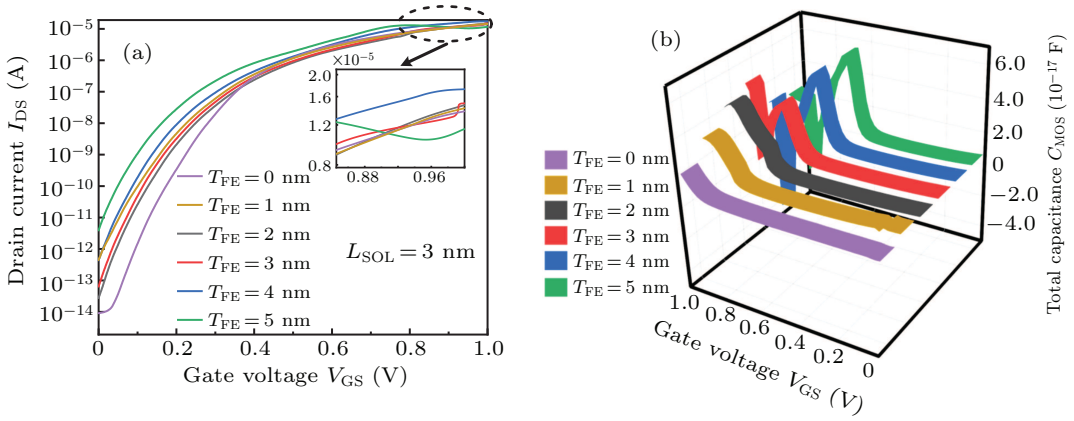


Fig. 11. (a) The I_{DS} of the NCGAA-SOL-TFET versus V_{GS} under different T_{FE} values; (b) C_{total}–V_{GS} characteristics of the NCGAA-SOL-TFET at L_{SOL} of 3 nm and T_{FE} of 0, 1 nm, 2 nm, 3 nm, 4 nm, and 5 nm.

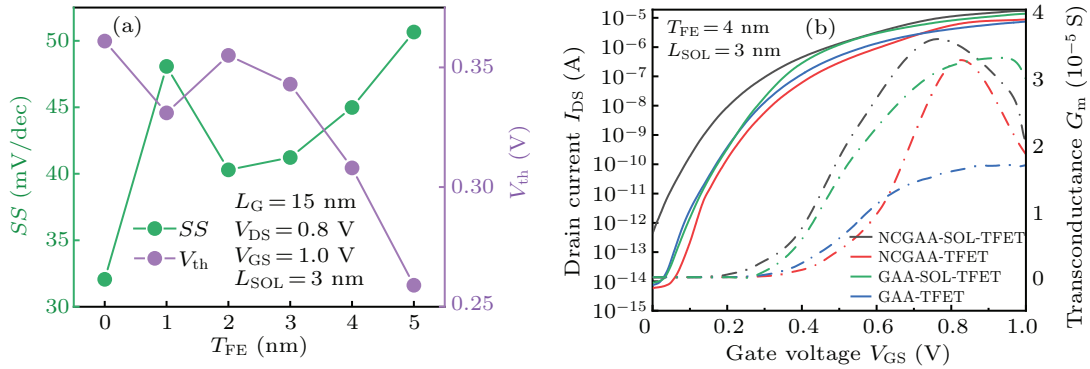


Fig. 12. (a) Changing trends of the SS and V_{th} at different T_{FE} values; (b) I_{DS}–V_{GS} and G_m–V_{GS} curves of the GAA-TFET, GAA-SOL-TFET, NCGAA-TFET, and NCGAA-SOL-TFET.

Table 1. Electrical performance comparison results of different devices.

Parameter (unit)	GAA-TFET	GAA-SOL-TFET	NCGAA-TFET	NCGAA-SOL-TFET
T_{FE} (nm)	0	0	4	4
L_{SOL} (nm)	0	3	0	3
I_{ON} (μA)	7.40	13.7	8.79	17.20
I_{ON}/I_{OFF}	10^9	1.52×10^9	1.47×10^9	3.99×10^7
SS (mV/dec)	30.14	30.06	34.30	44.98
G_m (S)	1.67×10^5	3.27×10^5	3.23×10^5	3.54×10^5
V_{th} (V)	0.39	0.36	0.43	0.31

4. Conclusion

This study proposes the NCGAA-SOL-TFET structure and performs a comprehensive investigation of the proposed structure via TCAD simulations. The results indicate that the NC effect on the silicon–germanium heterojunction and the gate-to-source overlap increase the band-to-band tunneling rate and tunneling area of the source–channel interface, increasing the device current. Thus, in the proposed structure, the problem of the insufficient driving capability of the TFET is effectively solved. In the NCGAA-SOL-TFET structure, changing the gate-to-source overlap length will affect the NC matching and dynamic response characteristics. Therefore, the SOL length and the ferroelectric layer thickness should be considered in the device design. In addition, the proposed structure can improve the driving ability of the GAA-TFET by design optimization. However, the improvement in driving ability may be at the cost of sub-threshold leakage, although the sub-threshold swing of the NCGAA-SOL-TFET is still less than 60 mV/decade. In summary, the proposed NCGAA-SOL-TFET can achieve both high driving ability and low sub-threshold swing, which makes it suitable for future low-power circuit applications.

Acknowledgements

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