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Research on self-supporting T-shaped gate structure of GaN-based HEMT devices

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A self-supporting T-shaped gate (SST-gate) GaN device and process method using electron beam lithography are proposed. An AlGaN/GaN high-electron-mobility transistor (HEMT) device with a gate length of 100 nm is fabricated by this method. The current gain cutoff frequency (f_T) is 60 GHz, and the maximum oscillation frequency (f_{max}) is 104 GHz. The current collapse has improved by 13% at static bias of (V_{GSQ}, V_{DSQ}) = (−8 V, 10 V), and gate manufacturing yield has improved by 17% compared with the traditional floating T-shaped gate (FT-gate) device.

Keywords: GaN, high-electron-mobility transistor (HEMT), self-supporting, T-gate

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1. Introduction

GaN high-electron-mobility transistor (HEMT) has a large band gap, high electron saturation velocity, high two-dimensional electron gas concentration at the heterojunction interface, high breakdown voltage, and high thermal conductivity. This series of characteristics makes it widely recognized in the fields of high frequency, high power, high temperature, and so on. Through the aggressive gate length scaling, the f_T and f_{max} of GaN HEMT have been continuously improved.[1–3] In practice, when the gate length is reduced below 100 nm, the parasitic RC charging delay caused by drain/source resistances and gate extrinsic capacitance can account for a significant fraction of the total delay.[4] To avoid this, floating T-shaped gate (FT-gate) has been widely used. The small size of the FT-gate can improve the frequency characteristics of the device, and the larger gate cap can ensure gate parasitic resistance at a low level.[5–11] The gate cap "floats" above the heterojunction and the medium is air, which effectively reduces the gate extrinsic capacitance.

With the continuous gate length scaling, the large gate cap is more and more mismatched, which presents a challenge to the stability of the gate and the yield of the gate fabrication.[12–15] This is crucial to radio frequency (RF) power applications with large gate widths. One common way is to form a dielectric layer (usually SiN) before the gate, forming a surface passivation and providing mechanical support. But this brings an enormous gate parasitic capacitance[16] and it is usually used in high-power and relatively low-frequency situations. Meanwhile, to improve the gate's mechanical stability, Matsumoto[17] improved the stability of the gate by placing a dielectric layer with spacing between the gate and the barrier layer. This scheme greatly increases the parasitic capacitance, resulting in a sharp deterioration of frequency performance. Wang[18] proposed a Π-type gate to increase the stability of the gate while improving the cutoff frequency. However, the gate has a greater influence on the channel scattering, which will affect the frequency performance of the device. Deng *et al.*[19] developed a 10-nm-thick T-shaped gate anchored by an Si_3N_4 sheath for high mechanical reliability, but the operating frequency is reduced by 17% compared with the conventional T-shape gate due to the existence of the sheath. Song *et al.*[20] investigated the fringing capacitance on a 40-nm T-gate device with low-*k* (SiON) gate dielectric and found that the gate extrinsic capacitance contributes approximately 50% of the total delay. As seen above, the difficulty is to achieve gate self-support without causing large gate parasitic capacitance.

This paper reports an SST-gate with gate pillars along the gate width without additional process. The gate pillars are only partially present along the gate width, so it only slightly reduces the frequency performance due to the low duty ratio of the gate pillar. At the same time, the SiN passivation layer outside the gate region is preserved, which can achieve good current collapse and avoid the gate parasitic effect. The result of yield shows that mechanical stability is significantly improved. These results also provide new ideas for realizing the device structure and process optimization.

2. Device fabrication

In this work, the epilayer on the sapphire substrate consisted of a 24-nm-thick AlGaN barrier layer. The sheet resistance was 369.5 Ω/□ and mobility was 1620 $cm^2 \cdot V^{-1} \cdot s^{-1}$.

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The source electrode and drain electrode were deposited from Ti/Al/Ni/Au, and rapidly annealed at 840 °C under the protection of N_2 atmosphere for 60 s. The ohmic contact resistance was 0.42 Ω·mm. Then the device was isolated by MESA etching and then passivated by a 60-nm-thick SiN layer. To suppress the gate parasitic capacitance, a 350-nm-long SiN layer was etched near the gate. And finally, the SST-gate with Ni/Au (45 nm/400 nm) was fabricated. As shown in Fig. 1(a), the gate length is 100 nm, the gate cap is 900 nm, the gate foot height is 200 nm, and source–drain spacing is 3 μm. An FT-gate device with the same dimensions was fabricated for comparison as indicated in Fig. 1(b).

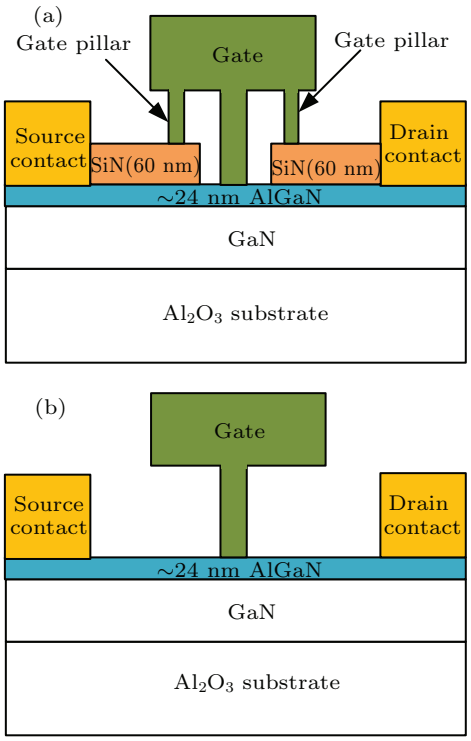


Fig. 1. Device structure diagram of (a) SST-gate and (b) FT-gate.

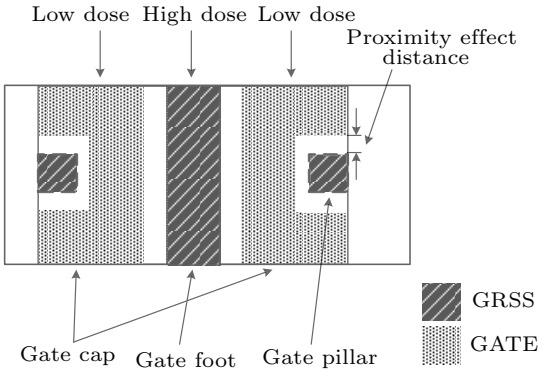


Fig. 2. Layout design of SST-gate.

The specific method of the SST-gate is shown as follows. Based on our previous fabrication process of FT-gate,[13] the SST-gate process used PMMA/PMMA-MA/PMMA-MA three-layer electron-beam resist process, which can complete the gate lithography by only one exposure and one development. The bottom PMMA layer required high dose exposure to make the small gate pillar and the gate foot. The upper two PMMA-MA layers needed to be exposed to a low dose to define the gate cap. To avoid exposure expansion caused by the proximity effect introduced by the difference in sharp dose between the two layers, a distance between the two exposure areas was set in layout as shown in Fig. 2. Then the SST-gate is formed by metal evaporation and lift-off. Since the gate pillars of the SST occupy only a small portion, the structure does not interfere with the lift-off effect (see Fig. 3).

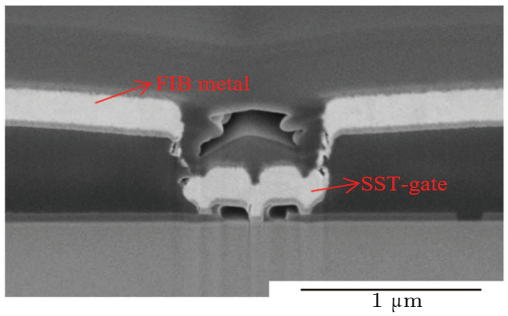


Fig. 3. FIB image of the cross-section of SST-gate.

3. Results and discussion

The DC characterization of the device with different gate pillar duty ratios is performed by a Keithley 4200-SCS semiconductor parameter analyzer. For the duty ratio of the gate pillar:

$$R = \frac{L_{\mathrm{gp}} \times N}{W_{\mathrm{g}}},$$

where R is the duty ratio of the gate pillar, L_{gp} is the length of the gate pillar, N is the number of gate pillars, and W_{g} is the length of the gate width.

The measured transfer characteristics of the devices are shown in Fig. 4, where the drain bias is 10 V and the gate is changed from 2 V to −8 V in steps of −0.1 V. It can be seen from Fig. 4(a) that all the SST-gate devices are about 40 mS/mm lower than the FT-gate device. And the g_{m} of the SST-gate device does not change obviously with the increase of duty ratio. So the main reason is the SiN passivation in the SST-gate device, which will cause the square resistance of the material to increase, thus enhancing the source resistance (R_{s}) and leading the non-intrinsic transconductance of the SST-gate device to decrease.

Figure 4(b) shows the change of breakdown voltage (V_{BV}) with gate duty ratio at a gate bias of −8 V. It can be seen that the gate leakage current gradually increases with the augment of the duty ratio of the pillar. As is well known, the SiN passivation brings about additional leakage current path. The gap between the gate and the SiN region can prevent the SiN leakage path from appearing in the SST-gate device. However,

there are contacts between gate pillars and the SiN layer, so the gate leakage current increases gradually with the increase of pillar duty ratio. Meanwhile, the gate leakage current of SST-gate device with low R is even lower than that of the FT-gate device. The assumed reason is the over-etching of SiN in the SST-gate device. It is equivalent to injecting a certain dose of F plasma into the larger area near the gate, thereby suppressing the gate leakage current of SST-gate devices to a certain extent.

In Fig. 4(b), it is also found that when I_{DS} is in the range of 10^{-2} mA/mm–1 mA/mm, the V_{BV} of the SST-gate device is significantly lower than that of the FT-gate device, and the V_{BV} is not obviously affected by the duty ratio of the pillar. We presume that this is also due to the SiN passivation layer in the SST-gate, which brings about an additional leakage path and reduces the V_{BV}. When I_{DS} reaches 10 mA/mm, the V_{DS} values of all devices gradually tend to be the same. The I_{DS} at this time is mainly the leakage current of the buffer layer. The buffer layer leakages of the two kinds of devices are comparable as their drain–source spaces are the same.

Figure 5 shows the cross-sections of electric field distribution from a three-dimensional (3D) Silvaco-TCAD simulation of the two devices at off-state ($V_{GS} = -6$ V and $V_{DS} = 10$ V). Although the gate pillars act as field plates and suppress the electric field beneath, the electric field intensity under the gate pillar area is very intense, which is more likely to generate leakage current through the SiN layer compared with other areas, resulting in breakdown voltage drop.

Figure 6 shows the comparison of pulsed I–V measured curves of current collapse between the two gates. The devices are tested on a Keithley 4200SCS semiconductor parameter analyzer. Static bias for pulse testing of devices is set at $(V_{GSQ}, V_{DSQ}) = (-8\text{ V}, 0\text{ V})$ and $(-8\text{ V}, 10\text{ V})$. The gate pulse voltage is selected as 2 V, and the drain pulse voltage is from -10 V to 0 V in steps of 0.2 V. Pulse cycle is 0.5 ms, and the pulse width is set to 0.5 μs, 1 μs, 5 μs, 10 μs, 50 μs. With the increase of pulse width, the current collapse decreases. This is because if the pulse width is long enough, some trapped electrons will have enough time to release the electrons, and the released electrons will recover the current to a certain extent, reducing the current collapse. Meanwhile, the current dispersion of FT-gate device without SiN passivation is serious, while the current dispersion of SST-gate device with the SiN passivation layer is well improved. It indicates that the retention of the SiN passivation layer can effectively reduce the surface trap and improve the current collapse caused by the surface trap.

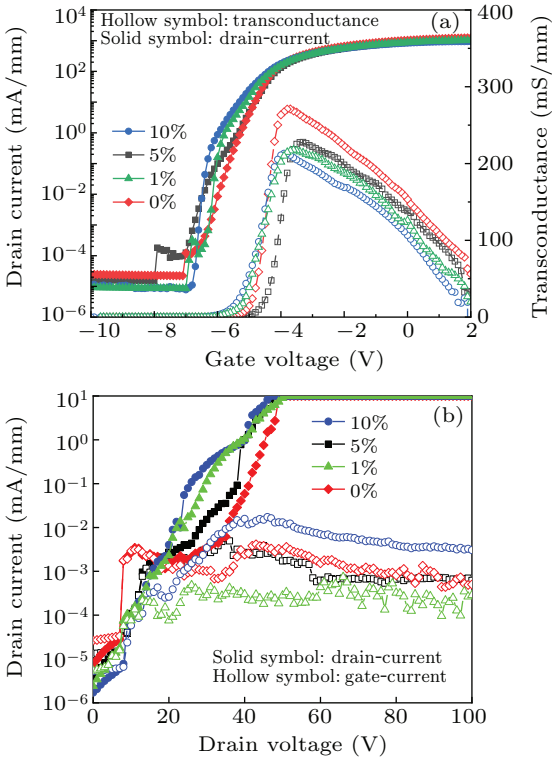


Fig. 4. DC characteristics of SST-gate devices with different gate pillar duty ratios: (a) transfer and (b) breakdown characteristic.

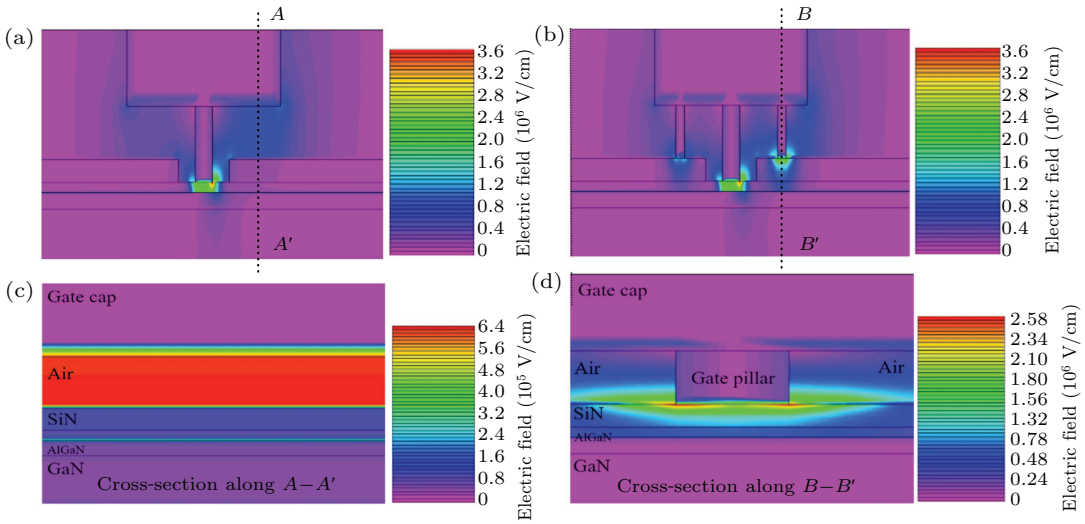


Fig. 5. Cross-section of electric field distribution of (a) FT-type gate device and (b) SST-type gate device.

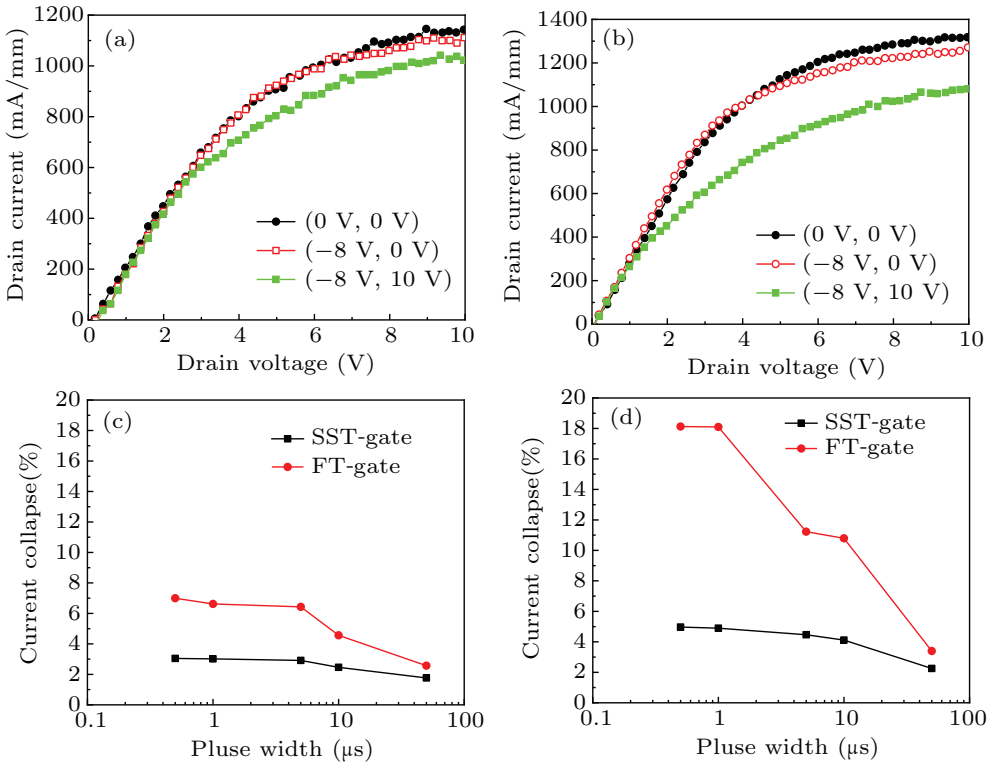


Fig. 6. Comparison of pulsed *I*–*V* tests for two devices: (a) SST-gate with 0.5-μs pulse width, (b) T-gate with 0.5-μs pulse width, (c) current collapse at (−8V, 0 V), and (d) current collapse at (−8 V, 10 V).

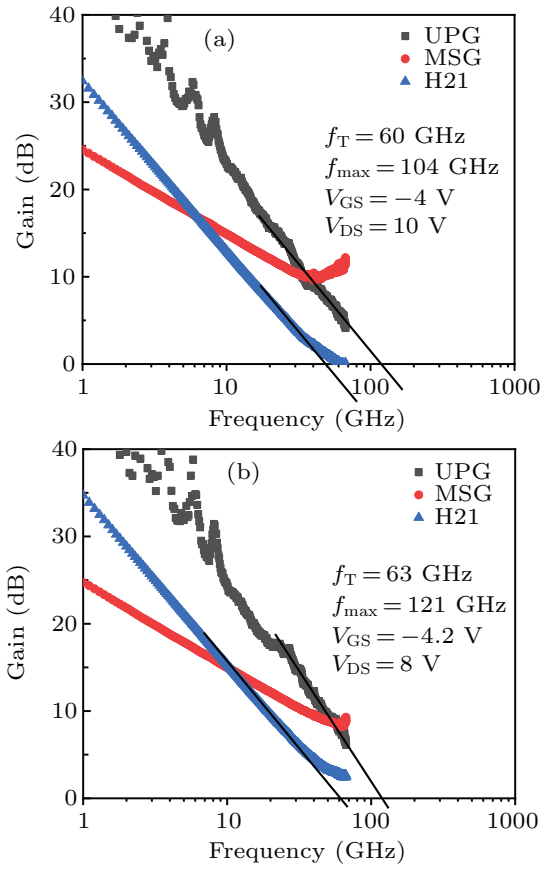


Fig. 7. Small signal characteristics of (a) the SST-gate and (b) the FT-gate.

Figure 7(a) shows the RF characteristics of the 100-nm SST-gate device with 1% duty ratio of the gate pillar measured under the bias condition: $V_{DS} = 10$ V and $V_{GS} = -4$ V. Simultaneously, high f_T/f_{max} of 60 GHz/104 GHz are obtained by extrapolating the current gain ($|h_{21}|^2$) and unilateral power gain (UPG), respectively, by using a −20 dB/decade slope. Similarly, the f_T/f_{max} of the FT-gate device is 63 GHz/121 GHz under the bias condition: $V_{DS} = 8$ V and $V_{GS} = -4.2$ V in Fig. 8(b). The slight decline in the frequency performance of the SST-gate device is caused by the slight decrease of g_m. Relatively, the f_{max} is more affected by the SST-gate device because f_{max} reflects the influence of parasitic parameters and there is greater parasitic capacitance around the gate pillar. In summary, the SST-gate device achieves essentially the same frequency performance as the SiN-free FT-gate device due to the low duty ratio of the gate pillar and the removal of SiN around the gate.

The reliabilities of the two gate structures are analyzed statistically on 144 devices in 12 dies. Among them, 72 FT-gate devices and 72 SST-gate devices are fabricated. In the case of an FT-gate, the small gate foot may not be able to support the large grid cap, causing the gate to collapse. This causes the gate to fail to control the two-dimensional electron gas underneath, resulting in poor transforming characteristics of the device. Therefore, the criterion for judging the reliability of the gate is as follows: I_{DS} reaches below 1 mA/mm at −10 V V_{GS} at off-state, and the g_m reaches above 100 mS/mm at on-state. Among the 144 devices, the FT-gate device has 42 devices (58%) that meet the criterion, and the SST-gate device has 54 (75%) devices that meet the criterion, as shown in

Fig. 8. The yield of the SST-gate device is improved by 17% compared with that of FT-gate device.

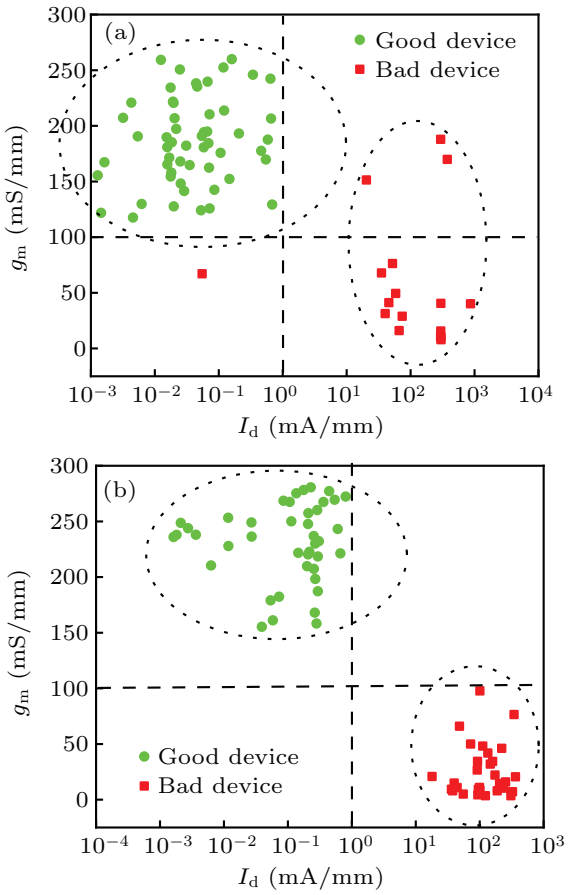


Fig. 8. Key parameter test results of (a) SST-gate and (b) FT-gate.

4. Conclusions and perspectives

In the present work, a method of fabricating the self-supporting floating T-gate by electron beam lithography is proposed. The results show that due to the novel self-supporting and partially passivated SiN structure, the mechanical stability of the T-gate and the current collapse effect of the AlGaN/GaN HEMT device are significantly improved, and the SST-gate device at gate pillar duty ratio of 1% can achieve almost unaffected frequency performance in comparison with the FT-gate device. This provides a feasible solution to improve the floating T-gate stability of the GaN-based HEMT devices.

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