Design and research of normally-off β-Ga_2O_3/4H-SiC heterojunction field effect transistor

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Ga_2O_3 is difficult to achieve p-type doping, which further hinders the development of Ga_2O_3-based power devices and is not conducive to the development of new devices with high power density and low power consumption. This paper expounds a β-Ga_2O_3/4H-SiC heterojunction lateral metal–oxide–semiconductor field-effect transistor (HJFET), which can make better use of the characteristics of PN junction by adding p-doped SiC in the channel region. Compared with the conventional devices, the threshold voltage of the heterojunction metal–oxide–semiconductor field-effect transistor (MOSFET) is greatly improved, and normally-off operation is realized, showing a positive threshold voltage of 0.82 V. Meanwhile, the off-state breakdown voltage of the device is up to 1817 V, and the maximum transconductance is 15.3 mS/mm. The optimal PFOM is obtained by simulating the thickness, length and doping of the SiC in each region of the epitaxial layer. This structure provides a feasible idea for high performance β-Ga_2O_3 MOSFET.

Keywords: MOSFET, heterojunction, threshold voltage

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1. Introduction

Gallium oxide (BGO), as a recently emerging power semiconductor, occupies a place in the fields of high power,[1] high temperature,[2] and high voltage.[3–5] These all benefit from the theoretical high critical breakdown electric field of 8 MV/cm,[6] ultra-wide bandgap of 4.5 eV–4.9 eV and high Baliga's figure of merit (3444).[7] In addition to these unique advantages, gallium oxide can also achieve controllable n-type doping of 10^{15} cm^{-3}–10^{20} cm^{-3} as well as semi-insulating properties through Si, Ge, Sn.[8] The successful acquisition of large diameter gallium oxide substrates in the molten state has made gallium oxide ready for mass production and cost-effective.

Although gallium oxide material has great advantages, the current research of Ga_2O_3 MOSFETs is mostly depletion mode (D-mode),[9–14] and the research on enhancement mode (E-mode) has only increased in recent years. At the same time, the ultra-wide bandgap and flat valence band make it easy for holes to form strong local polarons or self-trapped holes, which makes the p-type doping of Ga_2O_3 difficult to achieve.[15]

Many efforts have been made to realize E-mode devices, including the optimization of device structures, process and the use of heterojunctions. In terms of device structure and process, wrap-gate fin-array,[16] recessed gate,[17,18] vertical structure,[19] double gate structure,[20] current aperture,[21] oxygen annealing,[22] VLD structure,[7] *etc*. the use of these methods can shift the threshold voltage to the right to a certain extent, but some complex structures and processes will cause certain difficulties in production. Compared with structural optimization, the introduction of p-type doping materials can increase the turn-on voltage of the device without increasing the conduction loss, such as BP/β-Ga_2O_3,[23] graphene-gate/β-Ga_2O_3,[24] h-BN/β-Ga_2O_3,[25] SnO/β-Ga_2O_3,[26] *etc*.

So far, the material properties of Ga_2O_3 devices are still far from the critical value, and further improvement is required. Based on this, a Ga_2O_3 heterojunction metal–oxide–semiconductor field-effect transistor (HJFET) is proposed by selectively adding SiC in the epitaxial layer. To verify the validity of the proposed structure, the electrical properties of heterojunction transistor and conventional transistor (CONV) were investigated. And the device parameters are optimized, such as the length (L_{SiC}), thickness (T_{SiC}) of SiC and doping concentration of epitaxial layer. It is expected that the proposed structure can cause the threshold voltage to shift to the right and realize the design of E-mode devices, which provides a new idea for the design of subsequent normally-off device.

2. Devices structure and simulation

Figure 1 is the schematic cross-sectional view of the designed device, a homoepitaxial gallium oxide thin film layer on an Fe-doped (010) β-Ga_2O_3 substrate, including a 250-nm unintentionally doped buffer layer and a 240-nm epitaxial layer. The thickness of the gate oxide layer is 30 nm, the source–drain distance (L_{sd}), gate length (L_g), and gate–drain distance (L_{gd}) are designed to be 12 μm, 2 μm, and 8 μm respectively. Si^+ implantation was used to form ohmic contacts

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and reduce device resistance, and an unintentionally doped Ga_2O_3 buffer layer was used to reduce implant damage to the substrate and subsequent Fe out-diffusion.[27]

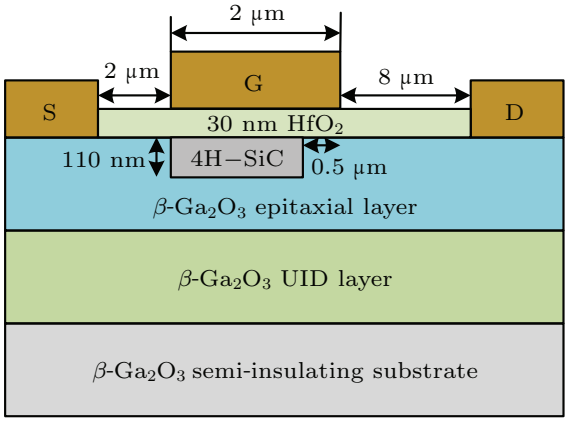


Fig. 1. Schematic cross-section of a β-Ga_2O_3/SiC HJFET.

Due to the lack of an accurate material model for Ga_2O_3, experimental data from literature were used in the simulation process. The dielectric constant is 10, and the mobility model has a great influence on the current transport process in the semiconductor, mainly including the doping dependence, the high field saturation (Caughey–Thomas model)[28] and enormal, which the doping dependence uses the Arora model.[29] For the computational efficiency in simulation, regardless of the impact ionization model, when the critical breakdown electric field of β-Ga_2O_3 is reached, the voltage in the channel is extracted as the breakdown voltage, which is consistent with the results reported by literature.[7]

3. Heterojunction principle

The electron affinities of β-Ga_2O_3 and 4H-SiC are 4.0 eV and 3.45 eV,[7] and the bandgaps are 4.85 eV and 3.3 eV.[30] Therefore, the offset discontinuity at the bottom of the conduction band is 0.55 eV and the offset at the top of the valence band is 2.1 eV. Figure 2(b) is an energy band diagram of β-Ga_2O_3/SiC heterojunction under thermal equilibrium. In the heterojunction, since the barrier height of electrons in β-Ga_2O_3 entering p-type SiC is 0.55 eV and the height of the barrier for holes to move to β-Ga_2O_3 is 2.1 eV, so the electrons of β-Ga_2O_3 are easier to enter into the SiC, resulting in the electrons playing a major role.

Due to the concentration difference between electrons and holes, a space charge region is formed near the interface between the P and N regions, and the thickness of the space charge region is related to the doping concentration. There is an internal electric field in the space charge area. In order to form a current in the PN junction, the resistance of the internal electric field in the space charge area must be eliminated. Therefore, an external electric field can be applied to offset the built-in electric field, so that the carrier can continue to move and form a linear positive current.

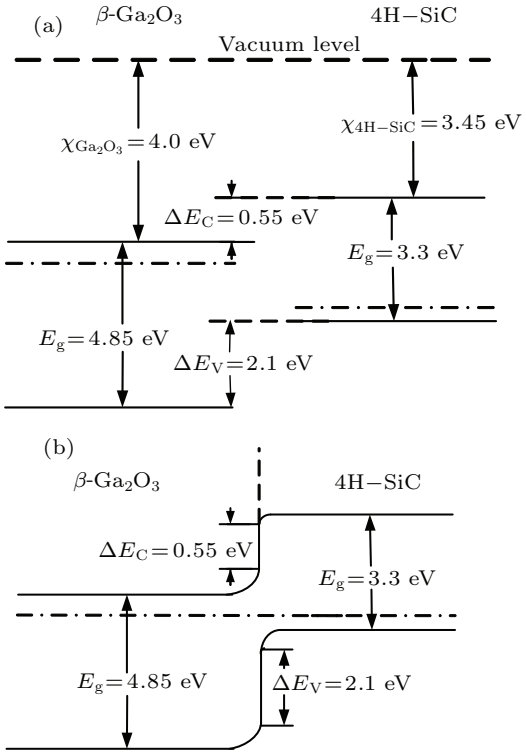


Fig. 2. (a) Band alignment of isolated β-Ga_2O_3 and 4H-SiC, (b) energy band diagram of β-Ga_2O_3/SiC heterojunction under thermal equilibrium.

4. Results and discussion

In addition to the P region, the traditional device structure and doping concentration used for simulation are completely the same as the proposed new device structure. The transfer characteristic curves of the conventional structure and the heterojunction device are shown in Fig. 3. It can be clearly seen that the threshold voltage of HJFET reaches 0.82 V, which is mainly due to the p-type doping that makes the electrons in the channel region are in a fully depleted state under zero bias. The built-in electric field can be offset by applying a positive gate voltage, which makes the depletion region thinner and the device opens. Figure 3(b) shows the transfer characteristic curve in logarithmic state. It can be seen that the current on/off ratio of the device is more than 10^9, and the maximum transconductance is 15.3 mS/mm.

Figure 4 shows the output characteristic curve of the heterojunction device. During the output characteristic test, the drain bias (V_{ds}) increases from 0 V to 30 V, the gate bias (V_{gs}) increases from 1 V to 7 V with a step size of 1 V. As can be seen from Fig. 4, the device exhibits a good pinch-off characteristic. When the gate bias is 7 V, the drain–source saturation current reaches 63 mA/mm. The electric field distribution of the transistor under V_{ds} = 1500 V and V_{gs} = 0 V shows in Fig. 5(a), ensuring that the device is in the off state.

The figure shows that the peak electric field of the heterojunction device reaches 7.46 MV/cm, which is lower than the critical breakdown electric field of Ga_2O_3 material. Figure 5(b) shows the relationship between the peak electric field and the drain–source voltage of the device after adding the heterojunction. Since the impact ionization model is not considered, the corresponding voltage when the breakdown electric field is 8 MV/cm is extracted. The breakdown voltage of the heterojunction MOSFET is 1817 V.

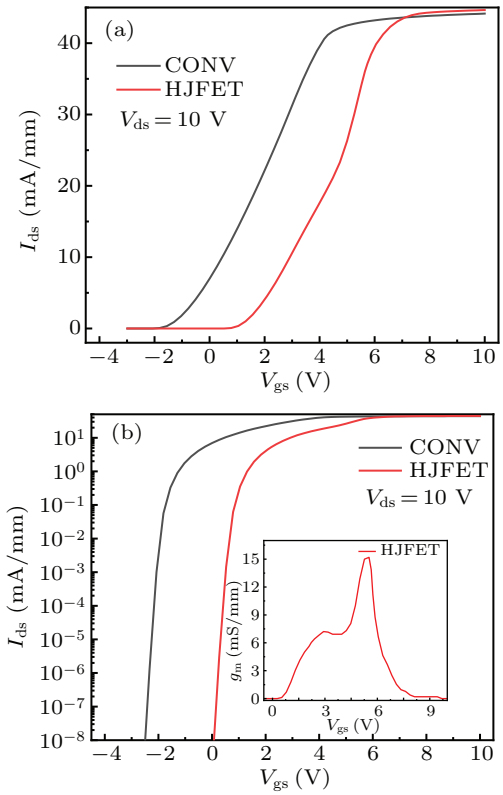


Fig. 3. Simulation results of transfer characteristics (a) line and (b) semi-logarithmic, the inset shows g_m–V_{gs} characteristics of HJFET.

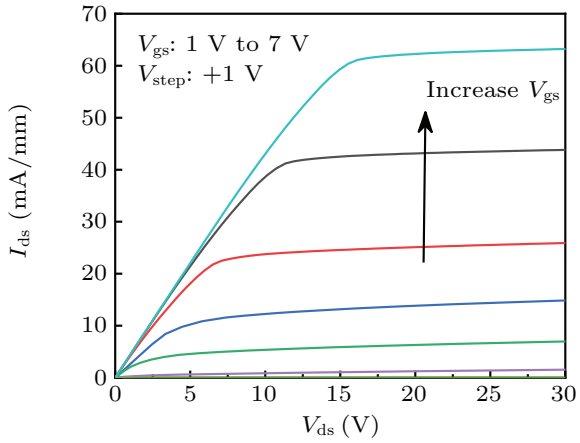


Fig. 4. Output characteristic curve of HJFET.

In the process of device design, the performance and PFOM of the device should be improved as much as possible. The expression of PFOM is[31]

$$\mathrm{PFOM} = \frac{V_{\mathrm{br}}^2}{R_{\mathrm{on,sp}}}, \tag{1}$$

where $R_{\mathrm{on,sp}}$ is the specific on-state resistance, and V_{br} is the breakdown voltage. The depletion region is particularly important for device turn-on and withstand voltage. The expression of the depletion width at the PN junction is

$$W = \sqrt{\frac{2\varepsilon_{\mathrm{s}}(N_{\mathrm{A}} + N_{\mathrm{D}})V_{\mathrm{D}}}{qN_{\mathrm{A}}N_{\mathrm{D}}}}, \tag{2}$$

where N_{A} and N_{D} represent the acceptor impurity and donor impurity respectively, V_{D} is the voltage at the edge of region N, and ε_{s} is the capacitance rate of the semiconductor. The length, thickness of SiC and doping concentration of the epitaxial layer have obvious effects on the breakdown voltage and on-resistance, so these parameters are optimized. Subsequent optimizations are carried out on the basis of the previous one.

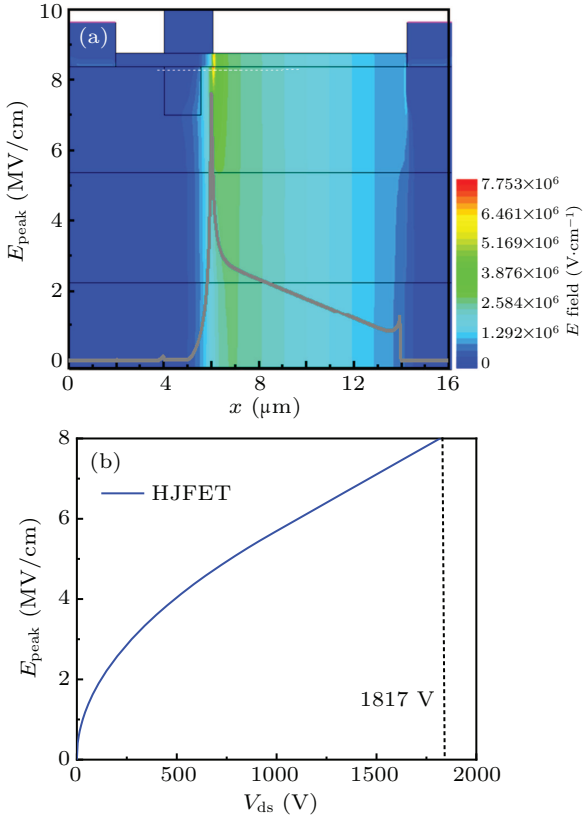


Fig. 5. HJFET (a) electric field distribution under V_{ds} = 1500 V and (b) peak electric field versus V_{ds}.

As shown in Fig. 6(a), the characteristics of different SiC lengths are compared. With the increase of L_{SiC}, the channel resistance of the device increases under the same cross-sectional area,[32] so the channel current decreases. The larger channel resistance is, the more difficult it is for the device to turn on. As the length of SiC increases, the threshold voltage first increases and then gradually becomes saturated. There is a PN junction at the edge of the SiC near the drain. As the length of SiC increases, the PN junction is close to the drain. Due to the voltage drop in the channel, as the length of the SiC increases, the reverse voltage applied to the PN junction is greater and the depletion region widens, resulting

in a higher breakdown voltage. With the further increase of the SiC, the depletion region begins to decrease, which leads to the decrease of the breakdown voltage, so it has the lowest breakdown voltage. Figure 6(b) shows the corresponding PFOM of different SiC lengths. The inset shows the relationship between breakdown voltage, $1/R_{on,sp}$, and L_{SiC}, when $L_{SiC} = 1.5$ μm, the maximum PFOM is reached, the peak electric field appears in Ga_2O_3, and the max electric field in SiC is 1.06 MV/cm, which is lower than the theoretical critical field strength (2.5 MV/cm).[33,34]

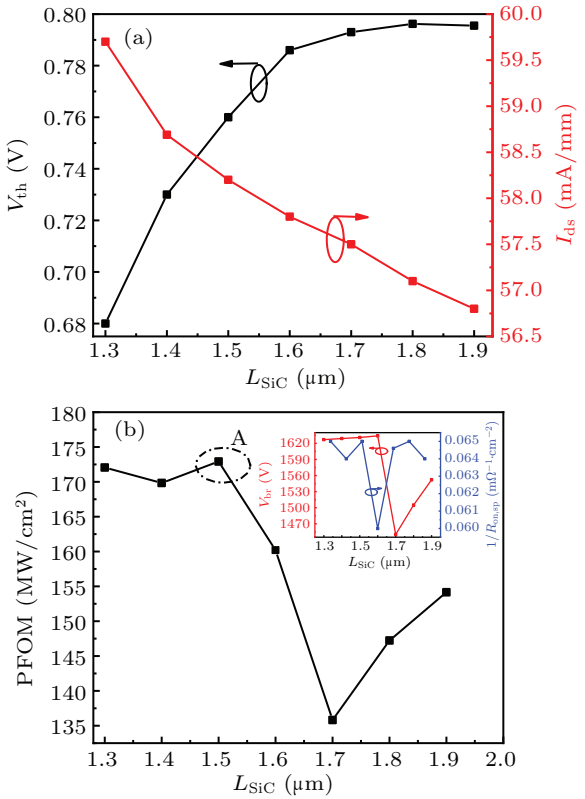


Fig. 6. (a) Characteristics comparison and (b) PFOM under different L_{SiC}, the inset shows the relationship between V_{br}, $1/R_{on,sp}$, and L_{SiC}.

When the thickness and concentration of SiC are low, the Ga_2O_3 in the channel is not completely depleted, and the device itself has a conductive channel, so the specific on-resistance increases slightly with the increase of thickness and concentration. As the thickness and concentration of SiC increase, Ga_2O_3 is completely depleted at a certain gate voltage, making it easier to create a inversion layer and making the conductive channel wider, so the specific resistance decreases. When reaching a certain extent, the depletion region is no longer widened, and the specific on-resistance changes little.

Figure 7 shows the PFOM for different T_{SiC}, the highest PFOM is at point B, so the best thickness of the SiC is 0.11 μm. As the thickness of this region increases, a larger gate voltage is required to make the device form an inversion layer, so the threshold voltage will continue to increase. But the increased thickness will also reduce I_{ds}, and the appropriate thickness of SiC is critical.

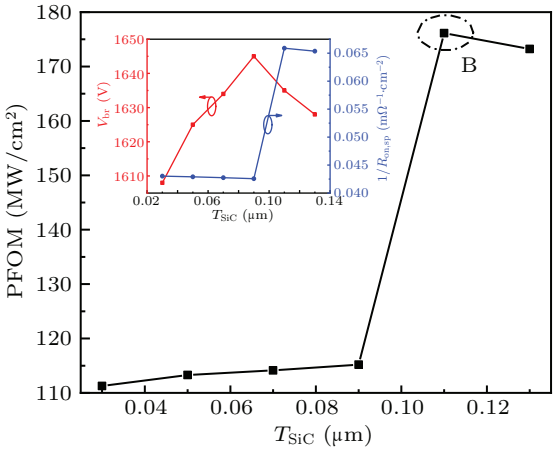


Fig. 7. PFOM at different T_{SiC}.

The doping concentration of the epitaxial layer changes the saturation current by affecting the mobility. Figure 8(a) shows the transfer characteristic curves under different doping concentrations of Ga_2O_3 epitaxial layer. At the same drain voltage, with the doping concentration of the epitaxial layer increases, the threshold voltage decreases and the drain–source current increases, which indicates that the on-resistance decreases, so the increase of doping concentration in this region can reduce the conduction loss.

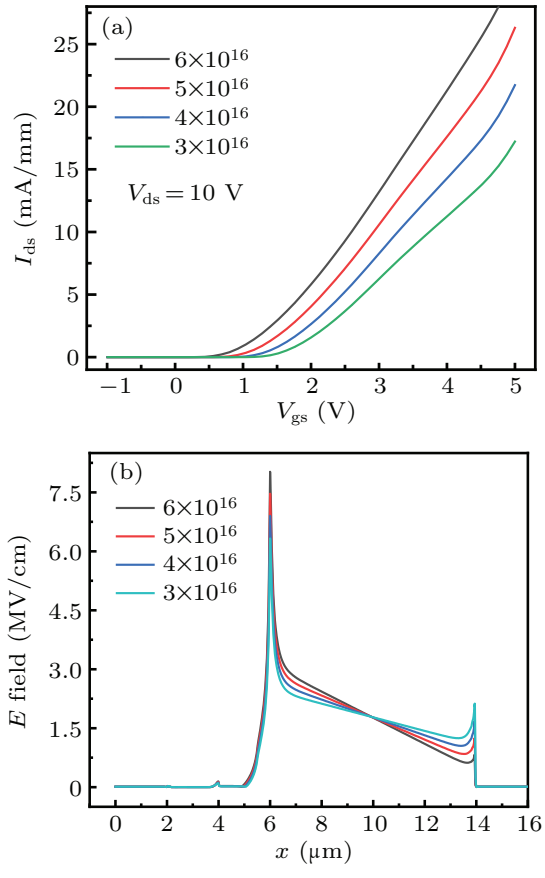


Fig. 8. (a) Transfer characteristic curves and (b) electric field distribution at the interface between the channel and oxide layer under the different doping of epitaxial layer.

Figure 8(b) shows the electric field distribution at different doping concentrations of the epitaxial layer when the drain–source voltage is 1500 V. It is necessary to ensure that the device is in the off state, and the gate close to the drain side will generate a peak electric field. The closer to the gate oxide layer, the greater the peak value of the electric field. Therefore, the electric field distribution under 2 nm on the channel surface is selected. With the decrease of the doping concentration of this region, the peak electric field is reduced to a certain extent, and the electric field at the edge of the drain is increased, which can achieve the effect of averaging electric field distribution. Mainly due to the reduction of the doping concentration in epitaxial layer, the depletion region continues to widen toward the drain to withstand a higher voltage, so a lower doping concentration in this region can achieve a higher breakdown voltage. The peak electric field corresponding to 3×10^{16} cm^{-3} is 6.4 MV/cm, which is the lowest electric field.

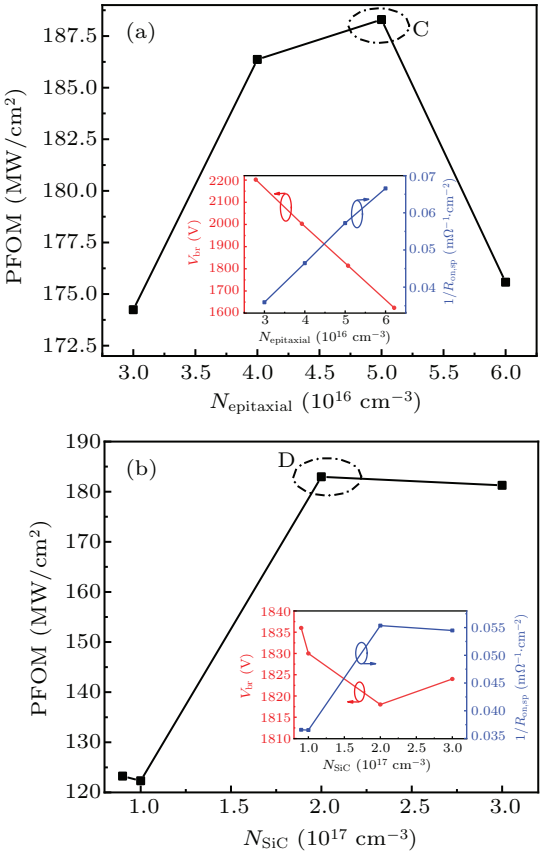


Fig. 9. PFOM under different doping concentrations: (a) epitaxial layer and (b) SiC, the inset shows the effect of doping concentration on $V_{\rm br}$ and $1/R_{\rm on,sp}$.

Figure 9 shows the PFOM under different doping concentrations, where the inset shows the effect of doping concentration on breakdown voltage and $1/R_{\rm on,sp}$. It can be seen from Fig. 9(a) that the highest PFOM is at point C, the corresponding doping concentration is 5×10^{16} cm^{-3}. Compared with other values, the resistance decreases to a large extent, and the breakdown voltage decreases to a relatively small degree, so a larger PFOM can be achieved. Figure 9(b) shows the effect of the doping concentration of the SiC on the PFOM. With the increase of the doping concentration in this region, the breakdown voltage has a small change, which is attributed to the doping of the P region. The increase of the concentration leads to the narrowing of the space charge region on this side, and the effect on the breakdown voltage becomes smaller.

By comparing the simulation results, it can be concluded that HJFET has the highest PFOM when the length of SiC layer is 1.5 μm, the thickness is 0.11 μm, the doping concentration of epitaxial layer is 5×10^{16} cm^{-3}, and the doping concentration of SiC is 2×10^{17} cm^{-3}.

5. Conclusion

In summary, a β-Ga_2O_3/4H-SiC heterojunction metal–oxide–semiconductor field-effect transistor is proposed, which makes full use of the switching and breakdown characteristics of the PN junction. By comparing the relevant parameters of the epitaxial layer, the best results are obtained, *i.e.*, the forward movement of the threshold voltage and a larger breakdown voltage are realized. Finally, the device achieves a turn-on voltage of 0.82 V, a breakdown voltage of 1817 V, and a maximum transconductance ($g_{\rm m}$) of 15.3 mS/mm. The results show that the addition of heterojunction can improve the performance of the device, providing a reliable solution for device optimization.

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