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Citation: Chin. Phys. B, 2023, 32 (**7**): 078504. DOI: 10.1088/1674-1056/ac9cbb
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Chin. Phys. B, 2018, 27 (**7**): 078502. DOI: 10.1088/1674-1056/27/7/078502

High on-state current p-type tunnel effect transistor based on doping modulation

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(Received 8 July 2022; revised manuscript received 22 September 2022; accepted manuscript online 21 October 2022)

To solve the problem of the low on-state current in p-type tunnel field-effect transistors (p-TFETs), this paper analyzes the mechanism of adjusting the tunneling current of a TFET device determined by studying the influence of the peak position of ion implantation on the potential of the p-TFET device surface and the width of the tunneling barrier. Doping-regulated silicon-based high on-state p-TFET devices are designed and fabricated, and the test results show that the on-state current of the fabricated devices can be increased by about two orders of magnitude compared with the current of other devices with the same structure. This method provides a new idea for the realization of high on-state current TFET devices.

Keywords: tunnel field-effect transistors (TFET), band-to-band tunneling (BTBT), on-state current, doping modulation

PACS: 85.30.Mn, 85.40.Ry, 73.40.Gk **DOI:** 10.1088/1674-1056/ac9cbb

1. Introduction

With the development of integrated circuits, power consumption has become a serious problem.[1] Compared with metal–oxide–semiconductor field-effect transistors, tunnel field-effect transistors (TFETs) have a lower power consumption that can significantly reduce the power loss of integrated circuits.[2] Although much research has been carried out on TFET devices in recent years, TFETs still have the problem of a low on-state current; this has become one of the key issues limiting the development of TFET devices.[3]

In recent years, researchers have fabricated n-TFET devices with higher currents by optimizing TFET devices,[4–6] and their on-state currents can reach up to 10^{-5} A·μm^{-1}.[7,8] However, the characteristics of p-TFETs are not as good as those of n-TFETs. The reason for this is that the tunneling probability is related to the effective carrier mass, and the effective carrier mass of holes is larger than that of electrons, resulting in a smaller tunneling probability for holes than electrons.[9] In order to enhance the on-state current, researchers have optimized the structure of p-TFET devices, proposing various structures such as U-type and L-type[10–13] or using heterojunction structures to optimize the devices.[14,15] Although these structures enhance the on-state current of the devices, the complex preparation process not only increases the cost but can also lead to degradation of device reliability. This means that TFET devices face reliability problems in practical applications, thus limiting their development.

In this paper the effect of the depth of the peak position of ion implantation concentration ($D_{\rm peak}$) on the on-state current of p-TFET devices is investigated. Technology computer aided design (TCAD) software is used to simulate the potential distribution and the minimum tunneling barrier width ($W_{\rm min}$) at the device surface under different values of $D_{\rm peak}$ so as to clarify its influence on the on-state current of the p-TFET device. Subsequently, a high on-current p-TFET device based on doping control was fabricated by using the ion implantation barrier layer to control $D_{\rm peak}$. The test results show that the on-state current of the fabricated p-TFET device is significantly improved compared with other devices with the same structural parameters.

2. Mechanism of the effect of source region doping on device on-state current

The turn-on current of a TFET depends on the tunneling probability at the tunneling junction when the device is on. The source doping profile affects the potential (or electric field) at the tunneling junction, which determines the tunneling probability of the TFET in the on-state, as shown in Eq. (1).[9] The impurity distribution in the source region can be divided into vertical distribution and lateral diffusion distribution, both of which have different effects on device characteristics. There have been many studies on lateral diffusion distribution, and the design of various structures is mainly focused on the regulation of lateral distribution,[16] but the mechanism of the influence of vertical distribution of impurities in

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the source region on TFET devices is still unclear. According to the principle of the tunneling effect, the tunneling conditions are that there are carriers on one side of the barrier and the other side of the barrier has energy levels corresponding to energy states that are not occupied by carriers, as well as a sufficiently narrow barrier width and strong electric field strength.[17] The electric field intensity at the device surface is maximum when the field-effect device is operating,[9] but the longitudinal distribution of impurities formed by ion injection satisfies a Gaussian distribution and the peak location is not at the semiconductor surface;[18] this leads to non-optimal control efficiency of the electric field on the tunneling junction. TCAD was used to simulate the effect of D_{peak} on the potential distribution, as shown in Fig. 1(a). For larger values of D_{peak} the potential of the device surface changes more slowly due to the gate bias, and the electric field strength at the tunnel junction is also smaller. It can be known from Eq. (1)[9] that when the electric field strength at the tunneling junction is smaller, the probability of tunneling is lower. This is unfavorable for increasing the tunneling current, so D_{peak} should be reduced to increase the electric field strength near the surface of the device and increase the tunneling probability of the device in the on-state.

$$T_{\text{tunnel}} = \exp\left(-\frac{4\sqrt{2m^*}E_{\text{g}}^{2/3}}{3q\hbar E}\right). \tag{1}$$

Here T_{tunnel} is the tunneling probability, E is the electric field strength, E_{g} is the band gap of the semiconductor, m^* is the effective carrier mass, q is the charge constant and $\hbar$ is the approximate Planck constant.

As the peak position of ion implantation approaches the surface, the potential change at the surface is steeper, and the tunneling barrier W_{min} also becomes narrower. As shown in Fig. 1(b), when the ion implantation peak position is closer to the surface, the width of the tunneling barrier near the surface decreases significantly, and the tunneling electric field increases. Since the tunneling current is positively related to the tunneling probability, as shown in Eq. (2),[19] the tunneling current is proportional to the negative exponential power of the tunneling barrier width. When the width of the tunneling barrier is reduced, the tunneling electric field is enhanced, and the tunneling current will be significantly improved.

$$I_{\text{BTBT}} \propto T_{\text{tunnel}} \propto \text{e}^{-W_{\text{min}}}. \tag{2}$$

Here I_{BTBT} is the tunneling current, T_{tunnel} is the tunneling probability and W_{min} is the minimum tunneling barrier width.

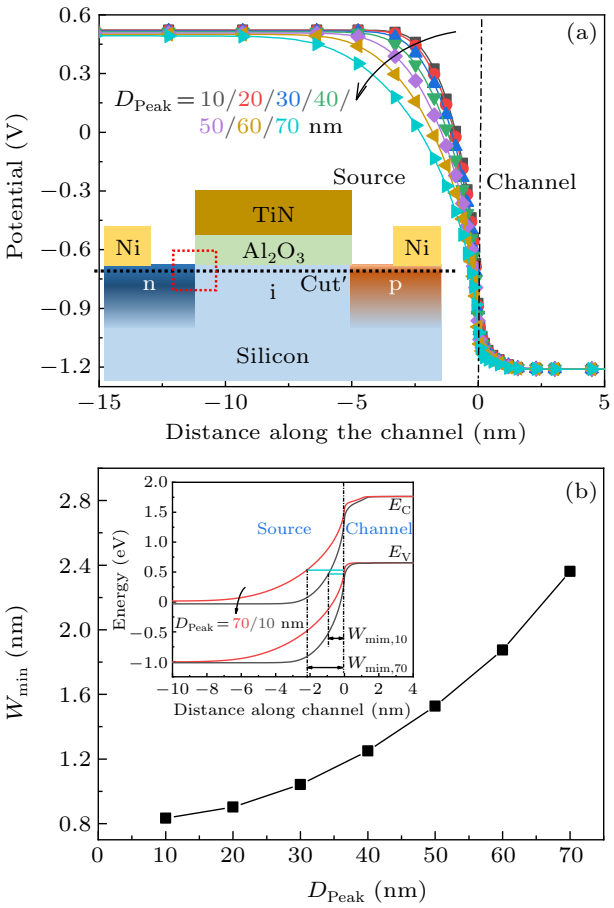


Fig. 1. (a) Potential distribution near the surface of the semiconductor when the tunnel junction is turned on at different peak positions. (b) The minimum tunneling barrier width when the TFET device is turned on at different peak positions; W_{min} is the minimum barrier width.

3. Design and characterization of a modulated doping ion implantation process

From the results discussed in the previous section, it is clear that reducing D_{peak} can effectively enhance the electric field strength at the tunneling junction on the device surface as well as reduce the width of the tunneling barrier and increase the tunneling probability, which could enhance the on-state current of the TFET device. There are two main methods for modulating D_{peak} in the current process: changing the ion injection energy or adding a barrier layer.[18] The impurity distribution in planar TFET devices is generally a shallow junction, and ion implantation is generally used for low-energy ion implantation, for which the range of energy options is small. In this work, the ion implantation D_{peak} is mainly regulated by adjusting the thickness of the ion implantation barrier layer.

The longitudinal distribution of ion implantation impurities is simulated by SRIM, and the distribution function is brought into TCAD software for device characterization to simulate D_{peak} and the minimum tunneling barrier width for different ion implantation barrier layers. As the thickness of the barrier layer increases in a certain range, D_{peak} gradually

decreases and W_{min} in the on-state of the device also decreases. When the barrier layer is thicker than 70 nm, W_{min} tends to rise. When the implantation barrier layer is thicker than 80 nm, the peak position of ion injection is already at the semiconductor surface. As the thickness of the barrier layer increases, more than half of the impurities remain in the barrier layer, resulting in a decrease in the impurity concentration at the surface and an increase in the tunneling barrier width, which reduces tunneling probability. Therefore, when the implantation energy is 60 keV, the thickness of the barrier layer should be ensured to be around 60 nm–70 nm. D_{peak} under this condition can make the tunneling barrier width near the surface smaller and the tunneling probability higher.

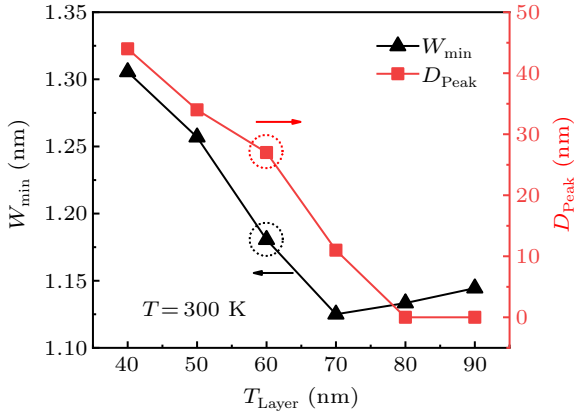


Fig. 2. The influence of different ion implantation barrier layer thicknesses (T_{layer}) on the minimum barrier width (W_{min}) of the TFET and the ion implantation peak position (D_{peak}).

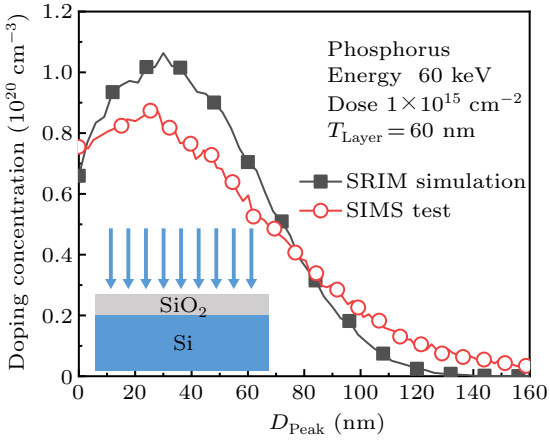


Fig. 3. Comparison of impurity distribution by SRIM simulation results and secondary ion mass spectrometry (SIMS).

According to the simulation results, the thickness of the ion implantation barrier layer (T_{layer}) in this work is set to 60 nm. In the experiment, the SiO_2 is grown by plasma enhanced chemical vapor deposition (PECVD) as the barrier layer. The actual thickness is about 61.30 nm when measured using a film thickness meter, and this thickness meets the experimental requirements. After the experimental samples were annealed by impurity activation and metallization, the impurity distribution was tested by secondary ion mass spectrometry and the test results were compared with the simulation results, as shown in Fig. 3. Because the actual barrier material grown is not completely consistent with the ideal material there are differences in the effect of impurity blocking. The annealing process also leads to the secondary diffusion of impurities, which results in a lower test result for the impurity concentration distribution peak compared with the simulation. This result does not affect device fabrication.

4. TFET device experiment and analysis

4.1. Device preparation process

The experiments in this work focus on source region ion implantation, and the process flow is shown in Fig. 4(a). According to the TCAD simulation results and the experimental test results, it is necessary to grow 60 nm SiO_2 as a barrier layer before ion implantation, and then form the source (P, 60 keV, 1×10^{15} cm^{-2}) and drain (B, 40 keV, 1×10^{15} cm^{-2}) regions by ion implantation. After removing the SiO_2, the doped impurity ions were activated by rapid thermal annealing (RTA) at 1050 °C. The high-k gate oxide layer Al_2O_3 is grown by atomic layer deposition, TiN is grown by magnetron sputtering and the gate electrode is formed by dry etching. The passivation layer is grown by PECVD and the contact hole is formed by reactive ion etching. The source and drain electrodes are formed by Ni/Au, and finally the metallization is completed by RTA. The morphology of the fabricated device is shown in Fig. 4(b).

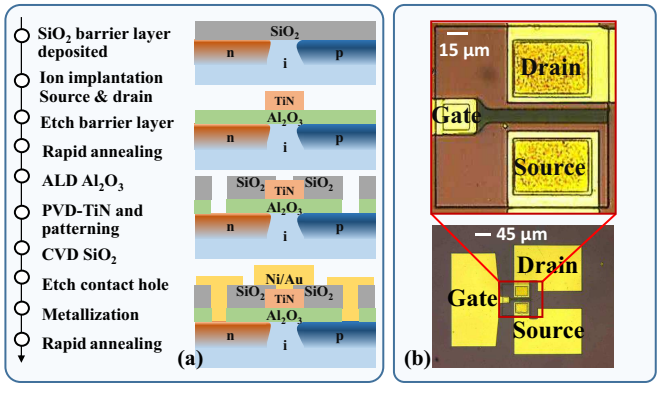


Fig. 4. (a) Key process flow chart of device preparation. (b) Device morphology.

4.2. Results and discussion

The test results for the p-TFET device fabricated in this work are shown in Fig. 5. The on-state current of the device is about 1.8×10^{-7} A·μm^{-1} when the drain bias voltage is −1 V. The current density is improved by about two orders of magnitude when compared with the test results for devices with the same structure reported in the literature.[20] It can be seen that

by adjusting the peak ion injection position, the chance of tunneling is effectively enhanced and the on-state current density of the device is significantly increased.

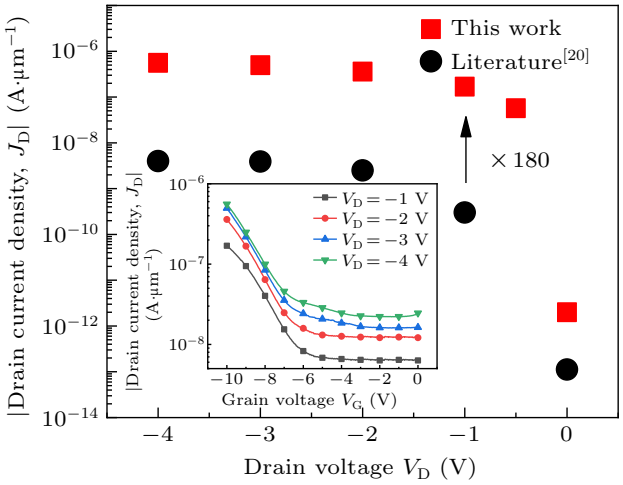


Fig. 5. The on-state current test results of the device under different drain voltage biases are compared with those in the literature.[20] The inset shows the test result of the transfer characteristic curve of the device.

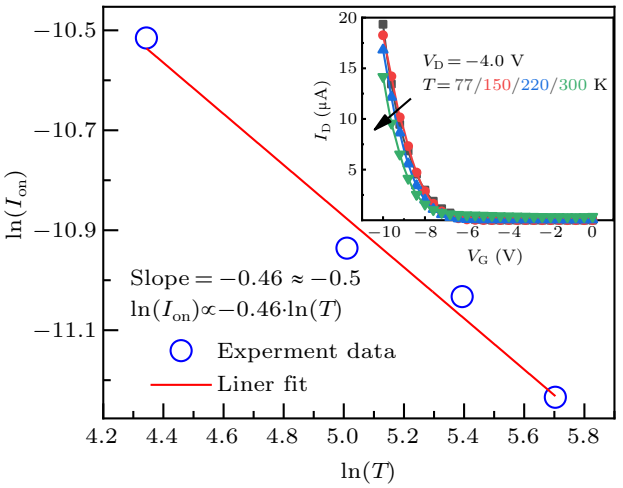


Fig. 6. Relationship between on-state current and temperature of the p-TFET device.

The transfer characteristic curves of the device were tested at 77 K, 150 K, 220 K and 300 K, as shown in the inset to Fig. 6. The current at a drain bias voltage of −1 V and a gate bias voltage of −10 V was extracted as the on-state current of the device for comparison. According to the analysis, the on-state current of the device is inversely correlated with the temperature, and the current increases as the temperature decreases. In Ref. [17], the tunneling current is independent of temperature. However, the carriers can only reach the channel region from the source region through the tunneling effect, and movement from the channel region to the drain region is by diffusion. The on-state current of the device should be the tunneling current limited by the diffusion mechanism. The diffusion current can be expressed as $J_{dif} = (kT/q) \cdot \mu_s \cdot (dn/dx)$, where T is the temperature, μ_s is the electron mobility in the channel with a T dependence of $T^{-1.5}$ due to phonon scattering and dn/dx is the carrier concentration gradient in the channel, which is independent of temperature because the carriers in the channel region are tunneled from the source region, and its concentration gradient is independent of temperature. The relationship between diffusion current and temperature is $J_{dif} \propto (kT/q) \cdot \mu_s \propto T^{-0.5}$. It can be expressed on a logarithmic scale as $\ln J_{dif} \propto -0.5 \ln T$, which is a straight line with a slope of −0.5. The slope of the curve fitted in Fig. 6 is −0.46, which is extremely close to the slope of the theoretical value of −0.5, and the turn-on current can be considered as the tunneling current limited by diffusion.[21]

5. Conclusion

In this paper, the mechanism of regulating the tunneling current of TFET devices is illustrated by studying the influence of the ion injection peak position on the potential and tunneling barrier width at the surface of p-TFET devices. A planar p-TFET device with a high on-state current is fabricated and the test results show that the device has a current that is increased by about two orders of magnitude compared with reported devices having the same structure. This method provides a new idea for increasing the current of p-TFET devices, and the method is theoretically applicable for n-TFETs as well. The method helps to optimize the matching design of TFETs in realizing the basic unit of the circuit, and promotes the development of TFETs device in integrated circuit applications.

Acknowledgments

Project supported by the Key Research and Development Program of Shaanxi (Grant No. 2021GY-010) and the National Defense Science and Technology Foundation Strengthening Program of China (Grant No. 2019-XXXX-XX-236-00).

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