Low switching loss and increased short-circuit capability split-gate SiC trench MOSFET with p-type pillar

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A split-gate SiC trench gate MOSFET with stepped thick oxide, source-connected split-gate (SG), and p-type pillar (p-pillar) surrounded thick oxide shielding region (GSDP-TMOS) is investigated by Silvaco TCAD simulations. The source-connected SG region and p-pillar shielding region are introduced to form an effective two-level shielding, which reduces the specific gate–drain charge ($Q_{gd,sp}$) and the saturation current, thus reducing the switching loss and increasing the short-circuit capability. The thick oxide that surrounds a p-pillar shielding region efficiently protects gate oxide from being damaged by peaked electric field, thereby increasing the breakdown voltage (BV). Additionally, because of the high concentration in the n-type drift region, the electrons diffuse rapidly and the specific on-resistance ($R_{on,sp}$) becomes smaller. In the end, comparing with the bottom p^+ shielded trench MOSFET (GP-TMOS), the Baliga figure of merit (BFOM, $BV^2/R_{on,sp}$) is increased by 169.6%, and the high-frequency figure of merit (HF-FOM, $R_{on,sp} \times Q_{gd,sp}$) is improved by 310%, respectively.

Keywords: SiC gate trench MOSFET, gate oxide reliability, switching loss, gate–drain charge ($Q_{gd,sp}$), short circuit

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1. Introduction

Silicon carbide (SiC) power MOSFET is regarded as one of the most promising power device candidates, and it can be widely used in solar power inverters, electric cars, rail transportation, spacecraft, and other high temperature, high pressure, and high power fields.[1–6] These applications require SiC power MOSFETs to possess both low switching loss and high reliability, such as gate oxide reliability and short-circuit capability.

Compared with SiC planar gate MOSFET, SiC trench gate MOSFET (UMOSFET) can accommodate many channels and completely eliminate the JFET effect, resulting in a significant reduction in specific on-resistance ($R_{on,sp}$).[7,8] However, the conventional SiC UMOSFET possesses the peak gate oxide electric field (E_{ox}) and large transfer capacitance (C_{rss}). These problems will affect its wide applications. To relieve the peak E_{ox} around the gate trench, some novel device structures to solve this problem have been reported in recent years.[9–19] A gate bottom p^+ shielded trench MOSFET (PS-TMOS) has been reported.[9–13] However, the $R_{on,sp}$ of the device will be significantly increased. A high performance SiC trench MOSFET with double-trench was proposed by Rohm Inc. to reduce the high E_{ox} around the bottom of the gate trench.[14] Song *et al.*[15] studied a new SiC UMOSFET by using an L-shaped shielding region to reduce E_{ox}. The CoolSiC™ MOSFET with an asymmetric cell was proposed by Infineon Inc.[16] Yang *et al.*[17] reported a 1200-V SiC trench MOSFET with an enhanced vertical reduced surface field. Wei *et al.*[18] proposed a superior SiC UMOSFET structure by using a floating p-shield region to effectively reduce E_{ox}. Yang *et al.*[19] investigated a novel SiC UMOSFET by using a deep p^+ shielded region and current spreading layer. Besides, the stepped oxide,[20–22] split-gate (SG),[23–25] and thick bottom-oxide structure[26–28] have been proposed to further improve the compromise relationship between E_{ox} and $R_{on,sp}$.

Additionally, in high-frequency applications, the high gate–drain capacitance ($C_{gd} = C_{rss}$) of the SiC trench gate MOSFET results in a large switching loss.[29] It is an effective method to increase the thickness or change the shape of the gate oxide at the bottom of the SiC UMOSFET structure.[30,31] Then, the concept of source-connected SG is introduced into the SiC trench gate MOSFET. It effectively reduces contact between gate and drain, thus achieving the goal of reducing C_{gd}. However, the source-connected SG increases the $R_{on,sp}$ of the structure. In Ref. [32], it was reported that a super-junction (SJ) structure is a novel structure that further reduces the $R_{on,sp}$ without increasing E_{ox}. In Ref. [33], proposed was an SiC trench gate MOSFET with deep p-pillar embedded in the n-type drift layer, which enables the modified structure to effectively reduce C_{gd} and switching loss.

In this paper, a split-gate SiC UMOSFET structure with a source-connected SG and p-pillar surrounding a thick-oxide

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shielded region is studied by utilizing TCAD simulation. In on-state mode, the n-type drift layer of the GSDP-TMOS structure has a higher doping concentration, which exceeds the JFET effect itself brought, thus reducing $R_{on,sp}$ of the device. In off-state mode, the peak E_{ox} around the bottom of the trench gate can alleviate due to the p-pillar shielded region. Thus, the reliability of gate oxide of GSDP-TMOS structure is effectively improved, and the *BV* of the device is increased. Meanwhile, the GSDP-TMOS structure exhibits a lower specific gate–drain charge ($Q_{gd,sp}$) and the saturation current, which can reduce the high-frequency switching loss and increase the short-circuit capability.

2. Device structure and fabrication procedure

Figure 1 shows the cross-section of the PS-TMOS structure[19] and the GSDP-TMOS structure. The gate trench structure of the GSDP-TMOS is composed of a stepped trench including shallow trench and deep trench. Moreover, the gate structure of the GSDP-TMOS has a p-type pillar surrounding the deep trench and a split gate connected to the source. The shallow trench is wider than deep trench and is mainly composed of gate poly-silicon and SG poly-silicon. The thickness of gate oxide layer and SG oxide layer are 0.05 μm and 0.5 μm, respectively.

The deep trench is filled with thick oxide. A split-gate connected to the source in the gate trench decouples the drain-gate interaction. Therefore, the C_{gd} charge and gate–drain charge (Q_{gd}) are significantly reduced, resulting in higher switching speed loss and lower switching loss. The super-junction shield region composed of p-pillar drift region and n-type drift region) surrounds the deep trench to ensure that the whole drift region is fully depleted and breakdown point appears in the middle of the adjacent gate trench. At the same time, the n-type drift region has a higher doping concentration due to the p-pillar embedded in the new structure. The n-type drift region doping concentration (N_d) was set to 3×10^{16} cm^{-3}. The length of the p-pillar ($L_{p\text{-pillar}}$) was 7.0 μm. The main device parameters of the GSDP-TMOS and PS-TMOS were listed in Table 1.

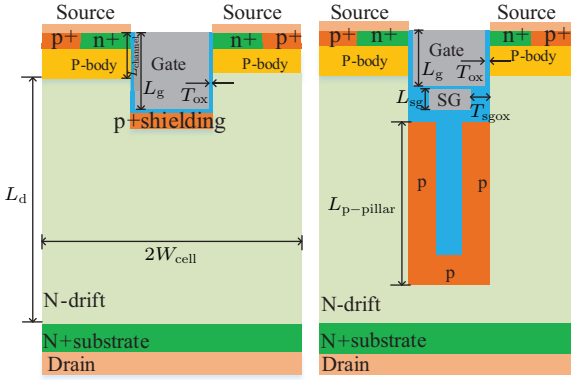


Fig. 1. Cross-sectional views of (a) the PS-TMOS structure and (b) the proposed GSDP-TMOS structure.

Table 1. Device parameters in simulations.

Main parameters	PS-TMOS	GSDP-TMOS
Gate trench depth L_g (μm)	1.55	0.60
N-drift layer thickness L_d (μm)	10.0	10.0
Gate oxide thickness T_{ox} (μm)	0.05	0.05
Split gate oxide thickness T_{sgox} (μm)	–	0.5
Split gate thickness L_{sg} (μm)	–	0.75
The p-pillar shielded region length under trench $L_{p\text{-pillar}}$ (μm)	–	7.0
Channel length $L_{channel}$ (μm)	0.5	0.5
Width of half cell pitch W_{cell} (μm)	2.10	2.10
Trench depth (μm)	1.6	1.6
P-body region concentration (cm^{-3})	2×10^{17}	2×10^{17}
N-type drift layer concentration N_d (cm^{-3})	8×10^{15}	3×10^{16}

Figure 2 shows a possible fabrication process flows for the GSDP-TMOS structure. An n-type layer was epitaxially grown on the SiC n$^+$ substrate and the trench was etched by using inductively coupled plasma (ICP) etching as shown in Fig. 2(a). The p-type trench-filling epitaxial growth was performed by using a hot-wall chemical vapor deposition system as shown in Fig. 2(b). The chemical mechanical polishing was performed to remove the excess p-type epitaxial layer from the trench and to adjust the p-pillar depth to 7.0 μm as indicated in Fig. 2(c). Then, the p-body and p$^+$ and n$^+$ sources were epitaxially grown on the n-type drift layer, and the process is similar to the conventional PS-TMOS manufacturing process as shown in Fig. 2(d). The first gate trench was formed by ICP etching and vertical injection formed a p-type region at the bottom of the trench as displayed in Fig. 2(e). The deep trench was filled with SiO_2, and n-type poly-silicon was deposited and etched on the back as shown in Fig. 2(f). The trench was filled with oxide and etched on the back as shown in Fig. 2(g). Thick oxide and n-type poly-silicon were deposited, then the n-type poly-silicon was etched as shown in Fig. 2(h). Gate oxide is grown and gate poly-silicon filled the trench and etch back, as shown in Fig. 2(i), forming the ohmic metal layer on the front and back sides. Then, the top metal layer is formed as shown in Fig. 2(j).

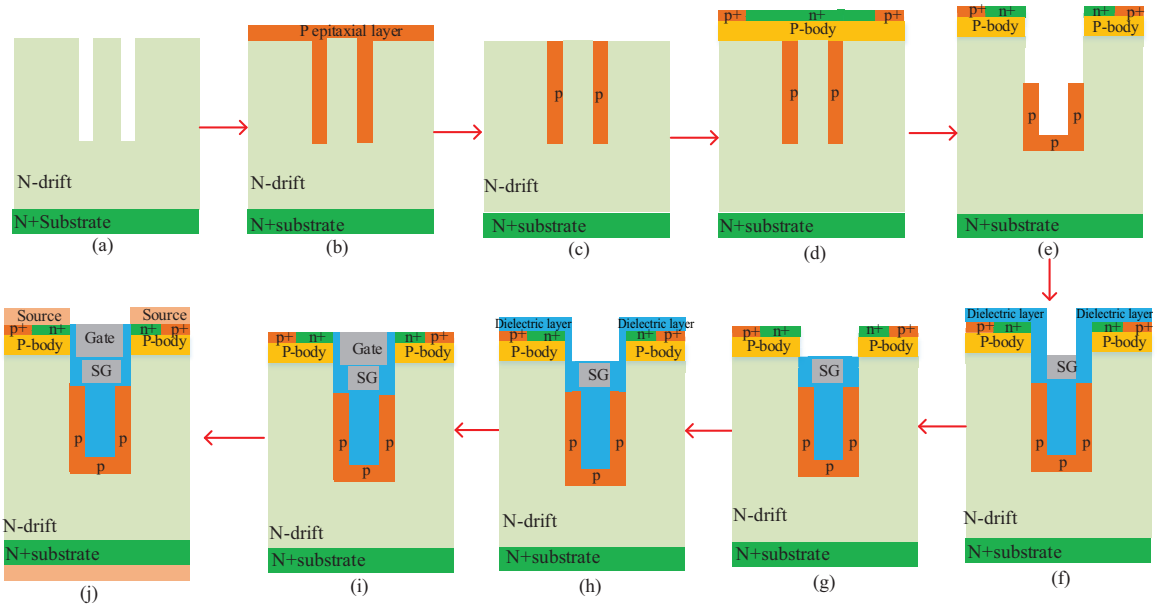


Fig. 2. Possible fabrication process flowchart for GSDP-TMOS.

3. Simulation result and discussion

The electrical performance of the PS-TMOS and GSDP-TMOS were verified by using Silvaco TCAD simulations.[34] The TCAD simulation results of the two structures largely depend on the physical model selection of the device.[35,36] Several models were used in this work, including the Shockley–Read–Hall (SRH) model and auger (AUGER) model. Owing to the presence of high concentration doping region, the band-gap narrowing (BGN) model was considered. In the mobility model (ANALYTIC) the effects of carrier concentration and electric field were taken into account. Besides, incomplete ionization and the Selberherr impact ionization model used to calculate ionization rates were considered. The parameters related to the physical model mentioned may refer to Refs. [34,37]. Prior to the discussion and analysis, the GSDP-TMOS structure must be optimized. For the GSDP-TMOS structure, the different $L_{\text{p-pillar}}$ of the p-pillar shielded region has a different significant effect on breakdown voltage (BV) and $R_{\text{on,sp}}$. And then, the different $L_{\text{p-pillar}}$ values of the p-pillar shielded region were simulated as shown in the following Fig. 3.

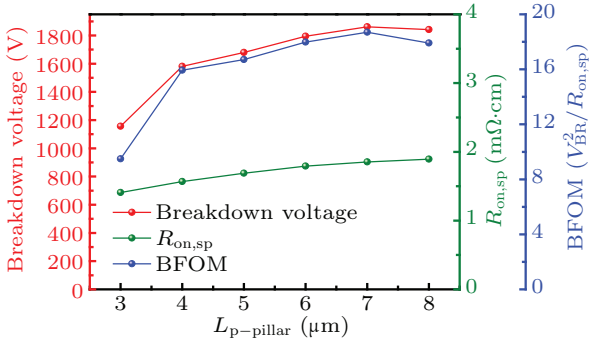


Fig. 3. Curve of BV, $R_{\text{on,sp}}$, and BFOM ($BV^2/R_{\text{on,sp}}$) versus $L_{\text{p-pillar}}$ of the GSDP-TMOS structure.

It can be seen that the highest BV about 1860 V appears at $L_{\text{p-pillar}} = 7.0$ μm corresponding to $R_{\text{on,sp}}$ of 1.87 mΩ·cm^2. Besides, with $L_{\text{p-pillar}}$ increasing from 7.0 μm to 8.0 μm, the $R_{\text{on,sp}}$ almost keeps rising, while the BV decreases. The Baliga figure of merit (BFOM, $BV^2/R_{\text{on,sp}}$) values under different $L_{\text{p-pillar}}$ values are shown in Fig. 3, indicating that the optimal $L_{\text{p-pillar}}$ is 7.0 μm.

In on-state, the I–V characteristic curves of the PS-TMOS and GSDP-TMOS at the gate-source voltage (V_{gs}) of 8 V, 12 V, 16 V, and 20 V, respectively, as shown in Fig. 4. It can be seen from Fig. 4 that the drain current of the PS-TMOS is lower than that of the GSDP-TMOS, which is due to the higher doping concentration in the n-type drift region of the optimized structure and the decrease of $R_{\text{on,sp}}$. Thus, $R_{\text{on,sp}}$ values of the two structures at $V_{\text{gs}} = 20$ V and drain–source voltage (V_{ds}) of 1 V are extracted. The $R_{\text{on,sp}}$ value of the PS-TMOS and GSDP-TMOS are 3.62 mΩ·cm^2 and 1.87 mΩ·cm^2, respectively.

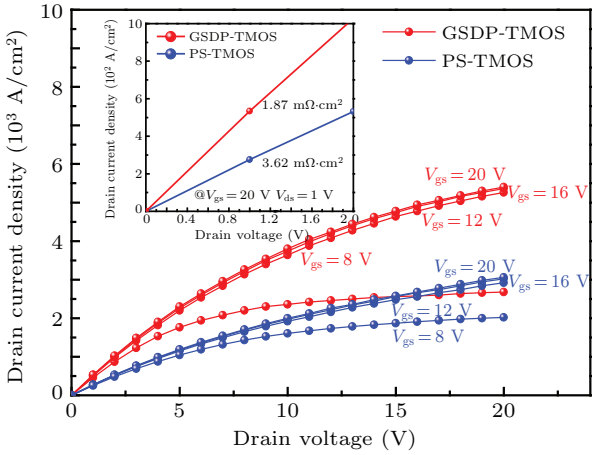


Fig. 4. The I–V characteristic curves of the PS-TMOS and GSDP-TMOS at $V_{\text{gs}} = 8$ V, 12 V, 16 V, and 20 V, respectively.

And then, comparing with the PS-TMOS, the $R_{on,sp}$ of the GSDP-TMOS decreases by 93.5%. To fully verify the above results, the distribution of the electron concentration for PS-TMOS and GSDP-TMOS are shown in Fig. 5. As can be seen from Fig. 5, the electron concentration in the n-type drift region of the GSDP-TMOS is higher than that of the PS-TMOS due to n-type drift region of the optimized structure with higher doping concentration. Specifically, the higher the electron concentration in the channel region, the lower the electron concentration in the depletion region is, which makes the current path of the GSDP-TMOS structure larger, thus reducing the $R_{on,sp}$. And the calculation result can be expressed as follows:

$$R_{on,sp} = \left(\frac{W_d}{q\mu_n N_d}\right), \tag{1}$$

where μ_n represents the mobility of the electron and W_d denotes the maximum depletion width.

The forward blocking I–V characteristic curve of the PS-TMOS and GSDP-TMOS are shown in Fig. 6(a). It can be seen that the BV of the GSDP-TMOS and PS-TMOS were 1860 V and 1576 V, respectively. Comparing with the PS-TMOS, the BV of the GSDP-TMOS increases by 18%. The increase of doping concentration in n-type drift region does not lead to the decrease of BV. It is mainly due to the fact that the thick oxide that surrounds a p-pillar shielded region efficiently protects the gate oxide from damaging by high electric field. Specifically, as the p-pillar drift region and n-type drift region in the GSDP-TMOS form a similar super-junction structure, the mutual depletion between the p-pillar layer and n-drift layer makes the electric field distribution in the n-drift layer more uniform, thereby alleviating the peak E_{ox} around the bottom of the trench gate. Therefore, BV of the GSDP-TMOS is higher than that of the PS-TMOS.

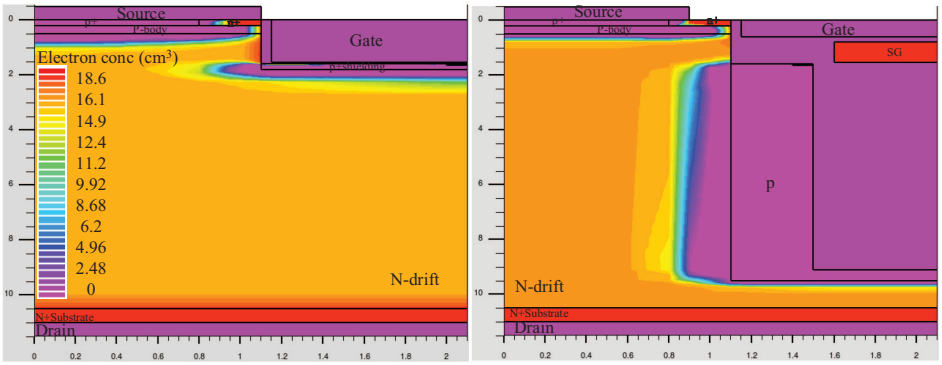


Fig. 5. Distribution of the electron concentrations for (a) PS-TMOS, (b) GSDP-TMOS.

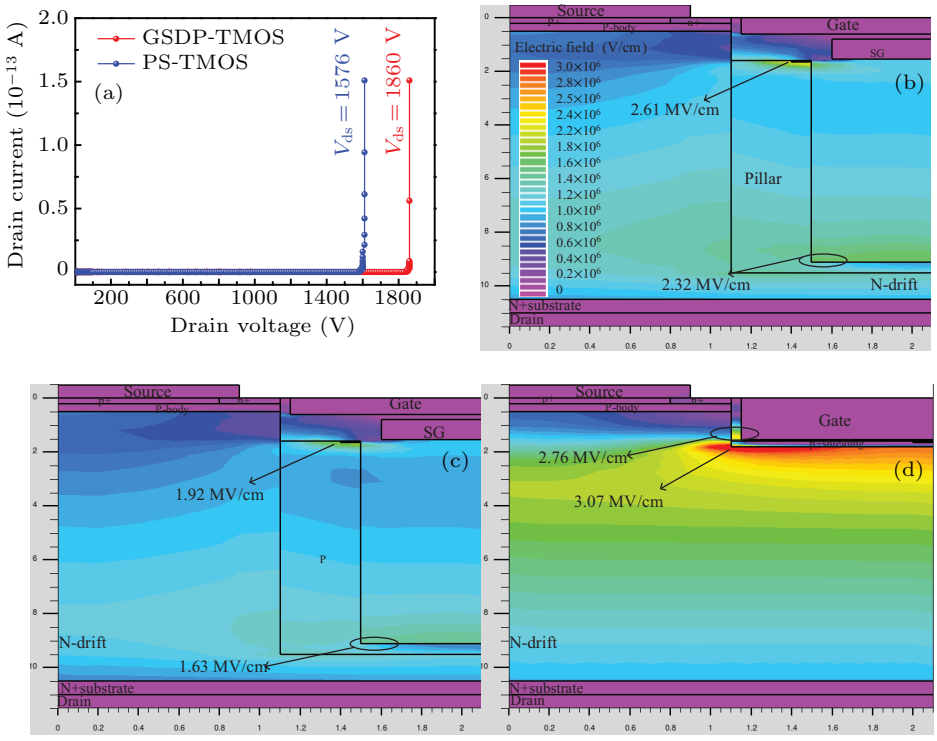


Fig. 6. (a) Forward blocking I–V characteristic curves of the two structures, the electric field distribution for (b) GSDP-TMOS at V_{ds} = 1860 V, (c) GSDP-TMOS at V_{ds} = 1200 V, and (d) PS-TMOS at V_{ds} = 1200 V.

The electric field distribution of the GSDP-TMOS at V_{ds} = 1860 V is shown in Fig. 6(b). It can be seen that the peak electric field in gate oxide ($E_{peak-ox}$) is 2.32 MV/cm for the GSDP-TMOS. Meanwhile, figures 6(c) and 6(d) show the electric field contours of the PS-TMOS and GSDP-TMOS under V_{ds} = 1200 V condition, respectively. As can be seen from Figs. 6(c) and 6(d), the $E_{peak-ox}$ of the PS-TMOS is 2.76 MV/cm. However, $E_{peak-ox}$ of the GSDP-TMOS is only 1.63 MV/cm. The $E_{peak-ox}$ is far below the PS-TMOS. Considering good long-time reliability, the higher electric field at *BV* for the PS-TMOS will induce gate oxide to break down or degrade. It can be concluded that since the p-pillar shielded region for the GSDP-TMOS relieves the $E_{peak-ox}$ around the bottom of the trench gate, the breakdown point is transferred to the PN junction between the p-pillar region and the n-drift region, which increases the breakdown voltage of the GSDP-TMOS structure to 1860 V. The $E_{peak-ox}$ of 2.32 MV/cm occurring at 1860 V is now below 3.0 MV/cm, for the GSDP-TMOS is in the safe area. As a result, an excellent BFOM ($BV^2/R_{on,sp}$) of 1850 MW/cm^2 is obtained, which is improved by 169.6% in comparison with PS-TMOS (686.1 MW/cm^2).

Figure 7 shows the curves of the typical C_{gd}, gate–source capacitance (C_{gs}), and drain–source capacitance (C_{ds}) of the GSDP-TMOS and PS-TMOS at f = 1 MHz and V_{ds} from 0 V to 1000 V. It can be seen that the C_{gd}, C_{gs}, and C_{ds} of the GSDP-TMOS are smaller than those of the PS-TMOS. The decrease of gate depth and the decoupling of the gate and drain interaction result in a significant decrease in C_{gd} and C_{gs}. A smaller C_{rss} is the main reason for the reduction in Miller's platform time, resulting in lower switching losses. As can be seen from Fig. 7, when the value of the V_{ds} is less than 45 V, the C_{rss} is small due to p-pillar shield region, which shields C_{gd}. Therefore, the capacitance at this time is mainly contributed by C_{gs}. When the V_{ds} is greater than 45 V, the shielding region of the p-pillar will be slowly depleted, and the shielding effect it can play will gradually decrease, resulting in the increase of the value of C_{rss}.

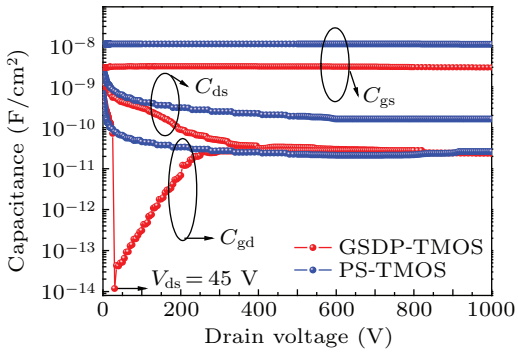


Fig. 7. Curves of capacitance C_{gd}, C_{gs}, and C_{ds} *versus* drain voltage of PS-TMOS and GSDP-TMOS.

The gate charge characteristic curves of the PS-TMOS and GSDP-TMOS are shown in Fig. 8, with inset indicating the gate charge test circuit. It can be seen that the GSDP-TMOS structure exhibits a smaller gate–drain charge (Q_{gd}). Compared with 74.9 nC/cm^2 for the PS-TMOS, the Q_{gd} for the GSDP-TMOS is only 28.3 nC/cm^2. The Q_{gd} is smaller than 164.6% of the PS-TMOS due to the source-connected SG and p-pillar shield region working together to reduce the overlap area between gate and drain of the GSDP-TMOS structure.

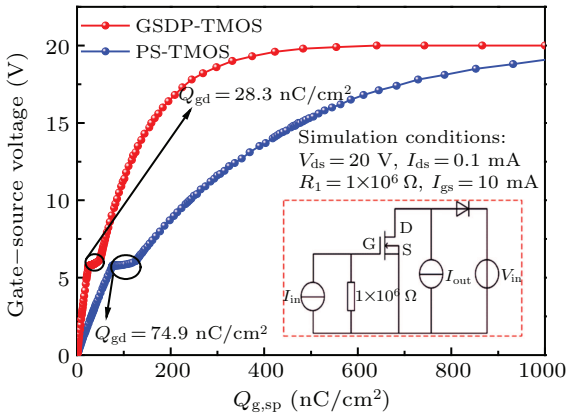


Fig. 8. Characteristic curves of gate–source voltage *versus* gate charge of PS-TMOS and GSDP-TMOS, with inset indicating the test circuit.

Moreover, the high-frequency figure of merit (HF-FOM, $R_{on,sp} \times Q_{gd,sp}$) is a very important parameter to comprehensively evaluate the electrical performances of SiC power devices,[38–40] and it can be obtained by calculating the $R_{on,sp}$ and $Q_{gd,sp}$ values of the above two structures. The HF-FOM ($R_{on,sp} \times Q_{gd,sp}$) of the PS-TMOS is 271.1 mΩ·nC. However, the GSDP-TMOS obtained superior HF-FOM ($R_{on,sp} \times Q_{gd,sp}$) is only a value of 52.9 mΩ·nC, which decreases by 310% compared with the counterpart of the PS-TMOS.

To verify the superior switching characteristics of GSDP-TMOS more effectively, the switching power loss of GSDP-TMOS is evaluated by a double-pulse test circuit and compared with that of PS-MOS as shown in Fig. 10(a). The double-pulse test circuit includes gate series resistor (R_g = 20 Ω), DC drain series voltage (V_{dd} = 600 V), and stray inductance (L_s = 10 nH). The gate series voltage pulse variation is used to simulate the real switch circuit situation of the device.

Figures 9(a) and 9(b) show the switching waveform of the PS-TMOS and GSDP-TMOS. As can be seen from Figs. 9(a) and 9(b), the GSDP-TMOS structure can achieve high V_{ds} and high I_{ds} in a shorter time than the PS-TMOS structure. Moreover, the turn-on and turn-off power loss of the two structures are shown in Figs. 9(c) and Fig. 9(d), respectively. It can be seen that the turn-on and turn-off power loss of the GSDP-TMOS significantly decrease due to the lower Q_{gd}. Meanwhile, the comparison of switching energy loss between the PS-TMOS and GSDP-TMOS is shown in Fig. 10(b). It can be seen that the turn-on energy loss (E_{on}) and turn-off energy loss (E_{off}) of GSDP-TMOS decrease. For the GSDP-TMOS, the calculated value of E_{on} and E_{off} are 31.3 mJ/cm^2

and 34.5 mJ/cm^2, respectively, which correspondingly reduces 15.6% and 26.6% of the counterparts for the PS-TMOS. The main electrical characteristic parameters of the GSDP-TMOS and PS-TMOS, including the $R_{on,sp}$, BV, BFOM ($BV^2/R_{on,sp}$), Q_{gd}, HF-FOM ($R_{on,sp} \times Q_{gd,sp}$), E_{on}, and E_{off} are listed in Table 2.

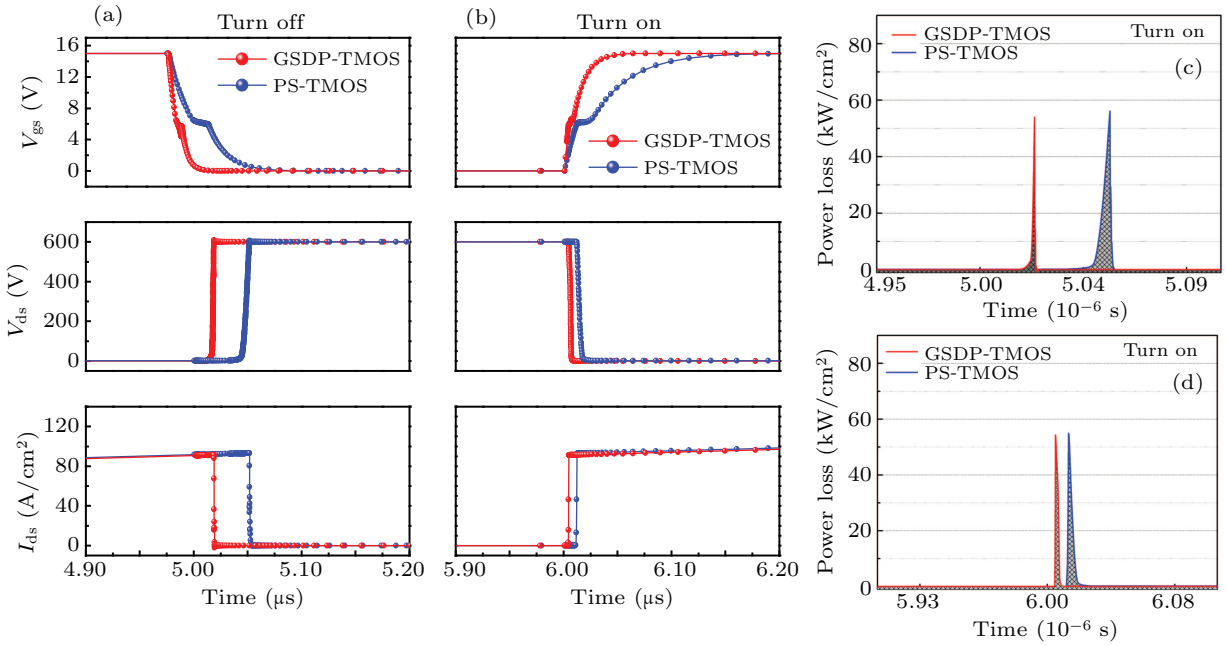


Fig. 9. (a) Turn-off switching waveform of PS-TMOS and GSDP-TMOS, (b) turn-on switching waveform of the PS-TMOS and GSDP-TMOS, (c) turn-off power loss between PS-TMOS and GSDP-TMOS, (d) turn-on power loss between PS-TMOS and GSDP-TMOS.

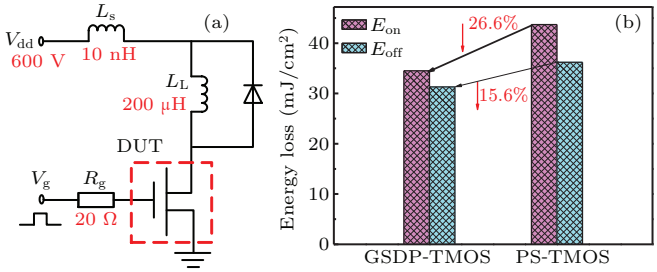


Fig. 10. (a) Test circuit, (b) comparison of power losse between the two structures.

Table 2. Comparison of performance between the PS-TMOS and GSDP-TMOS.

Parameters	PS-TMOS	GSDP-TMOS
[a]$R_{on,sp}$	1.87 mΩ·cm^2	3.62 mΩ·cm^2
BV	1576 V	1860 V
BFOM ($BV^2/R_{on,sp}$)	686.1 MW/cm^2	1850 MW/cm^2
Q_{gd}	74.9 nC/cm^2	28.3 nC/cm^2
HF-FOM ($R_{on,sp} \times Q_{gd,sp}$)	217.1 mΩ·nC	52.9 mΩ·nC
E_{on}	36.2 mJ/cm^2	31.3 mJ/cm^2
E_{off}	43.7 mJ/cm^2	34.5 mJ/cm^2

[a]$R_{on,sp}$ at $V_{gs} = 20$ V, $V_{ds} = 1.0$ V.

In addition, considering the application of the SiC power trench gate MOSFET in power electronic systems, the ability to safely turn off the power switch device in the event of short-circuit is essential. In general, the short-circuit capability of the SiC power MOSFET decreases with the value of $R_{on,sp}$ decreasing. When the SiC MOSFET works in the on-mode, due to the short circuit of the load, the high voltage source can be directly applied to the drain, which is called the short-circuit situation. High drain current and high drain voltage flow through the device, resulting in high power loss and increasing internal lattice temperature.

To verify the improvement of GSDP-TMOS short-circuit capability. The short-circuit simulations of mix-mode circuit is shown in Fig. 11(a). The short-circuit test circuit includes gate series resistor ($R_g = 10$ Ω), DC drain series voltage ($V_{dd} = 800$ V), and stray inductance ($L_s = 20$ nH). The gate series voltage pulse variation is used to simulate the real short circuit situation of the device. The short-circuit test simulations results of the GSDP-TMOS and PS-TMOS are shown in Fig. 11(b). It can be seen that the GSDP-TMOS has the low drain current density and minimum temperature compared with the PS-TMOS.

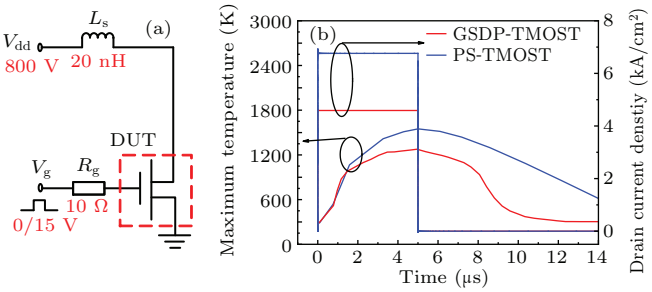


Fig. 11. (a) Circuit for short-circuit simulations, and (b) curve of maximum temperature and drain current density *versus* time of the GSDP-TMOS and PS-TMOS under short-circuit condition.

Figure 12 shows the lattice temperature distribution of the GSDP-TMOS and PS-TMOS during short-circuit for 5 μs. As can be seen from Fig. 12(b), the position of the maximum lat-

tice temperature of the GSDP-TMOS is further away from the surface, which can effectively avoid the phenomenon of metal Al melting due to the high temperature. Due to the difference in the electric field distribution in the vertical direction, the peak electric field of the PS-TMOS is located near the device surface, while the peak electric field of the GSDP-TMOS structure is located at the bottom, resulting in Joule heating in the deeper region of the GSDP-TMOS structure and the temperature of the device rising, thus forming a positive feedback of temperature, which will eventually lead the current to increase sharply and leakage current to generate. Usually, owing to metal Al melting or gate oxygen degrading, the near surface region of SiC MOSFET can not withstand the instantaneous high temperature above 1300 K–1500 K. When the temperature reaches about 1500 K, the SiC MOSFET device will fail to work.[41–43] As a result, the GSDP-TMOS structure has a higher robustness than the PS-TMOS against the short-circuit accident happening due to lower thermal stress in SiC/SiO_2 interface.

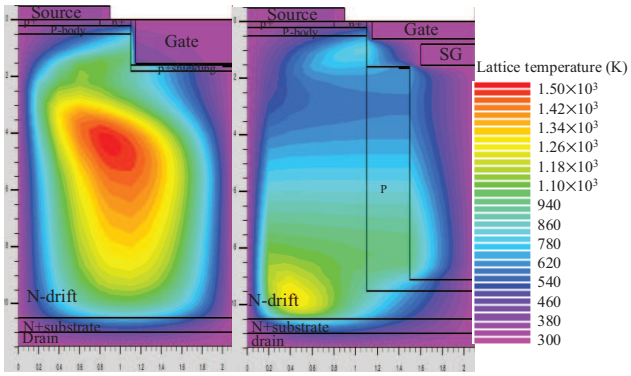


Fig. 12. Lattice temperature distribution of (a) PS-TMOS and (b) GSDP-TMOS during short-circuit for 5 μs.

4. Conclusions and perspectives

The 4H-SiC trench MOSFET with a source-connected SG and p-pillar shielded region is presented in this work. With p-pillar surround thick-oxide shielded region, the improved structure shows that it can effectively alleviate the peak electric field around gate oxide in off-state mode. Meanwhile, the n-type drift layer of the GSDP-TMOS structure has a higher doping concentration, thus reducing $R_{on,sp}$ of the device without sacrificing the BV. In addition, the GSDP-TMOS demonstrates superior switching characteristics, and thus reducing the switching loss and increasing the short-circuit capability due to a lower $Q_{gd,sp}$ and the saturation current. As a result, the enhanced performance enables the GSDP-TMOS structure to act as one of the favorable candidates for high power applications.

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