Degradation mechanisms for polycrystalline silicon thin-film transistors with a grain boundary in the channel under negative gate bias stress

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The negative gate bias stress (NBS) reliability of n-type polycrystalline silicon (poly-Si) thin-film transistors (TFTs) with a distinct defective grain boundary (GB) in the channel is investigated. Results show that conventional NBS degradation with negative shift of the transfer curves is absent. The on-state current is decreased, but the subthreshold characteristics are not affected. The gate bias dependence of the drain leakage current at V_{ds} of 5.0 V is suppressed, whereas the drain leakage current at V_{ds} of 0.1 V exhibits obvious gate bias dependence. As confirmed via TCAD simulation, the corresponding mechanisms are proposed to be trap state generation in the GB region, positive-charge local formation in the gate oxide near the source and drain, and trap state introduction in the gate oxide.

Keywords: negative bias stress, poly-Si, thin-film transistor, grain boundary

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1. Introduction

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) are widely used in pixel circuits and peripheral driver circuits of small-size and high-resolution active-matrix flat-panel displays. However, due to the polycrystalline nature and the existence of grain boundaries (GBs) in the poly-Si film, the electrical characteristics of poly-Si TFTs may be deteriorated depending on the location of the GBs.[1–3] On the contrary, the GB in scaled TFTs is reported to be able to improve the off-state current and the subthreshold swing of poly-Si TFTs.[4]

In addition to the electrical performance of the as-fabricated poly-Si TFTs, degradation behavior and the corresponding degradation mechanisms under various kinds of bias stress should be well understood before the optimal design of poly-Si TFTs and TFT-based circuits. Stress conditions, such as positive gate bias stress, negative gate bias stress (NBS), and hot-carrier (HC) effect, could all result into degradation in TFTs' electrical characteristics, but the typical degradation phenomena obviously differ, exhibiting positive[5] and negative shift of the transfer curves[6–8] and decreased on-state current (I_{on}) with unaffected subthreshold characteristics,[9] respectively.

GB-related HC degradation in poly-Si TFT has been reported,[10] whereas the effects of GB on other kinds of stress-induced degradation are not yet clarified. In the present paper, NBS degradation in poly-Si TFTs with a defective GB in the channel is investigated. Typical NBS degradation with negative shift of the transfer curves is found to be absent. Instead, reduced on-state current, unaffected subthreshold characteristics and suppressed gate-induced drain leakage (GIDL) current are observed. The corresponding mechanisms for the observed degradation phenomena are proposed in this paper.

2. Experiments

TFTs with a defective GB in the channel were fabricated on the basis of metal-induced lateral crystallization (MILC) technology.[11] A 100-nm-amorphous silicon was firstly deposited by the low-pressure chemical vapor deposition on silicon wafers covered with 500-nm thermal oxide. It was then patterned into the active islands before the deposition of 300-nm low-temperature oxide (LTO). After the definition of metal-introducing windows (MIWs) and the following deposition of 10-nm Ni by electron-beam evaporation, MILC heat-treatment was carried out in nitrogen atmosphere at 550 °C for 24 hrs. Further 24 hrs of post-annealing at 550 °C was performed to improve the quality of the poly-Si after removing the unreacted nickel.[12] The TFTs were fabricated on the bilaterally crystallized poly-Si regions, where MIWs were opened on the two ends of the active island and crystallization proceeded from the MIWs towards the center of the active island, as schematically shown in Fig. 1. The two MILC fronts met and formed the defective MILC/MILC GB in the channel region of the TFT, which was perpendicular to the direction of the current flow in the channel.

After the 300-nm covering LTO was removed, the 100-nm LTO was deposited as the gate dielectric and 300-nm poly-Si was deposited and patterned to form the gate, followed by self-aligned phosphorus implantation at a dosage of 4×10^{15} cm^{-2} and an implantation energy of 120 keV. Dopants were activated at 620 °C for 3 hrs. A 500-nm LTO was then

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deposited, through which contact holes were opened, followed by deposition and patterning of 500-nm Al–1%Si into electrode pads. Finally, forming-gas annealing was performed at 420 °C for 30 min.

During the application of NBS to the poly-Si TFTs at the room temperature, a constant negative gate bias of −35 V was applied to the gate electrode with the source and drain electrodes grounded. The TFTs' transfer curves before and after NBS were measured with the semiconductor parameter analyzer Agilent 4156C. The default channel width-to-length ratio of the poly-Si TFTs used in this paper is $W/L =$ 10 μm/30 μm.

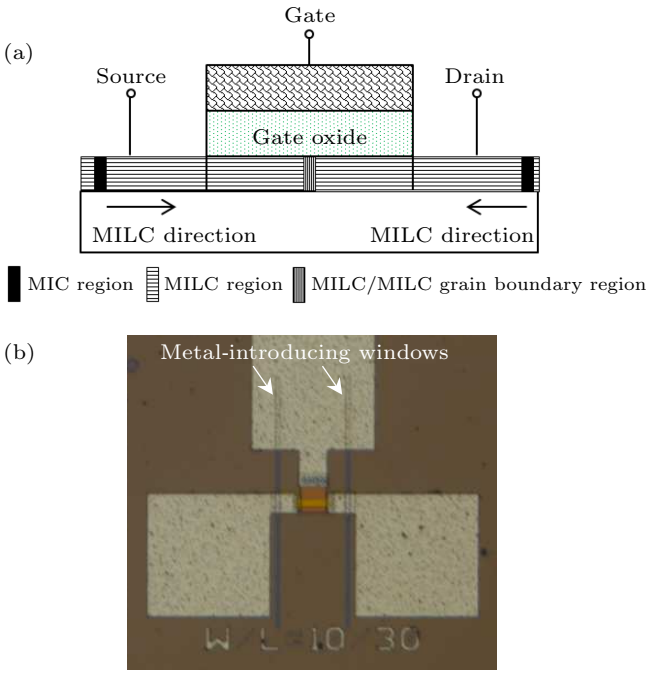


Fig. 1. (a) Cross-sectional diagram and (b) plane-view picture of the TFT with bilaterally crystallized poly-Si channel and one MILC/MILC grain boundary in the channel.

3. Results and discussion

The electrical performance of the fabricated poly-Si TFTs were firstly characterized. Figure 2 shows the representative transfer curves and output curves. From the transfer curve measured with V_{ds} of 0.1 V, the field-effect mobility (μ_{FE}), extracted from the maximum transconductance, and threshold voltage (V_{th}), extracted by the linear extrapolation method, were 85.1 cm^2/V·s and 6.5 V, respectively. With an off-sate leakage current (I_{off}) of 2.1×10^{-11} A defined as the minimum drain current at V_{ds} of 5.0 V, and on-state current (I_{on}) of 3.0×10^{-5} A defined as the drain current at V_{ds} of 5.0 V and V_{gs} of 15.0 V, I_{on}/I_{off} is estimated to be 1.43×10^6. The gate voltage difference characterizing the drain-induced barrier lowing effect (V_{DIBL}) for the same drain current of 1×10^{-9} A at V_{ds} of 0.1 V and 5.0 V is 1.6 V and the subthreshold swing (SS) is 1.45 V/decade. The output curves exhibit good linear dependence on drain bias at small drain bias voltages and good saturation phenomenon at high drain bias voltages.

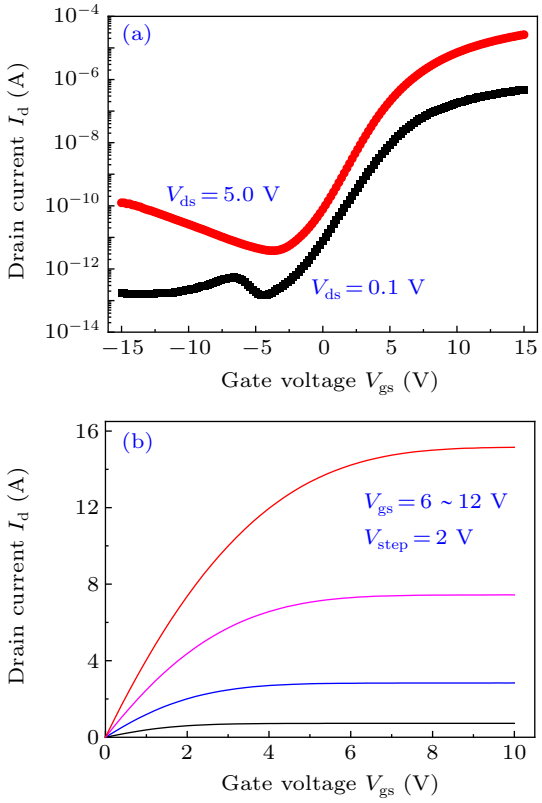


Fig. 2. (a) Transfer curves and (b) output curves of the fabricated poly-Si TFTs.

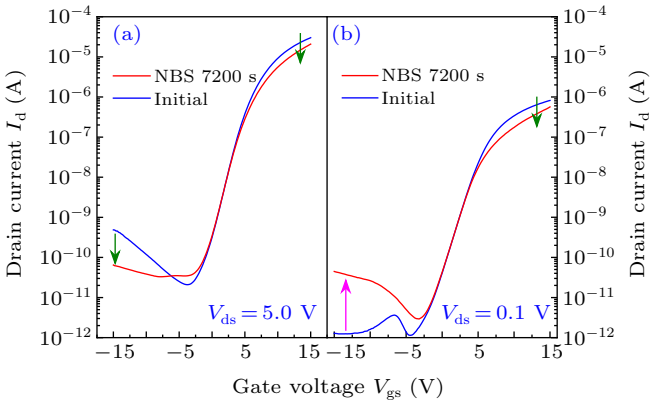


Fig. 3. Comparison of the transfer curves measured before and after NBS for 7200 s with (a) $V_{ds} = 5.0$ V and (b) $V_{ds} = 0.1$ V.

Figure 3 compares the transfer curves of one poly-Si TFT before and after NBS for 7200 s. The negative shift of the transfer curves frequently observed for poly-Si TFTs under NBS is absent. Instead, the TFT after NBS exhibits decreased I_{on}, unaffected subthreshold characteristics, and suppressed GIDL current at a V_{ds} of 5.0 V (Fig. 3(a)). These degradation phenomena are quite similar to the typical HC stress-induced degradation phenomena at the first sight. However, the reverse-mode characteristics of the TFT behave almost the same as the forward-mode characteristics (Fig. 4), where the reverse-mode characteristics are measured with the source

and drain exchanged from the configurations in forward-mode measurements. While the on-state current degrades more under reverse mode than under forward mode in HC-induced degradation.[13]

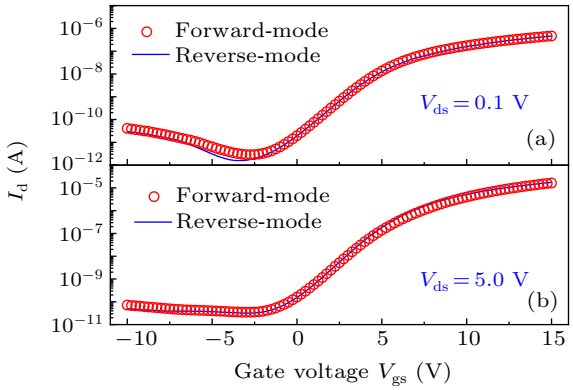


Fig. 4. Comparison of the transfer curves measured in forward mode and reverse mode for poly-Si TFT under NBS for 7200 s with (a) $V_{ds} = 0.1$ V and (b) $V_{ds} = 5.0$ V.

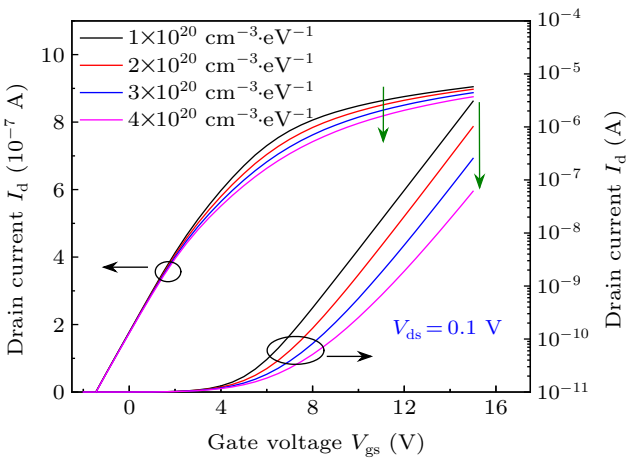


Fig. 5. Simulated transfer characteristic curves for poly-Si TFTs with different n_{TA} values in the grain boundary.

The decreased on-state current after NBS indicates the trap state generation and the unaffected subthreshold characteristics imply that the trap states are not produced uniformly in the channel region.[14,15] Further considering the existence of weak Si–Si bonds and Si–H bonds in the GB, the trap states are most probably locally generated in the MILC/MILC GB. The hypothesis that the locally increased trap states in the GB result into the decreased on-state current were verified by simulation with Silvaco Atlas,[16] where the GB region was set to be 1 μm wide and the concentration of the acceptor-like tail states (n_{TA}) was increased after fitting the initial transfer curves. The parameters, including the distribution of trap states in the poly-Si outside the GB and in the GB, are summarized in Tables 1 and 2, respectively.

As shown in Fig. 5, the on-state current dose decreases with the increase in n_{TA}. The energy barrier in the conduction band formed at the GB in the on-state with V_{gs} of 15 V increases with the increase in n_{TA} (Fig. 6) which could hinder the current flow and suppress the on-state current. Furthermore, when the n_{TA} in the GB region is increased to

Table 1. Parameters for the poly-Si outside the GB region.

Parameter	Value	Description
τ_n (s)	5×10^{-10}	lifetime of electrons outside the GB region
τ_p (s)	5×10^{-10}	lifetime of holes outside the GB region
Acceptor-like tail states	$g_{TA}(E) = N_{TA} \times \exp[(E - E_C)/W_{TA}]$	
N_{TA} (cm^{-3}·eV^{-1})	1.8×10^{19}	density of acceptor-like tail states at E=E_C
W_{TA} (eV)	0.055	characteristic decay energy for the acceptor-like tail states
Acceptor-like deep states	$g_{GA}(E) = N_{GA} \times \exp[-((E - E_{GA})/W_{GA})^2]$	
N_{GA} (cm^{-3}·eV^{-1})	0.6×10^{18}	peak value of acceptor-like deep states
E_{GA} (eV)	0.3	energy position of the peak value of acceptor-like deep states
W_{GA} (eV)	0.1	characteristic decay energy of the acceptor-like deep states
Donor-like tail states	$g_{TD}(E) = N_{TD} \times \exp[(E_V - E)/W_{TD}]$	
N_{TD} (cm^{-3}·eV^{-1})	2×10^{19}	density of donor-like tail states at E=E_V
W_{TD} (eV)	0.1	characteristic decay energy for the donor-like tail states
Donor-like deep states	$g_{GD}(E) = N_{GD} \times \exp[-((E - E_{GD})/W_{GD})^2]$	
N_{GD} (cm^{-3}·eV^{-1})	0.3×10^{18}	peak value of donor-like deep states
E_{GD} (eV)	0.4	energy position of the peak value of donor-like deep states
W_{GD} (eV)	0.1	characteristic decay energy of the donor-like deep states

Table 2. Parameters for the poly-Si in the GB region.

Parameter	Value	Description
τ_n (s)	5×10^{-11}	lifetime of electrons in the GB region
τ_p (s)	5×10^{-11}	lifetime of holes in the GB region
Acceptor-like tail states	$g_{TA}(E) = N_{TA} \times \exp[(E - E_C)/W_{TA}]$	
N_{TA} (cm^{-3}·eV^{-1})	1.0×10^{20}	density of acceptor-like tail states at E=E_C
W_{TA} (eV)	0.055	characteristic decay energy for the acceptor-like tail states
Acceptor-like deep states	$g_{GA}(E) = N_{GA} \times \exp[-((E - E_{GA})/W_{GA})^2]$	
N_{GA} (cm^{-3}·eV^{-1})	1.0×10^{18}	peak value of acceptor-like deep states
E_{GA} (eV)	0.3	energy position of the peak value of acceptor-like deep states
W_{GA} (eV)	0.1	characteristic decay energy of the acceptor-like deep states
Donor-like tail states	$g_{TD}(E) = N_{TD} \times \exp[(E_V - E)/W_{TD}]$	
N_{TD} (cm^{-3}·eV^{-1})	5.0×10^{19}	density of donor-like tail states at E=E_V
W_{TD} (eV)	0.1	characteristic decay energy for the donor-like tail states
Donor-like deep states	$g_{GD}(E) = N_{GD} \times \exp[-((E - E_{GD})/W_{GD})^2]$	
N_{GD} (cm^{-3}·eV^{-1})	1×10^{18}	peak value of donor-like deep states
E_{GD} (eV)	0.4	energy position of the peak value of donor-like deep states
W_{GD} (eV)	0.1	characteristic decay energy of the donor-like deep states

4.2×10^{20} cm^{-3}·eV^{-1} and the n_{GA}, the peak value of acceptor-like deep states, is increased to 1.2×10^{18} cm^{-3}·eV^{-1}, the measured subthreshold and on-sate characteristics after NBS for 7200 s could be well fitted by the simulated results (Fig. 7), thereby confirming the validity of the proposed mechanism.

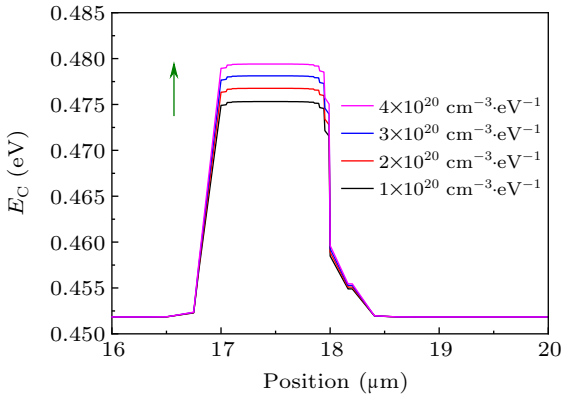


Fig. 6. Comparison of the energy barrier for electrons in the conduction band formed at the grain boundary with different n_{Ta}, where V_{gs} is 15 V and $V_{ds}=0$ V.

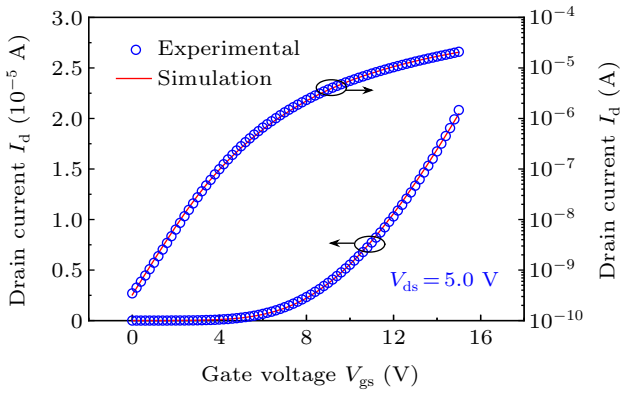


Fig. 7. Comparison of the transfer curve measured with $V_{ds}=5.0$ V after NBS for 7200 s and that simulated with $n_{TA}=4.2\times10^{20}$ cm^{-3}·eV^{-1} and $n_{GA}=1.2\times10^{18}$ cm^{-3}·eV^{-1} in the grain boundary.

In the NBS degradation mechanism, the holes available in the active layer are important factors to trigger the reactions in the NBS degradation and generation of positive charges in the gate oxide.[17–19] So, the 2D distribution contour of hole concentration in the active layer under the stress gate bias of −35 V was simulated. As shown in Fig. 8, high-concentration holes appear at the front surface in the GB and outside the GB regions.

Vertical distributions of the holes in the GB and those outside the GB were firstly extracted and compared (Fig. 9). At the top surface, the hole concentration is as high as 1.0×10^{19} cm^{-3} and 5.8×10^{18} cm^{-3} for the poly-Si outside the GB and in the GB regions, respectively. For a position far from the surface and at the same depth, the hole concentration in the GB is also much smaller than that outside the GB due to the higher trap state density in the GB. The lateral distribution of the holes in the channel at a depth of 80 nm from the top surface of the active island was also extracted, as shown in Fig. 10. The hole's concentration shows a peak value near the source/drain junctions and the peak concentration is surprisingly found to be more than two orders of magnitude higher than that in the active layer far from the source/drain junctions.

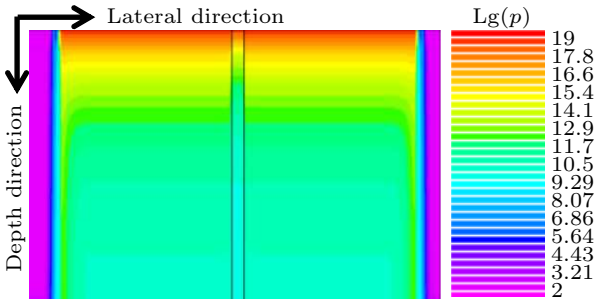


Fig. 8. Simulated 2D distribution contour of holes in cross-section of the active layer with a gate bias of −35 V.

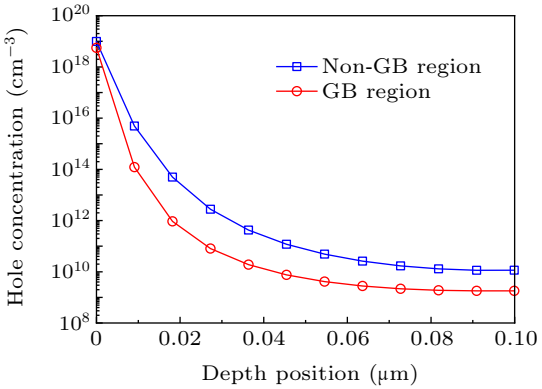


Fig. 9. Depth distribution of holes in the GB and outside the GB region with a gate bias of −35 V.

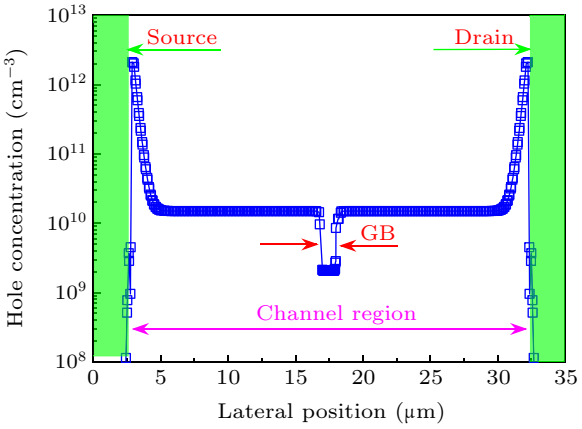


Fig. 10. Simulated lateral distribution of holes in the active island at a depth position of 80 nm with a gate bias of −35 V.

During NBS, the potential of the channel is coupled to be negative in respect to the grounded n^+ source and drain. Thus, reversely biased pn junctions are formed. The generated carriers in the depletion region of the source/drain pn junctions are separated by the electric field and holes drift into the channel of the TFT. In the neutral channel region, the holes diffuse towards the channel center from the source and drain sides, accompanied by recombination in the channel simultaneously.

Then, a non-uniform distribution of holes in the channel could be observed.[20]

The validity of the proposed explanation on the non-uniform distribution of holes in the active layer was further verified, where the lifetime of holes was varied. As shown in Figs. 11(b) and 11(c), the peak concentration and the distribution range of the peak for holes near the source/drain decrease as the lifetime of holes decreases. When the carrier generation in the source/drain depletion region through trap-assisted tunneling is further excluded, which is accounted for the fitting of the GIDL current during the simulation of initial transfer curves, the holes distribute uniformly in the channel and the concentration is as low as 1.5×10^{10} cm^{-3} [Fig. 11(d)], which is also reasonable as the thermal generation of holes in the active layer is uniform.

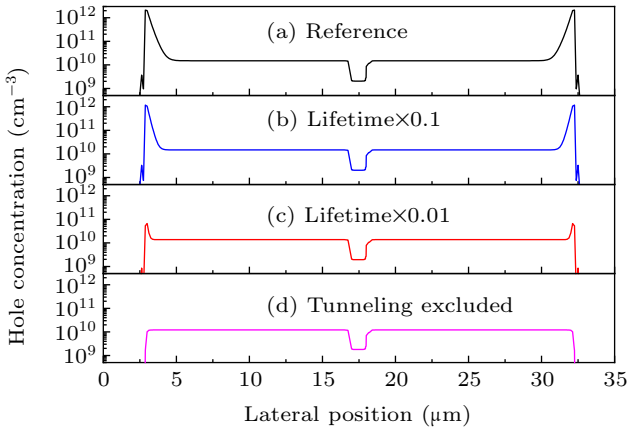


Fig. 11. Comparison of the simulated lateral distribution of the hole at a depth position of 80 nm in the active island with (a) default parameters, (b) lifetime reduced by one order of magnitude, (c) lifetime reduced by two orders of magnitude, and (d) carrier tunneling model excluded during simulation.

Considering the higher-concentration holes in the channel near the source and drain under NBS, typical NBS degradation still takes place with positive charges (Q_{ox}) formed locally in the gate oxide near the source and drain. The locally distributed positive changes screen the electric field from the gate in the off-state and reduce the GIDL current, such that the dependence of leakage current on gate bias at V_{ds} of 5.0 V is greatly reduced, as observed in Fig. 3(a).[21] As shown in Fig. 12, the suppression effect of the GIDL current after NBS could be achieved by adding positive charges in the gate oxide in 0.5-μm-long regions from the gate edges, and the suppression effect is more effective with the increase in locally distributed positive charges in the gate oxide. For example, with a Q_{ox} of 4.0×10^{17} cm^{-3}, the GIDL current is suppressed to a current level of 5.8×10^{-11} A, which is very close to the measured current of 6.5×10^{-11} A after NBS.

Figure 3(b) shows that the leakage current at V_{ds} of 0.1 V, which is initially thermal generation dominated and gate-bias independent, significantly increases and becomes gate-bias dependent after NBS. Figure 13 compares the drain current, source current (I_s), and gate leakage current (I_g) in the off-state at V_{ds} of 0.1 V after NBS for 7200 s. The drain current and the source current show gate-bias dependence, and the dependence trend is similar to that for the gate leakage current. The sum of drain current and source current equals to the gate leakage current in the off-state. Thus, after NBS, the drain current at V_{ds} of 0.1 V is clearly dominated by the gate leakage current. Considering that the gate leakage current before NBS shows gate-bias independence and as low as 0.1 pA (Fig. 13), the defect-related conduction path in the gate oxide could be concluded to be introduced during NBS, such that the gate leakage becomes larger than the generation current at the drain junction and dominates the drain current at small V_{ds}.

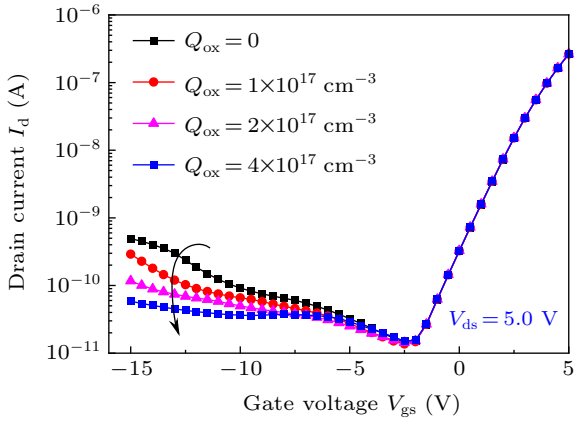


Fig. 12. Suppressed GIDL current in the simulated transfer curves with different Q_{ox} values added in the gate oxide near the source and drain.

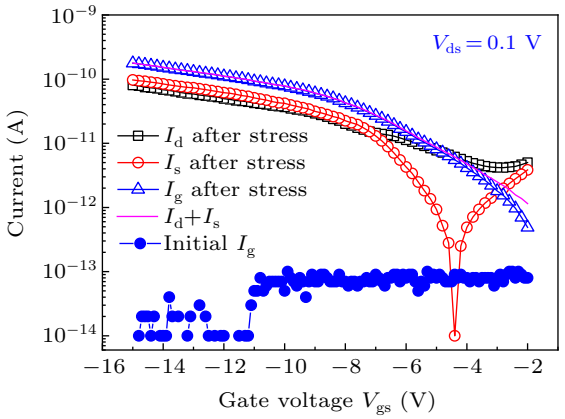


Fig. 13. Comparison of the drain current, source current, and gate leakage current after NBS. The initial gate leakage current before NBS is also shown as a reference.

4. Conclusion

NBS degradation phenomena featured with reduced on-state and GIDL but increased gate bias dependence of the leakage current at V_{ds} of 0.1 V are observed for poly-Si TFTs with a defective GB in the channel. Trap state generation in the GB, local generation of positive charge in the gate oxide near the source/drain, and trap state generation in the gate oxide are proposed to be the respective causes for the observed phenomena. The high-concentration holes in the bulk of the

active island near the source/drain junctions are responsible for the local generation of positive charges in the gate oxide which suppresses the GIDL current. Meanwhile, the low concentration of holes in the bulk of the active island far from the source/drain junctions is proposed to the reason for the absence of the shift of the transfer curve after NBS.

Acknowledgments

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