Dynamic electrostatic-discharge path investigation relied on different impact energies in metal–oxide–semiconductor circuits

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Gate-grounded n-channel metal–oxide–semiconductor (GGNMOS) devices have been widely implemented as power clamps to protect semiconductor devices from electrostatic discharge stress owing to their simple construction, easy triggering, and low power dissipation. We present a novel *I*–*V* characterization of the GGNMOS used as the power clamp in complementary metal–oxide–semiconductor circuits as a result of switching the ESD paths under different impact energies. This special effect could cause an unexpected latch-up or pre-failure phenomenon in some applications with relatively large capacitances from power supply to power ground, and thus should be urgently analyzed and resolved. Transmission-line-pulse, human-body-modal, and light-emission tests were performed to explore the root cause.

Keywords: electrostatic discharge, trigger voltage, latch up, $\mathrm{d}V/\mathrm{d}t$ effect

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1. Introduction

Design of electrostatic discharge (ESD) protection networks that protect semiconductor devices from ESD stress is becoming increasingly difficult for each technology node.[1–4] For general complementary metal–oxide–semiconductor (CMOS) circuits, the protection strategy based on dual diodes and power clamps is the most popular ESD network owing to its simplicity and efficiency. However, this type of circuit should be designed elaborately to avoid latent latch-up (LU) effect reported before.[5,6] With regard to power clamp devices, dynamic floating gate-coupled and resistance-capacity (RC) transient-detect gate-driven n-channel metal oxide semiconductor field effect transistors (MOSFETs) have been widely implemented to lower the trigger voltage and to improve the nonuniformity turn-on problem.[7–10] However, the area consumption and power dissipation of these devices are larger than those of the gate-grounded n-channel MOSFETs (GGNMOS). Therefore, in current engineering applications, a preferable alternative for the power clamp is GGNMOS with a relatively large resistor connecting its gate and source, which simultaneously possesses a lower trigger voltage and lower power dissipation.

The $\mathrm{d}V/\mathrm{d}t$ coupling effect can assist the devices aforementioned to trigger easily, as reported in the previous study,[11] a faster ESD transient with a higher $\mathrm{d}V/\mathrm{d}t$ over the drain-bulk junction capacitances can significantly reduce the effective Vt1 below the junction breakdown. On the other hand, this effect could also result in unexpected latch-up or pre-failure in CMOS circuits.[12,13] In the previous study,[13] researchers have disclosed a failure window phenomenon caused by the $\mathrm{d}V/\mathrm{d}t$ coupling effect under low voltage stresses by setting up some improperly designed structures. However, this failure window can be completely eliminated by using well-designed devices and is not a universal phenomenon in CMOS circuits.

In this work, a novel snapback characterization of the GGNMOS acting as the power clamp is found in ESD transmission-line-pulse (TLP) tests, which is on account of the switch of ESD paths under different impact energies related to the $\mathrm{d}V/\mathrm{d}t$ coupling effect. The unique *I*–*V* curve here is general in many kinds of applications with relatively huge capacitances from power supply voltage (VDD) to ground voltage (VSS) so that it should urgently be analyzed and resolved. TLP, human-body-modal (HBM) and light-emission tests have been carried out to explore the root cause.

2. Circuit framework

Figure 1 shows the partial ESD protection network implemented in this experiment as a typical ESD solution for various CMOS circuits.[14–16] The output of the circuit consists of a pair of laterally diffused MOSFETs (LDMOS) acting as the pull-on transistor (P_LDMOS) and pull-down transistor (N_LDMOS). Generally, conventional output transistors with large device width can protect themselves from ESD stress.[17] However, the big LDMOSs here are incapable of self-protection because of their relatively higher trigger voltage compared to MOSFET devices. Therefore, well-designed ESD protection networks should be applied to efficiently defend the circuits.

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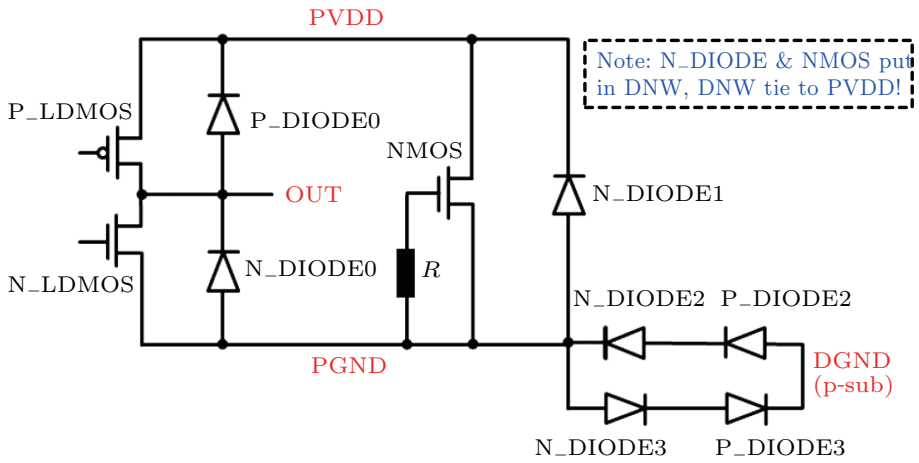


Fig. 1. Partial ESD protection network used in this experiment. PVDD: power device supply, PGND: power device ground, DGND: degital ground.

In this study, a power-clamp-based ESD strategy was implemented. The reverse parasitic diodes of the LDMOSs serve as a pull-on diode (P_DIODE0) and a pull-down diode (N_DIODE0), protecting the LX-PVDD (PD) and PGND-LX (NS) paths, respectively. A GGNMOS (NMOS) with its gate connected to source through a resistance (R) acted as a power clamp device to protect the PVDD-PVSS path while its reverse parasitic diode (N_DIODE1) could also protect the PVSS-PVDD path. Furthermore, two pairs of back-to-back diodes (N_DIODE2 & P_DIODE2, N_DIODE3 & P_DIODE3) were employed here to defend the interface of the PGND and DGND. All the N_DIODEs mentioned were placed in a deep n-well (DNW) tied to PVDD.

3. Results and discussions

The circuit is implemented in the commercial 0.18-μm 5 V bipolar-CMOS-DMOS (BCD) process, and the 100-ns TLP system with 10-ns rise time test, which applies a positive ESD stress at the PVDD with respect to PGND, was carried out to obtain the *I*–*V* curves of the power clamps listed in Table 1. To explore the root case in depth, a new test system comprising the light-emission test and HBM test was set up, which facilitates us to catch the identification of different ESD current paths in the process of the HBM test.

3.1. Novel phenomenon description

The basic circuit in this work, i.e., key 0, listed in Table 1, consists of a GGNMOS with its gate connected to source by a 2.0 kΩ resistance and a pair of LDMOSs with a rated current of 3.0 A. The TLP results in Fig. 2 demonstrate that the *I*–*V* curve measured here is significantly different from that of conventional GGNMOS devices. It exhibits a deep snapback phenomenon similar to a silicon controlled rectifier (SCR) under relatively low ESD stresses, while expressing a normal GGNMOS-like characteristic relatively at approximately 0.5 A. The strange snapback characteristic lead to poor ESD protection effect, besides low holding voltage will cause severe latch-up effect in this 5 V VDD circuit network. Moreover, if the parasitic routes were not robust enough, pre-failure under the ESD stresses could also occur, leading to the full chip ESD performance to deviate from the design drastically. However, this phenomenon is so novel that no work has been reported to explain this principle. Here, we discuss the mechanism of the matter in detail and propose some rational tips to mitigate or even eliminate it.

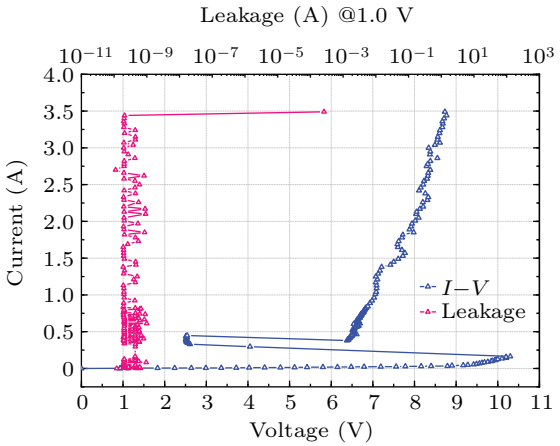


Fig. 2. A deep snapback at approximately 0.5 A found in the TLP *I*–*V* curve of key 0 (with *R* of 2.0 kΩ and rated current of 3.0 A), which will cause the latch-up effect in the 5 V VDD application.

Table 1. Device parameter of circuit.

	Rated current (A)	P_LDMOS total width (μm)	N_LDMOS total width (μm)	Power clamp total width (μm)	Gate resistance (kΩ)
Key 0	3.0	300000	200000	600	2.0
Key 1	3.0	300000	200000	600	0.5
Key 2	1.5	150000	100000	600	2.0
Key 3	3.0	300000	200000	600	1.5

Figure 3 shows the light-emission results of the circuit under different HBM stresses applied at the PVDD to PGND. When applying a 200 V HBM, the energy concentrates on the n-type cathodes of the back-to-back diodes, indicating that the current flows clustering here in the meantime. When the HBM voltage reaches 750 V, the ESD current only discharges through the inverter of the circuit, and the current path in back-to-back diodes disappears. Eventually, with the HBM voltage up to 2000 V, the current will only flow through the elaborately designed power clamp, that is, the GGNMOS device.

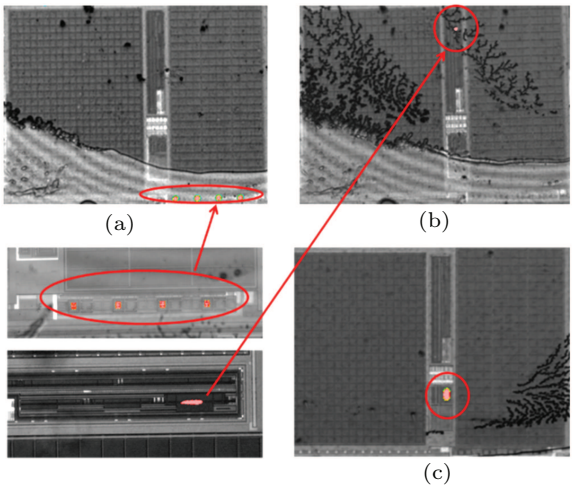


Fig. 3. Light-emission results of key 0 under different HBM stresses applied at the PVDD to PGND: (a) 200 V, the current concentrates on the n-type cathodes of the back-to-back diodes, (b) 750 V, the current only discharges through the inverter of the circuit, (c) 2000 V, the current only flow through the power clamps.

The analysis shows that the peculiar I–V curve is the result of ESD discharge paths switching under different ESD stresses. As shown in Fig. 4, there are three paths participating in the ESD current discharge: the parasitic vertical n–p–n transistor (VNPN) in back-to-back diodes caused by the deep n-well tied to PVDD, the parasitic lateral SCR in the inverters of the circuit, and the well-designed GGNMOS working as the power clamp.

The ESD stress strength will lead to different paths between the PVDD and PGND, and the behaviors of the devices can be analyzed as follows:

(i) When a relatively lower ESD pulse strikes the PVDD with respect to PGND, the VNPN turns on first duo to its relatively lower trigger voltage, namely BV_{ceo} of the vertical transistor whose base is floating now. Consequently, the energy point captured under low HBM stresses is located at the n-type cathodes of the back-to-back diodes.

(ii) When the amplitude of the ESD pulse increases and its rise time remains constant (usually 10-ns for TLP tests), the voltage-to-time ratio $\mathrm{d}V/\mathrm{d}t$, increases, which induces a stronger displacement current from PVDD to PGND through the large capacitance of the output transistors. Because of the existence of substrate resistance, this displacement current rises up the potential of the p-type substrate, promotes the forward bias of the p-sub/n-well junction, and finally accelerates the turn-on of parasitic SCR in inverters,[18] as shown in Fig. 4. Once the SCR is triggered, a strong conductivity modulation effect will occur in its wells and drastically clamping the terminal voltage at a very low level, which could easily shut down the VNPN device. Therefore, the energy point captured under middle HBM stresses is only concentrated at the inverters.

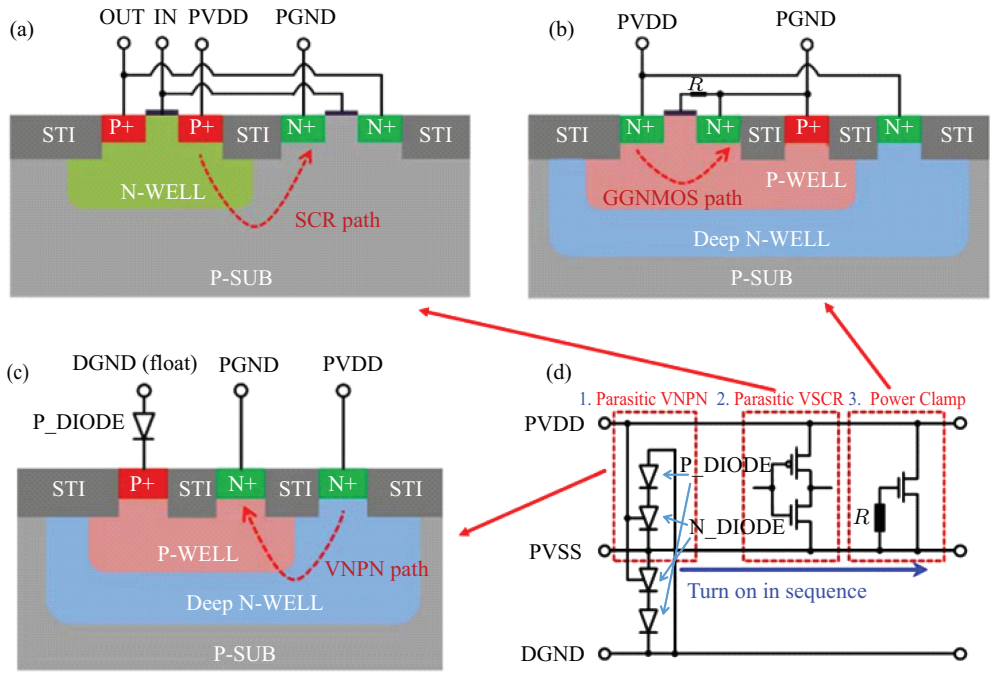


Fig. 4. Simplified cross section for three ESD paths: (a) parasitic SCR, (b) GGNMOS and (c) parasitic vertical NPN transistor; (d) equivalent circuit diagrams for the ESD paths.

(iii) To further improve the HBM voltage, the stronger dv/dt effect leads to a more intense gate-coupled effect in the GGNMOS, which could lower its trigger voltage tempestuously. When the trigger voltage of the GGNMOS is smaller than that of parasitic SCR and VNPN, the GGNMOS will turn on primarily in the HBM process, and once the GGNMOS goes into the snapback state, the SCR and VNPN cannot be triggered anymore unless the terminal voltage once again exceeds the trigger voltage of the GGNMOS at a very high current level.

Figure 5 shows the relative relationship among the trigger voltages of three types of ESD devices. Since each of them has several p–n junction capacitances, they could be more or less affected by the $\mathrm{d}V/\mathrm{d}t$ effect, revealing a relatively lower trigger voltage under larger HBM stresses. Nevertheless, as the GGNMOS has a huge resistance connecting its gate to PGND, the $\mathrm{d}V/\mathrm{d}t$ effect is obviously fiercer than that in the SCR or VNPN.

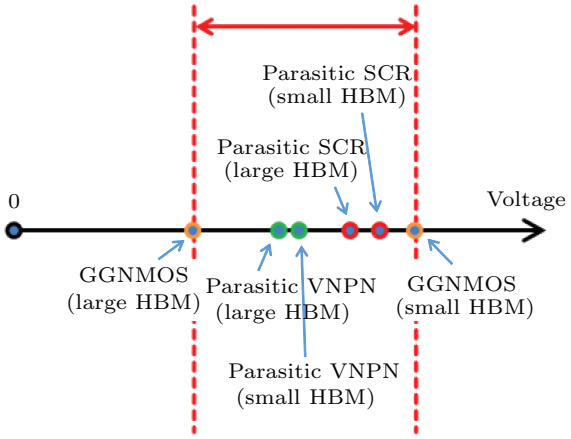


Fig. 5. Relative relationship of the trigger voltage of three types of ESD devices.

3.2. Device parameter influence

The device parameters of the circuit in this study are listed in Table 1 to explore the ESD behavior. The rated current is the normal operating current of the output port in direct proportion to the total device width of the N_LDMOS and P_LDMOS. The power clamp width is the device width of the GGNMOS, which remains constant in this experiment, and the gate resistance is the resist in the GGNMOS which links its gate to PGND.

3.2.1. Impact of resistance

Figure 6 shows the I–V characteristics of key 0 and key 1, which are only different from the size of R in Table 1. The shift current of the former is 0.45 A while the latter is 1.1 A because the resistance between its gate and source is relatively smaller. With a smaller resistor, the gate-coupled effect in the GGNMOS deteriorates.

Therefore, a larger $\mathrm{d}V/\mathrm{d}t$ value is needed to reduce the trigger voltage of GGNMOS to the parasitic SCR's lower level, corresponding to a higher ESD shift current.

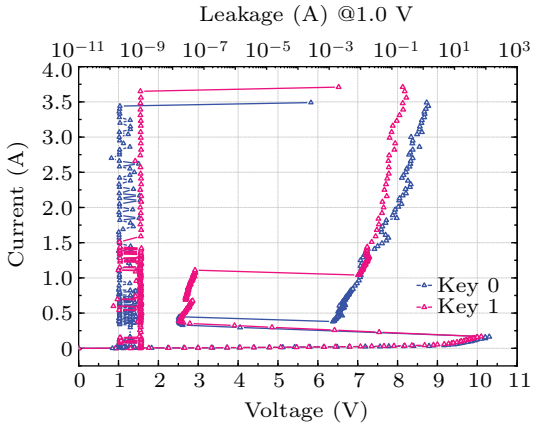


Fig. 6. TLP I–V curves of key 0 (with $R = 2$ kΩ) and key 1 (with $R = 0.5$ kΩ).

3.2.2. Impact of capacitance

Figure 7 shows the I–V characteristics of key 0 and key 2 both with $R = 2.0$ kΩ, which are only different from the total width of P_LDMOS and N_LDMOS in Table 1. Notice that the I–V curve of key 2 behaves like a conventional GGNMOS-like characteristic with a smaller holding current contrasted to the key 0. This is because of the lower rated current level of key 2, i.e., 1.5 A compared to the 3.0 A of key 0, corresponding to smaller layout areas of the N_LDMOS and P_LDMOS. As the capacitance is proportional to the area, smaller areas could decrease the capacitance value between PVDD and PGND, making it more difficult to trigger the parasitic SCR through the substrate current. On the other hand, the smaller capacitance mitigates the delay effect on the ESD pulse and then reinforce the $\mathrm{d}V/\mathrm{d}t$ effect in the GGNMOS.[13] The synthetical influence of these two effects makes the GGNMOS turn on more easily than the parasitic SCR. The normal I–V curve indicates that the ESD current discharges only through the GGNMOS device at this moment regardless of the ESD energies, which can be testified by Fig. 8. Figure 8 shows the light-emission results of key 2 under different HBM stresses applied at the PVDD to PGND, exhibiting the same ESD paths under the 200 V and 2000 V HBM stresses.

Apparently, the above discussion provides two solutions to this unexpected problem that we can enlarge the gate resistance of the GGNMOS or decrease the layout area of the output transistors to promote the turn-on of the GGNMOS while suppressing the parasitic SCR simultaneously. Besides increasing the gate resistance to reduce the trigger voltage of GGNMOS, we can also optimize the paths of the parasitic devices when dealing with an output port with fixed-sized output transistors, considering the device performance. For example, we can add multiple guard rings or magnify the active area width of single guard ring between PMOS and NMOS in the inverter and put the NMOS into the deep N-well to efficiently stifle the latent latch-up effect caused by the parasitic SCR.[5,6]

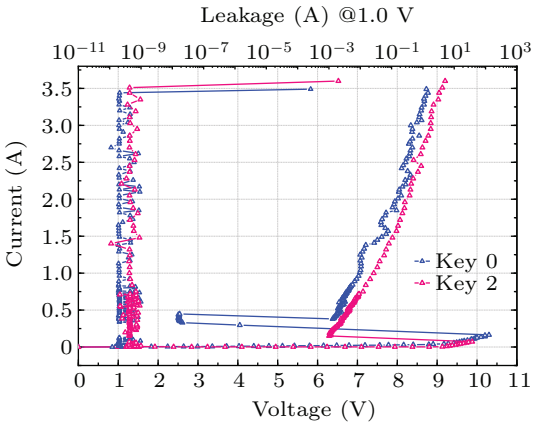


Fig. 7. TLP *I*–*V* curves of key 0 (with related current 3.0 A) and key 2 (with related current 1.5 A), which are only different from the total width of P_LDMOS and N_LDMOS.

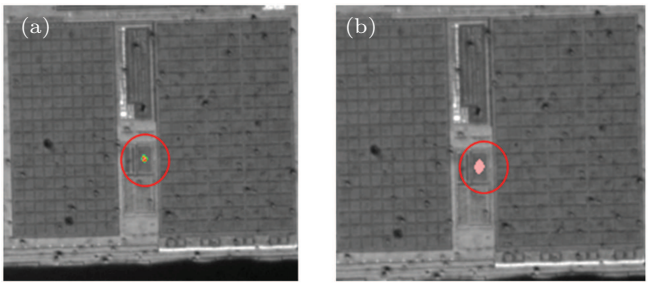


Fig. 8. Light-emission results of key 2 (with related current 1.5 A) under different HBM stresses applied at the PVDD to PGND (a) 200 V and (b) 2000 V, exhibiting the same GGNMOS ESD paths.

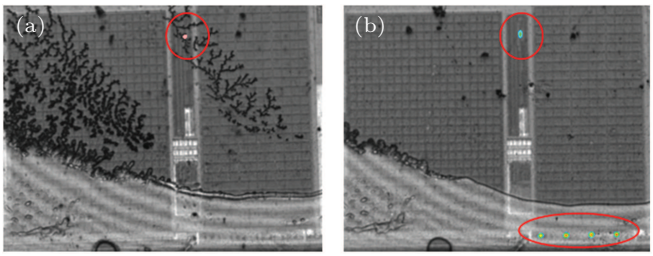


Fig. 9. Light-emission results of key 1 (with $R = 0.5$ kΩ) under different HBM stresses applied at the PVDD to PGND: (a) 300 V, the current is at the inverter; (b) 750 V, the current is at both the inverter and the back-to-back diodes.

A strange phenomenon was observed in the light-emission test under the HBM stress as shown in Fig. 9. When applying a lower HBM stress (300 V in this experiment) at the PVDD of key 1 (with $R = 0.5$ kΩ), the energy point is only located at the inverter. However, when applying a higher HBM stress (750 V in this experiment) the energy points are located at both the inverter and the back-to-back diodes. Here, there seems to be a contradiction between this phenomenon and the aforementioned analysis where we have demonstrated that the VNPNs turn on in the earlier time at relatively lower HBM stresses compared to the parasitic SCR. Actually, this is caused by the difference in the capture time. When the HBM stress rises to a level that can trigger the SCR path, both the VNPN and SCR can discharge ESD current in earlier times of the HBM process, while only the SCR contributes to the conduct current after it snaps back relatively in later times of the HBM process. Therefore, the capture time of the 750 V-HBM stress is earlier than that of the 300 V-HBM stress when both of the SCR and VNPN are exhausting the ESD currents.

3.2.3. Influence of rise time

According to the above discussion, the novel snapback characteristic proposed in this study is caused by the $\mathrm{d}V/\mathrm{d}t$ effect which has the most significant impact on the GGNMOS because of the large resistance between its gate and source. Then a deduction can be induced such that, if a larger $\mathrm{d}V/\mathrm{d}t$ value can be enabled at the same current level, the current of the turning point will decrease accordingly. A reasonable manipulation is to reduce the rise time of the TLP pulse which could increase the $\mathrm{d}V/\mathrm{d}t$ value under the same voltage amplitudes.[11] As shown in Fig. 10, when apply TLP pulses with 10-ns and 2-ns rise time to PVDD with respect to PGND, the shift current of the latter drops about 0.3 A, indicating that the GGNMOS device turns on more easily than before.

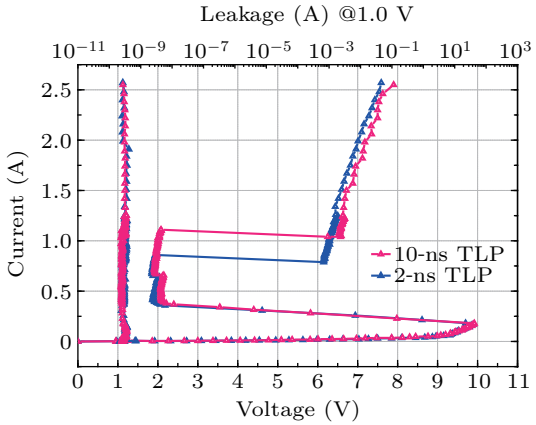


Fig. 10. TLP *I*–*V* curves of key 1 under the 10-ns and 2-ns rise-time tests, respectively, observing a shift current drop.

4. Conclusion

In summary, a novel snapback characteristic of the GGNMOS device used as the power clamp in CMOS circuits has been proposed with a relatively big capacitance between the VDD and GND. TLP and light-emission tests have shown that the unique phenomenon is caused by the competition between the GGNMOS and other parasitic ESD paths in the circuits as a result of the transient $\mathrm{d}V/\mathrm{d}t$ effect during ESD tests. As the capacitance between the VDD and GND becomes increasingly higher in advanced nanoscale CMOS processes, this special *I*–*V* characteristic will become unavoidable and will introduce unexpected problems, such as latch-up and pre-failure. Co-design of the ESD network and the internal functional circuits, as well as the ESD circuit-level modeling with the transient $\mathrm{d}V/\mathrm{d}t$ effect, are indispensable to relieve or even eliminate this phenomenon.

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