

An integrated split and dummy gates MOSFET with fast turn-off and reverse recovery characteristics

Weizhong Chen(陈伟中), Liuting Mou(牟柳亭), Haifeng Qin(秦海峰), Hongsheng Zhang(张红升), and Zhengsheng Han(韩郑生)

Citation: Chin. Phys. B, 2023, 32 (**6**): 067303. DOI: 10.1088/1674-1056/ac9045
Journal homepage: http://cpb.iphy.ac.cn; http://iopscience.iop.org/cpb

What follows is a list of articles you may be interested in

Impact of low-dose radiation on nitrided lateral 4H-SiC MOSFETs and the related mechanisms

Wen-Hao Zhang(张文浩), Ma-Guang Zhu(朱马光), Kang-Hua Yu(余康华), Cheng-Zhan Li(李诚瞻),Jun Wang(王俊), Li Xiang(向立), and Yu-Wei Wang(王雨薇)
Chin. Phys. B, 2023, 32 (**5**): 057305. DOI: 10.1088/1674-1056/acbd2e

Design and research of normally-off β-Ga_2O_3/4H-SiC heterojunction field effect transistor

Meixia Cheng(程梅霞), Suzhen Luan(栾苏珍), Hailin Wang(王海林), and Renxu Jia(贾仁需)
Chin. Phys. B, 2023, 32 (**3**): 037302. DOI: 10.1088/1674-1056/aca39c

Degradation and breakdown behaviors of SGTs under repetitive unclamped inductive switching avalanche stress

Chenkai Zhu(朱晨凯), Linna Zhao(赵琳娜), Zhuo Yang(杨卓), and Xiaofeng Gu(顾晓峰)
Chin. Phys. B, 2022, 31 (**9**): 097303. DOI: 10.1088/1674-1056/ac615b

Study on a novel vertical enhancement-mode Ga_2O_3 MOSFET with FINFET structure

Liangliang Guo(郭亮良), Yuming Zhang(张玉明), Suzhen Luan(栾苏珍), Rundi Qiao(乔润迪), and Renxu Jia(贾仁需)
Chin. Phys. B, 2022, 31 (**1**): 017304. DOI: 10.1088/1674-1056/ac21c4

Investigation on threshold voltage of p-channel GaN MOSFETs based on p-GaN/AlGaN/GaN heterostructure

Ruo-Han Li(李若晗), Wu-Xiong Fei(费武雄), Rui Tang(唐锐), Zhao-Xi Wu(吴照玺), Chao Duan(段超), Tao Zhang(张涛), Dan Zhu(朱丹), Wei-Hang Zhang(张苇杭), Sheng-Lei Zhao(赵胜雷), Jin-Cheng Zhang(张进成), and Yue Hao(郝跃)
Chin. Phys. B, 2021, 30 (**8**): 087305. DOI: 10.1088/1674-1056/ac0793

An integrated split and dummy gates MOSFET with fast turn-off and reverse recovery characteristics

Weizhong Chen(陈伟中)[1,2], Liuting Mou(牟柳亭)[1,†], Haifeng Qin(秦海峰)[1], Hongsheng Zhang(张红升)[1], and Zhengsheng Han(韩郑生)[2,3]

[1] *College of Electronics Engineering, Chongqing University of Posts and Telecommunications, Chongqing* 400065, *China*
[2] *Institute of Microelectronics of Chinese Academy of Sciences, Beijing* 100029, *China*
[3] *Department of Microelectronics, University of Chinese Academy of Sciences, Beijing* 100049, *China*

(Received 29 April 2022; revised manuscript received 5 September 2022; accepted manuscript online 8 September 2022)

A power MOSFET with integrated split gate and dummy gate (SD-MOS) is proposed and demonstrated by the TCAD SENTAURUS. The split gate is surrounded by the source and shielded by the dummy gate. Consequently, the coupling area between the split gate and the drain electrode is reduced, thus the gate-to-drain charge (Q_{GD}), reverse transfer capacitance (C_{RSS}) and turn-off loss (E_{off}) are significantly decreased. Moreover, the MOS-channel diode is controlled by the dummy gate with ultra-thin gate oxide t_{ox}, which can be turned on before the parasitic P-base/N-drift diode at the reverse conduction, then the majority carriers are injected to the N-drift to attenuate the minority injection. Therefore, the reverse recovery charge (Q_{RR}), time (T_{RR}) and peak current (I_{RRM}) are effectively reduced at the reverse freewheeling state. Additionally, the specific on-resistance ($R_{on,sp}$) and breakdown voltage (BV) are also studied to evaluate the static properties of the proposed SD-MOS. The simulation results show that the Q_{GD} of 6 nC/cm^2, the C_{RSS} of 1.1 pF/cm^2 at the V_{DS} of 150 V, the Q_{RR} of 1.2 μC/cm^2 and the $R_{on,sp}$ of 8.4 mΩ·cm^2 are obtained, thus the figures of merit (FOM) including $Q_{GD} \times R_{on,sp}$ of 50 nC·mΩ, $E_{off} \times R_{on,sp}$ of 0.59 mJ·mΩ and the $Q_{RR} \times R_{on,sp}$ of 10.1 μC·mΩ are achieved for the proposed SD-MOS.

Keywords: MOSFET, split gate, dummy gate, turn-off, and reverse recovery

PACS: 73.40.Qv, 85.30.De, 85.30.Tv, 51.50.+v **DOI:** 10.1088/1674-1056/ac9045

1. Introduction

The metal–oxide–semiconductor field effect transistor (MOSFET) with parasitic built-in P-base/N-drift PN junction diode plays a particularly important role in the consumer electronics and industrial bridge circuits.[1,2] The static properties including BV and $R_{on,sp}$ determine the voltage rating and conduction energy loss,[3–6] and the dynamic performances including Q_{GD}, E_{off}, and Q_{RR} determine the frequency and turn-off energy loss. Consequently, the FOM including $Q_{GD} \times R_{on,sp}$, $E_{off} \times R_{on,sp}$ and $Q_{RR} \times R_{on,sp}$ are extracted to evaluate the trade-off characteristics.[7–9] For the conventional MOSFET, the switching frequency is constrained by the reverse transfer capacitance (C_{RSS}), which is mainly composed of the gate oxide capacitance (C_{ox}) and the silicon depletion region capacitance (C_{dep}).[10] Then the advanced split gate Si/SiC MOSFET (SG-MOS) is proposed to reduce the C_{RSS} by the decrease of the coupling area between the gate and the drain electrodes. However, the BV and reliability are decreased by the SG structure, which leads to the crowded electric field at the silicon surface.[11–13] Additionally, the conventional device with poor reverse recovery property is also needed to be further improved. The excessive minority carriers Q_{RR} are injected in the N-drift by the parasitic P-base/N-drift (PN junction diode) at the reverse conduction, which leads to the high switching energy loss and strong current stress. Then the Schottky junction diode and external anti-parallel diodes are proposed to solve the issues.[13–16] The MOS-channel diode can effectively control the injection of the minority carriers and decrease the reverse recovery charge (Q_{RR}), which is widely used in power devices including rectifier in the recent years.[17–21]

In this paper, a power MOSFET with the integration of the trench split gate and dummy gate (SD-MOS) is proposed to improve the dynamic properties by the decrease of the gate-to-drain charge (Q_{GD}), turn-off energy loss (E_{off}) and reverse recovery charge (Q_{RR}). The simulation electrical behaviors and working mechanisms are investigated by the TCAD SENTAURUS, where physics models including the EffecticeIntrinsicDensity, Mobility (HighFieldSaturation Enormal PhuMob DopingDependence), Recombination (SRH Auger Avalanche) are adopted.[23]

2. Structure and mechanism

The structures for the SG-MOS with planar split gate in Ref. [11], the power MOSFET with built-in channel diode (BD-MOS) in Ref. [22], and the proposed SD-MOS with integrated split and dummy gates are compared, as shown in the Fig. 1. The devices are designed for 200 V breakdown voltage rating, and the doping concentration of the JFET and N-drift for the devices are 1.0×10^{16} cm^{-3} and 9.0×10^{14} cm^{-3}, re-

†Corresponding author. E-mail: 1005205632@qq.com

© 2023 Chinese Physical Society and IOP Publishing Ltd

spectively. The length of the N-drift and the width of the cell size are 16 μm and 7.6 μm, respectively. The width of the P-base and the JFET are 2.3 μm and 3 μm, respectively. In addition, the gate oxide thickness of the split gate and dummy gate are 100 nm and 16 nm for the BD-MOS and the SD-MOS, respectively. The device parameters are summarized in Table 1.

For the SG-MOS, the planar split gate is divided into two parts and the gap between the gates is 2.2 μm as shown in Fig. 1(a). For the BD-MOS, one of the planar MOS cells is replaced by the MOS-channel diode with short contacted source and dummy gate, and the current density will be inevitably reduced at the on-state as shown in Fig. 1(b). For the proposed SD-MOS, the trench split gate is surrounded by the source and shielded by the dummy gate. Moreover, the MOS-channel diode is controlled by the dummy gate with ultra-thin gate oxidet_{ox} as shown in Fig. 1(c), and the corresponding equivalent circuit at the on-state and reverse freewheeling state is shown in Fig. 1(d). At the forward conduction, the double MOS-channel diodes are turned off, and the equivalent circuit is similar to those of the conventional MOSFET, which the majority current I_{DS} flows from the drain and the source passing through the JFET region. At the reverse conduction, the double MOS-channel diodes are easily turned on with majority current I_{MOS}, and then the minority current I_{PN} is also conducted by the parasitic P-base/N-drift PN diode. The ratio between the I_{MOS} and the I_{PN} is adjusted by the turn on voltage V_{turn} of the MOS diode through the dummy gate oxide thickness t_{ox}. Therefore, the reverse recovery charge (Q_{RR}) is decreased by the suppress of the minority injection of the I_{PN}. Additionally, the coupling area between the trench split gate and the drain is also reduced by the shielding effect of the dummy gate of the MOS-channel diode, thus the reverse transfer capacitance (C_{RSS}), gate-to-drain charge (Q_{GD}) and turn-off energy loss (E_{off}) are remarkably decreased to improve the switching performance.

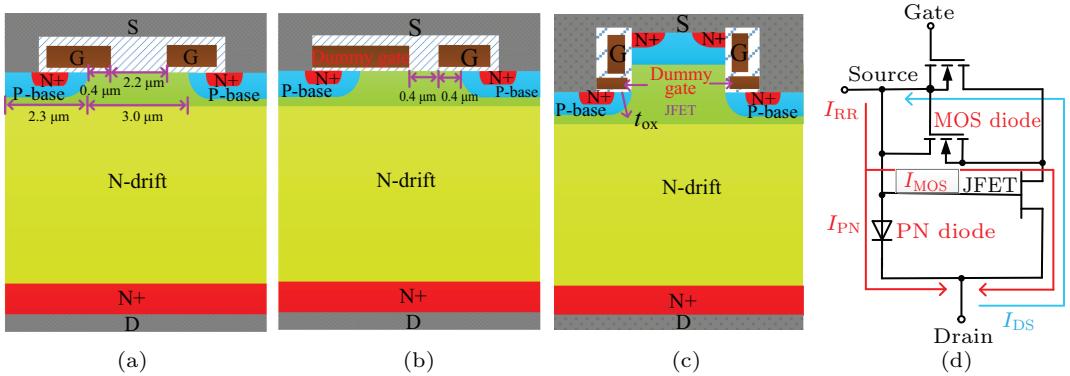


Fig. 1. The cross-sectional view of schematic and equivalent circuit for the devices. (a) The SG-MOS with planar split gate. (b) The BD-MOS with independent split and dummy gates. (c) The SD-MOS with integrated split and dummy gates. (d) The equivalent circuit (the MOS-channel diodes are turned on before the P-base/N-drift diode, and the V_{turn} is lower than the V_{PN}, the I_{DS} and I_{RR} are the forward and reverse conduction currents, respectively).

Table 1. Device parameters of the SG-MOS, BD-MOS and SD-MOS.

Symbol	Description	SG-MOS	BD-MOS	SD-MOS
W_{drift}	N-drift width (μm)	7.6	7.6	7.6
W_{P-base}	P-base width (μm)	4.6	4.6	4.6
W_{JFET}	JFET width (μm)	3	3	3
W_G	planar split gate gap width (μm)	2.2	0.4	–
L_D	N-drift length (μm)	16	16	16
T_{GO}	split gate oxide layer thickness (μm)	–	0.1	0.1
t_{ox}	dummy gate oxide layer thickness (μm)	–	0.016	0.016
N_{drift}	N-drift region doping (cm^{-3})	9×10^{14}	9×10^{14}	9×10^{14}
N_{JFET}	JFET doping (cm^{-3})	1×10^{16}	1×10^{16}	1×10^{16}

3. Results and discussion

Figure 2 demonstrates the static characteristics of the devices, and they are designed for 200 V voltage rating. The breakdown voltage (BV) and specific on-resistance ($R_{on,sp}$) are optimized by the doping of the N-drift as shown in Fig. 2(a). The BV is decreased with the increase of the N_{drift}, because the BV is mainly determined by the electric field E_{field} of the N-drift, and the E_{field} will be stopped and the expansion of the depletion region will be prevented by the increased N_{drift}. Moreover, the $R_{on,sp}$ is also decreased with the increased N_{drift} due to the decreased resistance R_{drift}. The four devices are compared at the N_{drift} of 9×10^{14} cm^{-3} according to Ref. [22], and the $R_{on,sp}$ of the C-MOS, SG-MOS and the SD-MOS are 8.2 mΩ·cm^2, 8.3 mΩ·cm^2 and 8.4 mΩ·cm^2, respectively. However, the BD-MOS is conducted with single channel because of the replacement of the MOS-channel diode, thus the

bigger $R_{on,sp}$ of 8.7 mΩ·cm^2 is achieved. The corresponding on-state output I–V curves are compared in Fig. 2(b), and it can be seen that the BD-MOS conducts the smallest drain current I_{DS} at the temperature of 300 K. The I_{DS} of the proposed SD-MOS will be decreased when the temperature increases from 300 K to 400 K, because the lattice scattering effect is enhanced, which leads to the decrease of the electron mobility.

In addition, the BV of the C-MOS, SG-MOS, BD-MOS and SD-MOS are 229 V, 193 V, 229 V and 235 V at the same N_{drift} of 9×10^{14} cm^{-3}, respectively. The corresponding breakdown characteristics and electric field E_{field} distribution are compared in Figs. 2(c) and 2(d), respectively. The leakage current of the proposed SD-MOS is increased obviously with the increase of the temperature, because the impact ionization rate and avalanche current are enhanced by the arising temperature. Moreover, there is no surface E_{field} for the proposed SD-MOS, and the maximum E_{field} is sustained by the P-base/N-drift junction at the JFET region.

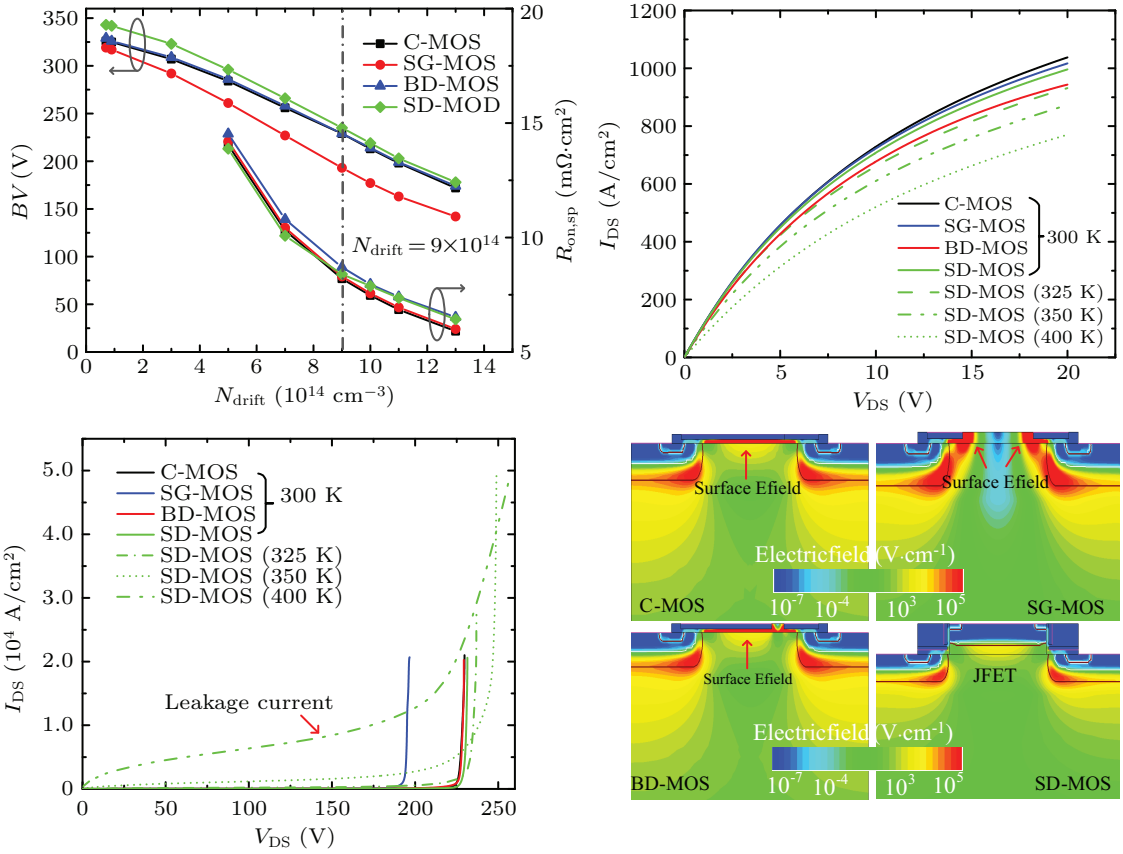


Fig. 2. The static characteristics for the four devices. (a) The variation of the BV and $R_{on,sp}$ by the optimization of the $N_{drift.}$ (b) The on-state output conduction property. (c) The off-state breakdown properties. (d) The electric filed distribution at the temperature of 300 K.

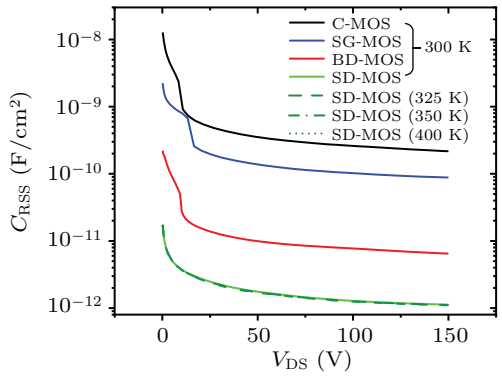


Fig. 3. The C_{RSS} aviation with the V_{DS} at the temperature of 300 K for the four devices, and the C_{RSS} is almost not changed when the temperature increases from 300 K to 400 K.

Figure 3 shows the reverse transfer capacitance (C_{RSS}) property for the devices. The coupling C_{RSS} is the sum of the overlap capacitance C_{ox} and the depleted capacitance C_{dep}. It is obviously decreased with the increased V_{DS} and then keep almost constant for all the devices, because the C_{dep} decreases abruptly with the expansion of the depletion region. However, the C_{ox} is constant and determined by the overlapping area between the gate and drain electrodes. As a result, the C_{RSS} at the V_{DS} of 150 V for the SG-MOS (88 pF/cm^2) and BD-MOS (11 pF/cm^2) are effectively decreased compared with C-MOS (217 pF/cm^2), due to the coupling area between the gate and the drain is remarkably reduced by the introduction of the split gate. The proposed SD-MOS achieves the minimum C_{RSS} of 1.1 pF/cm^2, because the coupling area is further reduced by the shielding effect of dummy gate of the MOS-channel diode. Additionally, the C_{RSS} is not correlated with the temperature.

Figure 4 shows the testing circuit and the gate charge

(Q_G) for the structures. The devices are tested at the same circuit as shown in Fig. 4(a) and the Miller platform Q_{GD} which stored in the C_{RSS} of the C-MOS, SG-MOS, BD-MOS and SD-MOS are 154 nC/cm^2, 82 nC/cm^2, 19 nC/cm^2 and 6 nC/cm^2 as shown in Fig. 4(b), respectively. The excellent Q_{GD} and the improved switching characteristics are achieved by the SD-MOS due to the smallest C_{RSS} as illustrated in Fig. 3. In addition, the Q_G is mainly stored in the C_{RSS} and C_{GS}, and the overlap area between the trench split gate and source of the SD-MOS is increased. Consequently, the C_{GS} is increased. Thus the Q_G of the SD-MOS is slightly bigger than those of the BD-MOS, and the Q_G of the C-MOS, SG-MOS, BD-MOS and SD-MOS are 340 nC/cm^2, 196 nC/cm2, 88 nC/cm^2, and 92 nC/cm^2, respectively.

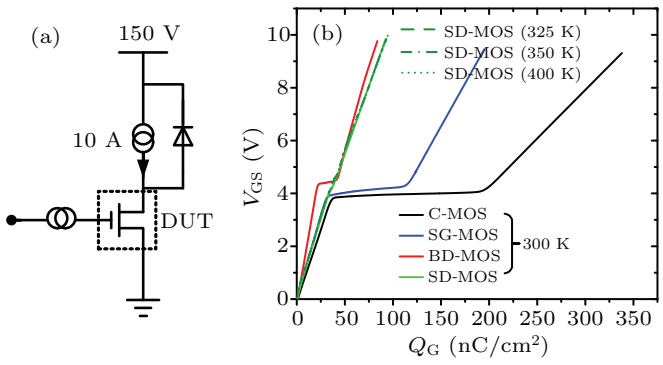


Fig. 4. The gate charge Q_G for the devices. (a) Testing circuit. (b) The V_{GS}–Q_G characteristics, and the Q_{GD} is almost not changed when the temperature increases from 300 K to 400 K.

Figure 5 demonstrates the turn-off characteristics including the testing circuit and switching waveform for the devices. They are all turned off at the same inductive load circuit as shown in Fig. 5(a), and the corresponding dynamic drain current (I_{DS}) and voltage (V_{DS}) variation with turn-off time are shown in Fig. 5(b). The BD-MOS, SG-MOS and SD-MOS are with split gate, which improves the T_{off} and E_{off} significantly compared with the C-MOS without split gate. The T_{off} of the C-MOS, SG-MOS, BD-MOS and SD-MOS are 109 ns, 91 ns, 26 ns and 13 ns, respectively. Moreover, the E_{off} of the devices are 0.75 mJ/cm^2, 0.61 mJ/cm^2, 0.18 mJ/cm^2 and 0.07 mJ/cm^2, respectively. The ultra-low T_{off} and E_{off} are achieved by the SD-MOS with the integrated trench split and dummy gates.

Additionally, the T_{off} of the SD-MOS is slightly increased when the temperature increases from 300 K to 400 K as shown in Fig. 5(c). It is because the lattice scattering effect under high temperature is enhanced.

Figure 6 exhibits the reverse conduction property and mechanism for the anti-parallel diodes. The four devices are with parasitic P-base/N-drift (PN junction diodes) with turn-on V_{PN} of 0.6 V, and the minority carriers (holes) are injected into the N-drift by the P-base. However, another single MOS-channel diode with lower turn-on voltage V_{turn} (0.5 V) is designed for the BD-MOS with dummy gate oxide t_{ox} of 16 nm. It is triggered before the PN diode, and abundant majority (electrons) are injected into the N-drift from the N+ source. The SD-MOS with double MOS-channel diodes are designed, and the V_{turn} is further decreased to 0.4 V at the t_{ox} of 12 nm as shown in Fig. 6(a), then the majority carriers injection is further enhanced at the JFET regions to attenuate the minority density. The comparison of the hole density at the at the same I_{SD} of 100 A/cm^2 is illustrated in Fig. 6(b). It can be seen that the minority is remarkably reduced for the BD-MOS, and it is further significantly decreased for the SD-MOS because of the turn on of the MOS-channel diodes. The temperature influence on the reverse conduction capability of the SD-MOS is demonstrated in Figs. 6(c) and 6(d), and the reverse current is improved when the temperature increases from 300 K to 400 K.

Figure 7 shows the reverse recovery testing circuit and performances for the devices. The C-MOS and SG-MOS are conducted with abundant and excess minority carriers (holes) Q_{RR} in the N-drift, which are injected by the parasitic PN junction diode at the reverse conduction as shown Fig. 6(b). However, the Q_{RR} is remarkably reduced by the MOS-channel diode for the BD-MOS and SD-MOS, thus the reverse recovery current is effectively decreased as shown in Fig. 7(b). The temperature influence on the reverse recovery capability of the SD-MOS is investigated in Fig. 7(c), and the biggest Q_{RR} is observed at the temperature of 400 K because of the abundant excessive carriers are stored in the N-drift as shown in Fig. 6(d).

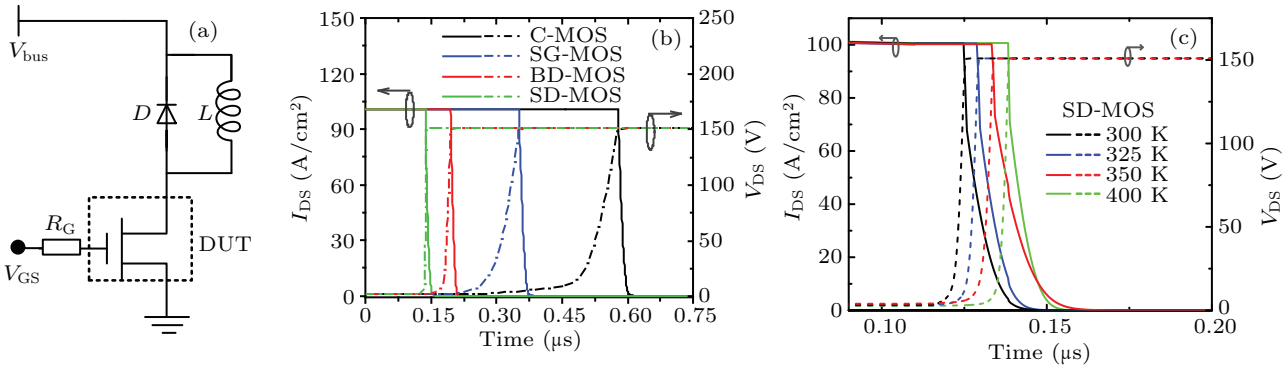


Fig. 5. The turn-off characteristics for the devices. (a) Testing circuit. (b) The dynamic switching waveform. The chip area of the DUT is set as 1 cm^2, and the R_G, V_{bus} and L are 10 Ω, 150 V and 4 mH, respectively. (c) The switching waveform aviation with the temperature from 300 K to 400 K of the SD-MOS.

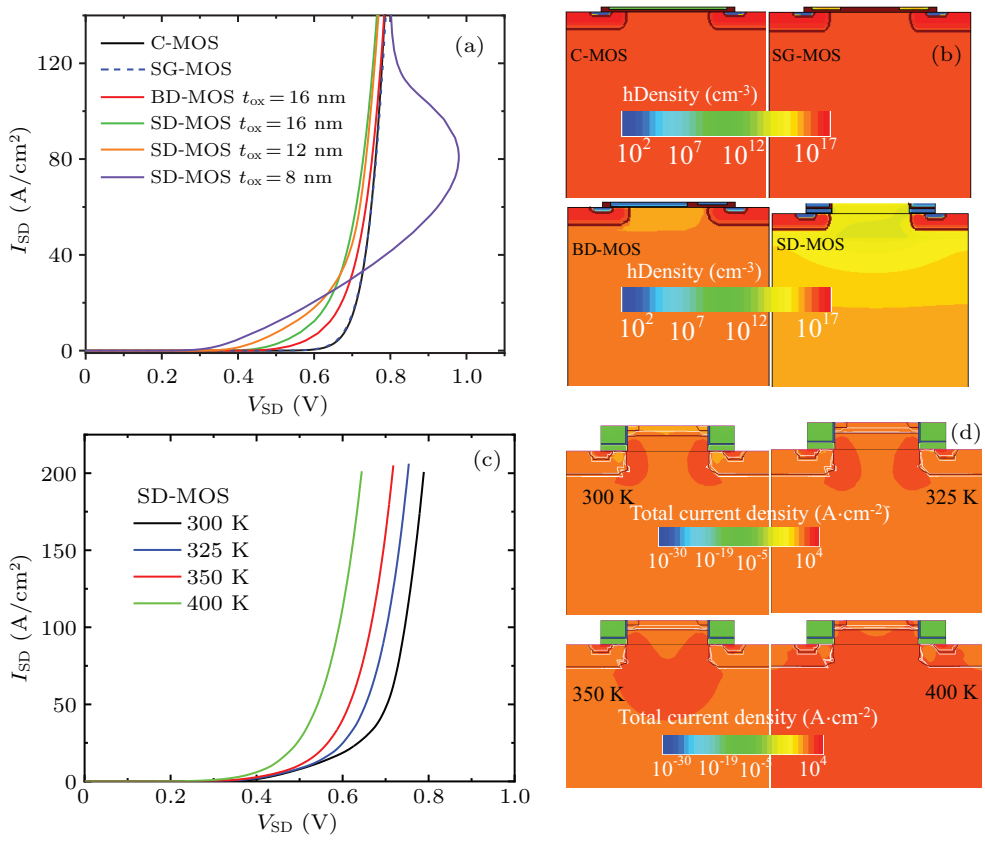


Fig. 6. The reverse conduction performances. (a) The I_{SD}–V_{SD} curves. (b) Minority carrier distribution at the I_{SD} of 100 A/cm^2. (c) The I_{SD}–V_{SD} curves aviation with the temperature from 300 K to 400 K of the SD-MOS. (d) The total current density distribution at different temperature of the SD-MOS.

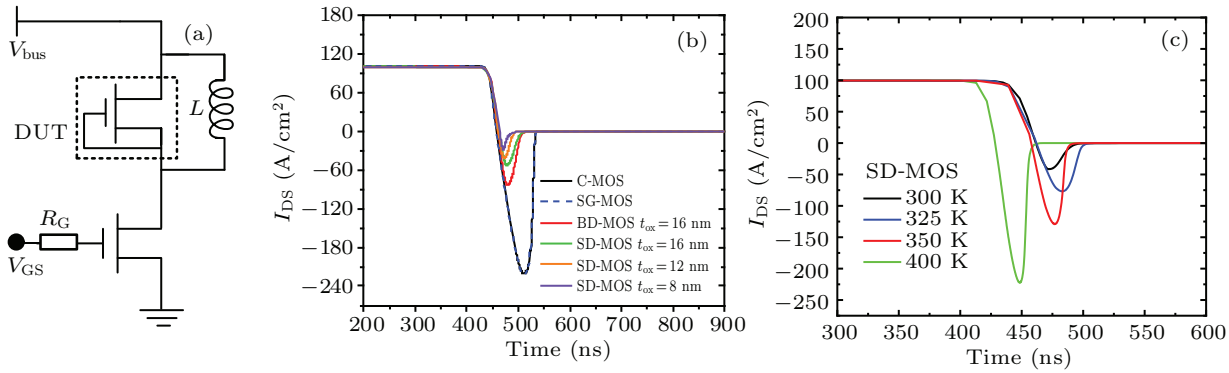


Fig. 7. The reverse recovery performances for the devices. (a) Testing circuit. (b) The I_{SD-t} characteristics. The chip area of the DUT is set as 1 cm^2, The RG, V_{bus} and L are 10 Ω, 150 V and 10 μH, respectively. (c) The reverse recovery aviation with the temperature from 300 K to 400 K of the SD-MOS.

Finally, the important performances and trade-off relationship between the static and dynamic characteristics of the four devices are listed in Table 2. The best FOM of $Q_{GD} \times R_{on,sp}$, $E_{off} \times R_{on,sp}$ and $Q_{RR} \times R_{on,sp}$ are achieved by the proposed SD-MOS.

Figure 8 shows the simplified fabrication sequence of the proposed SD-MOS. The JFET region is grew by the epitaxy technique as shown in Fig. 8(a). The JFET is etched, and the P-base and N+ source are respectively performed by the boron and arsenic implantation as shown in Fig. 8(b). The oxidation is deposited as shown in Fig. 8(c). The oxidation is etched, and the gate of the MOS-channel diode is deposited by the polysilicon as shown in Fig. 8(d). The trench gate with gate oxide are formed by the oxidation and polysilicon deposition as shown in Fig. 8(e). The metallization of the source and drain electrode is formed by the deposition as shown in Fig. 8(f).

Table 2. Comparison of the device characteristics.

	C-	SG-	BD-	Proposed	Unit
BV	229	229	193	235	V
$R_{on,sp}$	8.2	8.3	8.7	8.4	mΩ·cm^2
Q_G	340	192	88	92	nC/cm^2
Q_{GD}	154	82	19	6	nC/cm^2
C_{RSS}	217	88	11	1.1	pF/cm^2
Q_{RR}	10.5	10.5	2.0	1.2	μC/cm^2
I_{RRM}	220	220	83	52	A/cm^2
T_{RR}	74	74	46	42	ns
T_{off}	109	91	26	13	ns
E_{off}	0.75	0.61	0.18	0.07	mJ/cm^2
$Q_{GD} \cdot R_{on,sp}$	1262	680	165	50	nC·mΩ
$E_{off} \cdot R_{on,sp}$	6.15	5.06	1.57	0.59	mJ·mΩ
$Q_{RR} \cdot R_{on,sp}$	86.1	87.2	17.4	10.1	μC·mΩ

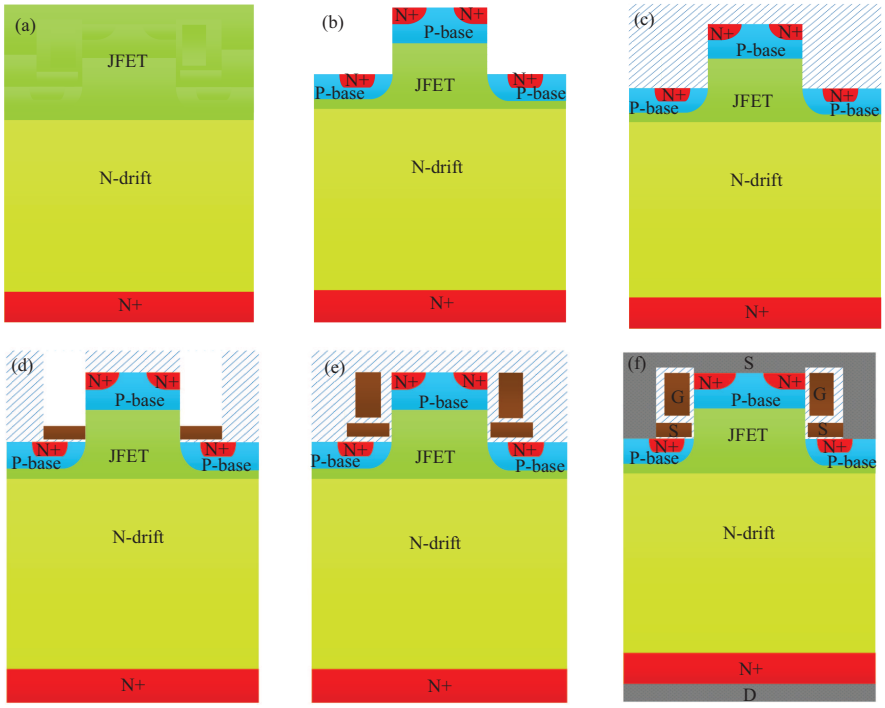


Fig. 8. Simplified key process. (a) JFET growth, (b) trench etching, boron and arsenic implantation, (c) oxidation, (d) trench etching, polysilicon deposition, (e) trench polysilicon deposition, and (f) electrode deposition.

4. Conclusion

A power MOSFET with the integrated trench split and dummy gates is demonstrated. The split gate is shielded by the shortly contacted source and dummy gate, which can remarkably reduce the C_{RSS} and Q_{GD} due to the decrease of the coupling area between the split gate and the drain electrode, thus the superior switching characteristics is achieved. The MOS-channel diode is formed and controlled by the dummy gate, which the lower V_{turn} are turned on before the parasitic PN junction diode, thus can obviously suppress the minority Q_{RR} injection of the P-base, and the excellent reverse recovery performances is achieved. The results show that the FOM of $Q_{\mathrm{GD}} \times R_{\mathrm{on,sp}}$, $E_{\mathrm{off}} \times R_{\mathrm{on,sp}}$ and the $Q_{\mathrm{RR}} \times R_{\mathrm{on,sp}}$ of the proposed SD-MOS are decreased by 69%, 62% and 42%, respectively, when compared with the advanced BD-MOS.

Acknowledgements

Project supported by the National Natural Science Foundation of China (Grants No. 61604027 and 61704016) and the Chongqing Natural Science Foundation, China (Grant No. cstc2020jcyj-msxmX0550).

References

[1] Yang B, Wang J, Xu S, Korec J and Shen Z J 2013 *IEEE Trans. Power Electron.* **28** 4202
[2] Saxena R S and Kumar M J 2009 *IEEE Trans. Electron Devices* **56** 1355
[3] Saxena R S and Kumar M J 2009 *IEEE Electron Device Lett.* **30** 990
[4] Chen W, Qin H, Huang Y, Huang Y and Han Z 2021 *IEEE Trans. Electron Devices* **68** 6286
[5] Chen W, Qin H, Zhang H and Han Z 2022 *IEEE Trans. Electron Devices* **69** 1900
[6] Wang Y, Hu H, Jiao W and Cheng C 2010 *IEEE Electron Device Lett.* **31** 338
[7] Saxena R S and Kumar M J 2009 *IEEE Trans. Electron Devices* **56** 1355
[8] Jiang Q, Wang M and Chen X 2010 *IEEE Trans. Electron Devices* **57** 1972
[9] Cheng X, Sin J K O, Kang B, Feng C, Wu Y and Liu X 2003 *IEEE Trans. Electron Devices* **50** 1422
[10] Xu S, Ren C, Liang Y. C, Foo P and Sin J K O 2001 *IEEE Trans. Electron Devices* **48** 2168
[11] Ng J C W and Sin J K O 2009 *IEEE Trans. Electron Devices* **56** 1761
[12] Xu S, Can K, Foo P, Su Y and Liu Y 2000 *IEEE Electron Device Lett.* **21** 176
[13] Wei J, Zhang M, Jiang H, Zhou X, Li B and Chen K J 2019 *IEEE Electron Device Lett.* **40** 1155
[14] Lin Z, Hu S, Yuan Q, Zhou X and Tang F 2017 *IEEE Electron Device Lett.* **38** 1059
[15] Natarajan, Varadarajan, Hitchcock and Chow 2004 2004 *Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs* pp. 261–264
[16] Baliga B J and Chang H R 1987 1987 *International Electron Devices Meeting* pp. 658–661
[17] Xu Z, Zhang B and Huang A Q 2000 *IEEE Trans. Power Electron* **15** 916
[18] Rodov V, Ankoudinov A L and Taufik 2008 *IEEE Trans. Ind. Appl.* **44** 234
[19] Chen W, *et al.* 2017 *IEEE Electron Device Lett.* **38** 902
[20] Ye Z, Liu L, Yao Y, Lin M and Wang P 2019 *IEEE Electron Device Lett.* **40** 1159
[21] Zhou X, *et al.* 2020 *IEEE Trans. Electron Devices* **67** 582
[22] Zhang M, Wei J, Zhou X, Jiang H, Li B and Chen K J 2019 *IEEE Electron Device Lett.* **40** 79
[23] *Sentaurus Device User Guide*, Version J-2014.09, Synopsys, Mountain View, CA, USA, Sep. 2014